A Real-Time Recording System using DSP-based Multiprocessor Technology

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Keywords: DSP, radio applications, data acquisition, SCSI recording system, multiprocessor technology

Abstract - Sundance Multiprocessor Technology Ltd. has a leading role in the research and development of sophisticated products which meet the myriad requirements of system builders. Sundance is a Texas Instrument’s Third Party and it allows us to develop advanced technology in the high-performance embedded processing market [1]. The paper describes a new real-time recording system for 10MHz based-band radio applications. The product is made by a modular and complex parallel architecture using concurrent real-time software and it achieves high performance at a low cost.

1 Introduction

High-performance computers and Digital Signal Processors (DSPs) are increasingly being used to address a diverse range of automation tasks. Typically, the applications which benefit include real-time control, robotics, radio, image processing and pattern recognition. Digital signal processing brings the benefits of increased efficiency, higher quality and lower running costs to many manufacturing and industrial organizations.

Sundance products, which main features are flexibility and expandability, are typically either board level, or conform to defined module and carrier standards. In each case, they are designed to be used either as stand-alone solutions, or in multiprocessor systems.

All Sundance’s products conform to the TIM (Texas Instruments Module) standard [2] for the TMS320C4x (‘C4x) and TMS320C6x (‘C6x) DSPs.

Specifically targeted at the C40, with its six communication ports, enabling hypercube multiprocessing [3][4][5], the specification does not exclude the use of other processors such as ADCs [6], DACs [7], SCSI controllers [8], re-configurable FPGAs [9], image processing frame grabbers [10], etc.

Restrictions come in the form of pin-outs, power limits or mechanical properties. The module is intended to be reusable on different architectures, to be plugged into motherboards to build homogeneous systems. TIM modules maybe double, triple or quadruple width dependent upon the backplane.

The TIM modules are provided with a support environment in the form of carrier boards. The carrier boards provide the environment for the modules to operate and communicate with others and the host machine. Larger systems maybe built by utilising multiple motherboards.

The motherboards are available for a variety of backplanes, (PC-ISA, VME, PCI, CompactPCI, VXI, PMC). There are no restrictions on the backplane, only on the module sites. The result is, users investments are in the processing and special-to-type modules which make the system.

The paper presents a real-time data acquisition and recording system which has been already included in the range the Sundance’s products.

The system is built using a modular architecture based on TIM modules hosted on a PCI-bus carrier board. Input data are from an analog channel at a rate up to 20Mbytes/sec. The multiprocessor architecture is symmetric and it is composed of two 10 Mbytes/sec channels working in parallel. The system is able to record data into 2 SCSI disks and to backup them both to a SCSI tape and to the host harddisk. The data of each acquisition are stored in a file. A directory both on the SCSI disks and on the SCSI Tape keep track of the files.

The paper outlines the system software in Section 2. Section 3 describes the hardware architecture and the system performance are reported in Section 4. Concluding remarks are made in Section 5.

2 The system software

The system is organised with a DSP-based multiprocessor architecture where a concurrent software
design guarantees real-time performance. The user controls the system from the host by a Graphical User Interface (G.U.I.) running on an Intel platform both under WinNT and under Win9x. A custom device driver, built using the SMT6010 [11] for WinNT or using the SMT6020 [12] for Win9x, allows data transfers from the system to the host and vice versa: high performance has been reached using the SMT6015 [13], which is a WinServer developed by Sundance.

2.1 The WinDriver

The above products (SMT6010, SMT6020 and SMT6015) are based on the WinDriver [14] which architecture (Fig. 1) enables to create the hardware access application, without having to write a kernel mode device driver. All the hardware access is done in the application, through the WinDriver interface, while maintaining kernel mode performance. The device driver produced with WinDriver accesses the hardware through the WinDriver kernel agent (Windrvr.VXD / SYS) using the standard WinDriver functions.

2.2 The Graphical User Interface

The main functions under the user’s control are a single or a multi-file record on SCSI disks (the size of the sampling file and the sampling frequency are input parameters) and the backup both on SCSI tape and on the host’s harddisk. It is possible to backup a single file, or part of it, or several files. All the files are organised in a directory showing the main features for each file. In particular, there are three different kind of backup as follows and for each of them is possible to define an offset and the data size to copy:

a) SCSI Disks → Local Disk (Host)

b) SCSI Disks → SCSI Tape

c) SCSI Tape → Local Disk (Host)

Other G.U.I.’s features are the Disk Directory Control (“Ready Directory”, “Delete File” and “Wipe Directory”) and “Wipe Disks”.

2.3 The DSP code architecture

A multi-tasking, parallel and symmetric software has been designed for the Embedded System (ES) with two 10Mbytes/sec digital channel hardware architecture: sophisticated synchronisation techniques enable high system efficiency.

In particular, the record process, which is the most complex function of the system and the only one where real-time performance is essential, needs 5 concurrent tasks and two processors per channel: one channel is used to record the even 1Mbytes data frames onto a SCSI disk and the other is for the odd ones on the second SCSI disk.

More in details, the two tasks on the DSP #1 implement a double buffering technique: while the TaskA receives a frame from the source the TaskB transmits the previous frame to the processor connected with the SCSI interface. The data transfers are through comm-port (CP) (byte wide communications link, as found in the ‘C4x) and the data rate is up to 20Mbytes/sec: a sophisticated DMA technique sets three DMA channels, one for receiving data and two for transmitting data. The DMA Data Bus is shared among the three DMA channels and perform a complete “read memory” and “write memory” in about 100nsec (the memory access is 32 bits), considering that data are in the external memory where a read is performed at 30MHz and a write at 15MHz.

On the DSP#2 there are three tasks that implement a complex technique to get working in parallel the DMA bus with the SCSI bus on a continuous data flow: a double buffering approach has been used and while the TaskC and the TaskD receive a frame from the processor#1 on independent CPs the TaskE writes into the SCSI disk the previous two frames.

The design for the backup function is composed of three modules: the first is for the backup from the SCSI disk to the SCSI tape and it consists of a simple files coping, whereas the other two backups to the host’s harddisk from the two different SCSI devices is very sophisticated in transmitting data.
through the PCI bus. Actually, high performance has been reached using an optimised Scatter/Gather DMA technique both on the DSP and host side.

3 The hardware architecture
The system is based on Sundance’s OEM products, is symmetric and is composed of 2 channels working in parallel: Figure 2 shows the picture of the system and Figure 3 is the picture of the ES. The hardware of the ES is composed of the SMT320 [15], which is a PCI TIM carrier, mounting 4 TIMs: the SMT359 [6] (a single width TIM-40 compliant module consisting of a single channel 40MHz, 12-Bit ADC), the SMT315 [16] (a dual processor SRAM TIM) and two SMT307 [8] (fast wide SCSI-2 TIMs). The above TIMs are all based on Texas Instruments’s DSPs (TMS320C4x) and on re-configurable computing hardware (Altera’s FPGA or XILINX’s FPGA) guaranteeing a flexible system design.

The most relevant FPGA design is on the SMT359 that implements two main functions: the Samples Processing (SP) on the ADC module and the Linear Feedback Shift Register (LFSR) Pseudo-Random (PN) Data Generator (Fig. 4). In the SP the 12-bit ADC converts the analogue input into 12-bit samples. The FPGA then truncates samples from 12 bits to 8 bits, packs the samples in 32-bit words and interleaves the words in two 10Mbytes/sec digital channels using a 2Kbytes FIFO. The PN generator is used for the Data Integrity Test that checks if there are any data losses in the sampling and backup process.

The SMT307 consists of a Texas Instruments’s TMS320C44 (‘C44) with 4Mbytes of Enhanced Dynamic RAM (EDRAM). The TIM module uses an NCR53C720 SCSI–2 I/O processor, C720, to provide a peak transfer rate to SCSI-2 devices of 20Mbytes/s synchronously and 10Mbytes/s asynchronously. The SCSI processor is capable of processing NCR SCRIPT codes in the EDRAM without intervention from the ‘C44. The board can access 68-way 16-bit wide SCSI drives. The SMT315 is a dual processor TIM with two ‘C44 and 4Mbytes of SRAM.

4 The system performance
One analogue channel is sampled and recorded on two 18Gbytes SCSI disks at a rate of up to 20Mbytes/sec: the file size can be maximum 36Gbytes. The backup from the 2 disks to the tape is at a rate of up to 4Mbytes/sec and the backup from the 2 disks or the tape to the host is at rate of up to 45Mbytes/sec.

5 Conclusions and future work
This research describes a novel technology design of a real-time recording system used for radio applications. At present, the system is a product, called SMT8001 [17].

Future work will be focused in increasing the recording capacity from 36Gbytes up to 72Gbytes and in getting the system working with more flexible hosts both in terms of platform and O.S..

Another future development will be the extension of the ES for a real-time video recording system handling industrial format frames.

References
Fig. 2 - The Picture of the System.

Fig. 3 - The Picture of the Embedded System.

Fig. 4 – The LFSR PN Data Generator.