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Transitioning from the voice-centric services of a 2G network to the multimedia-dominated data of 2.5G and 3G presents designers of wireless infrastructure systems with a number of challenges, such as how to reduce cost per channel while effectively increasing capacity, processing higher data rates and supporting several multimedia standards simultaneously. At the same time though, designers must address the usual engineering questions of size, cost and power consumption.

Base station manufacturers need a broad portfolio of flexible products to provide a large degree of freedom when it comes to partitioning and migrating various critical tasks within systems as they evolve. Successful manufacturers will be able to efficiently customize their system offerings for each cellular technology and standard, thus enabling network evolution for service providers in a cost-effective manner.

TI’s high-performance solutions enable more simultaneous voice and data calls so that base station manufacturers can support more user terminals including cell phones, smartphones, wireless PDAs, Internet appliances and other types of devices. This results in improved profitability for the service provider, which ensures customer satisfaction for the infrastructure system manufacturer. With higher capacity systems capable of higher data rates, service providers will be able to reduce subscriber churn and generate more revenue. In addition, TI’s unmatched system expertise will help manufacturers lower development costs and rapidly deliver new 2.5G and 3G systems to market.
In wireless infrastructure (WI) systems, designers must address several cross-disciplinary issues in the signal chain or that partition of the system where signals are processed. These challenging issues involve analog, mixed-signal, DSP, and chip-rate solutions, such as operational amplifiers (op amps). Highly flexible solutions provide system designers with the right level of hardware/software partitioning for cost-effective system-level products that can be brought to market quickly. In addition, highly flexible WI systems will better protect the manufacturer’s investment in software.

For 3G base station architectures and Voice-over-Packet (VoP) applications, the combination of TI’s high-performance TMS320C64x™ DSP generation and its leading-edge ASIC capability provides customers with a winning wireless infrastructure solution. And, TI’s unparalleled silicon expertise ensures that system designers receive state-of-the-art ASIC capability.

TI’s digital upconverters (DUCs) and digital downconverters (DDCs) lead the industry in performance. These DDCs and DUCs can support multiple standards from 2G to 2.5G and 3G. With the recent introduction of the industry’s best performing 14-bit 400-MSPS DAC, TI supports high-intermediate frequencies and 3G multi-carrier applications like the four-carrier W-CDMA.

Innovative architectures and technology have made TI’s operational amplifiers some of the leading solutions in the industry. For example, the patented architecture of the THS4271 makes it the only op amp to achieve low noise, low distortion, and high slew rate with unity gain stability.

And the THS4302 leverages a new fully complimentary bipolar silicon-germanium fabrication process to deliver the first op amp with over 10 GHz of gain bandwidth. These devices and a wide selection of fully differential op amps give TI the most comprehensive array of high-speed, high-performance amplifiers for wireless infrastructure applications.
TMS320TCI100 DSP in Symbol-Rate Processing for 2G, 2.5G, and 3G Applications

Applications:
- Symbol-rate processing for 2G, 2.5G, and 3G (shown above)
- Assist in chip-rate processing
- Layer 2 processing in RNC

DSP Block Diagram – TMS320TCI100 DSP

Applications:
- Voice encode and decode (shown above)
- Network control processing
- Data formatting and routing

HIGH-PERFORMANCE DSPs INCREASE BASE STATION SYSTEM EFFICIENCY
TMS320TCI100 DSP

Get samples and application reports at: www.ti.com/device/tms320tcici100

Key Features:
- Industry-leading 90-nanometer process node
- 720 MHz core performance
- Power-efficient design (~600-mW core power)
- High integration through state-of-the-art CMOS manufacturing process
- DSP designed for wireless infrastructure applications
  - Integrated Viterbi (VCP) and Turbo (TCP) coprocessors
  - TCP supports over 35 data (384 kbps) channels
  - VCP enables over 600 voice (7.95 kbps AMR) channels
- Complements TCI110 and TCI120 receive and transmit accelerators for wideband CDMA
- Rich mix of robust peripherals
  - Two high-bandwidth (up to 10 Gbps), flexible interfaces to external memory
  - Host port with glueless interface to most GPP
  - UTOPIA II port for interface to communication network
  - PCI for high-performance standard local bus
- Object-code compatible with all TMS320C6000™ DSPs
- Pin compatible with TMS3206415 and TMS320C6416 DSPs

HIGH-DENSITY SOLUTIONS FOR VOICE-OVER-PACKET (VoP) AND DATA TRANSCODING
TMS320C55x™/TMS320C64x™ DSP Generations + Telogy Software

Get samples and application reports at: www.ti.com/wisolutions_vop

The TMS320TCI100 DSP also fits well in voice-transcoding, mobile switching-center, and media-gateway applications. Combining the optimized TCI100 solution with TI's high-density, field-hardened voice-over-packet (VoP) gateway solutions addresses the tough challenges facing service providers deploying packet-based networks.

Key Features:
- Flexible, carrier-grade solution
  - Field-proven Telogy software with over 50 million total ports shipped
  - Carrier-certified echo cancellation
- Telogy software framework optimized for the TMS320C64x and TMS320C55x DSP generations
- Extensive voice CODEC suite
  - Includes wireless codecs such as SMV, EVRC, AMR, WB-AMR and QCELP

Read more about Wireless Infrastructure solutions at www.ti.com/wisolutionsguide
COMPREHENSIVE AND CUSTOMIZABLE UMTS BASEBAND SOLUTION

UMTS Baseband Platform

TI’s UMTS wireless infrastructure digital baseband platform is a comprehensive silicon and software product offering that enables the design of low-cost, high-density UMTS channel cards. The TCI1x platform supports the 3GPP FDD Release 99 standard as well as the HSDPA channels as per Release 5 of the 3GPP FDD standard. The platform consists of a high-performance wireless infrastructure tailored DSP and tightly coupled programmable accelerators. The design achieves a low cost-per-channel solution by leveraging an efficient pooling of silicon and memory resources on the chip-rate accelerators and optimally partitioning the symbol rate and chip rate functions between the DSP and accelerators.

The UMTS platform offering includes:

TMS320TCI100 DSP
- Industry leading 720 MHz core
- VCP and TCP coprocessors
- Pin and code compatible with TMS320C64x™ DSPs

TMS320TCI110
- Single device for de-spreading, RACH and searching
- Configured and controlled via DSP
- The device is highly customizable with parameters such as number of users, number of fingers per user, correlation lengths and accumulation lengths configured via DSP software
- Efficient host interface between the TCI110 and the TCI100 DSP resulting in a high-channel-density solution

TMS320TCI120
- The TCI120 is a highly configurable downlink chip-rate accelerator
- Configured and controlled by the DSP
- The channel block is made up of 9 channel groups and supports a total of 288 downlink channel elements that can be configured as common or dedicated channels
- The TCI120 supports HSDPA as per Release 5 of the 3GPP standard
- Support for all the common channels, variable-rate dedicated channels, shared channels and compressed mode as per Release 99 of the 3GPP standard

TCI1x Platform Software
- Physical layer reference design which includes layer 1 application and physical layer services manager
- The TCI1x hardware abstraction layer abstracts the hardware implementation details
- Highly optimized symbol- and chip-rate software modules
- TCI110 and TCI120 device control software
TCIStudio Development and Evaluation Tools
- The familiar Code Composer Studio (CCStudio) suite of development tools including the debug, profiling, and tuning tools allows for faster software development
- TCISStudio suite of evaluation and analysis tools includes accelerator probes and performance analysis tools
- The TCISStudio along with the TCI1x Evaluation Module (EVM) help carry out the evaluation and performance analysis of the TCI1x accelerators and software
- The EVM also allows for initial code development before the customer’s channel card is ready

Key Features:
- Customizable and flexible hardware configured and controlled through DSP software
- Comprehensive silicon and software UMTS baseband product offering
- TCI1x hardware abstraction layer provides a higher level of device abstraction to the user enabling them to develop a hardware independent application
- CCStudio, TCISStudio and EVM reduce the time-to-market by making software development quicker and easier

Applications:
- Low-cost, high-channel-density UMTS channel card
ASIC SOLUTIONS ENABLE NEXT-GENERATION WIRELESS INFRASTRUCTURE (WI)

ASIC

For detailed information, visit:
www.ti.com/sc/asic

For further information, please contact your local TI Sales Representative (see page 2)

- Global leadership in semiconductor manufacturing
  - 0.18 µm – 55 nm (Ldrawn) nodes. 95-nm (Ldrawn) Cu product 15% faster than competition
  - High-performance/density library, I/O, and memory for varying wireless infrastructure ASIC needs
  - Packaging: High-performance flip chip
- Experienced, flexible, and global design services
  - Worldwide design center staff for on-site support
  - Experienced WI applications team for system-level support
  - Collaborative design, traditional floor planning, place and route
  - Design kit with online documentation and full application notes
- System-level integration
  - Proven success on numerous multi-million gate designs
  - IP targeting WI, high-speed interfaces, and I/O (RapidIO / SerDes)
  - IP-Ethernet, DSP, microprocessor cores, broad array of peripherals
- Comprehensive ASIC cells and tool support
  - Robust module library/rich core library
  - Open EDA tool/flow support
  - Analog converter functions

Wireless Infrastructure Applications:
- Application-specific digital downconverter/digital upconverter
- Base-band processing
  - Chip-rate and symbol-rate processing for CDMA systems
  - Combining/decombining/bridge chips
- Specialized applications
  - Viterbi/turbo decoding
  - Switching matrix
- Network control and interface processing
  - Base station uplink
  - RNC control and protocol processor
- Transcoding/echo canceller
  - Customized applications
- Embedded SOC designs
  - High performance
  - Low peak power
  - PA linearization

Leading-Edge EDA Tools

Twenty Years of ASIC Leadership
PROGRAMMABLE QUAD DDC OR DUC FOR 3G SYSTEMS

GC5016

Get samples, datasheets, application reports, and EVMs at:
www.ti.com/sc/device/gc5016

Each one of the GC5016’s four channels can be independently programmed to perform digital upconversion or downconversion of 3G systems such as W-CDMA or CDMA2000. Customers can choose to use the device as a programmable digital upconverter or downconverter. Alternatively, they can use the device to implement a two-channel upconversion and a two-channel downconversion simultaneously on a single chip.

As with its predecessors, the GC5016 continues to offer the best performance in the industry by delivering better than 115 dB of spurious-free dynamic range, exceeding industry requirements. While the maximum input data rate for each channel is the fastest in the industry (at 150 MSPS) by more than 35%, it can provide even faster input data rates of up to 300 MSPS by combining two channels for even wider bandwidth applications.

In the upconversion mode, the GC5016 accepts real or complex signals, interpolates them, and modulates them to selected intermediate frequencies that are then output to a digital-to-analog converter, such as the DAC904, DAC2904, or DAC5686. In the downconversion mode, the GC5016 accepts digital signals from an analog-to-digital converter, such as the ADS5410.

Key Features:
• Input clock rates
  – Up to 150 MSPS
  – Up to 300 MSPS in two-channel even/odd mode
• SFDR: 115 dB
• Integrated AGC
• FIR filter block consists of 16 cells providing up to 256 filter taps per channel
• 64 parallel input bits and 64 parallel output bits provide flexible I/O options
• Multiple multiplex output options
• Future-proof filter performance, clock rate, and bandwidth
• Power dissipation: 1 W at 100 MHz with all four channels in operation

Applications:
• Process four-channel UMTS in both downconvert or upconvert modes, as well as combination upconvert and downconvert mode
• Efficient and economic beamforming
• Low power is ideal for micro and pico base stations
QUAD DIGITAL UPCONVERTER PROVIDES TWO 3G W-CDMA CHANNELS
GC4116
Get samples, datasheets, and IBIS models at: www.ti.com/sc/device/gc4116

The GC4116 is the first digital upconverter (DUC) to support multiple standards. The chip can upconvert four narrowband channels and up to two UMTS/CDMA2000-3x channels. The GC4116 also can directly accept QPSK, GMSK, or QAM symbols for transmit filtering or pulse shaping.

Key Features:
- Output rates up to 106 MSPS
- Four identical upconvert channels
- 16-bit real or complex inputs, with summed output
- Independent frequency, phase and gain controls
- Serial interface controller simplifies interfacing with ASICs or DSPs
- Low power: 117 mW (per GSM channel), up to 305 mW (per UMTS channel)

Applications:
- Wireless base transceiver stations: macro, micro, and pico
- Repeaters
- Wireless local loop
- Cable headend and customer premise equipment

GC4116 DUC Block Diagram

QUAD DIGITAL DOWNCONVERTER ENABLES UMTS, MULTI-STANDARD DOWNCONVERSION
GC4016
Get samples, datasheets, and IBIS models at: www.ti.com/sc/device/gc4016

The GC4016 is the first digital downconverter (DDC) supporting multiple wireless standards, including 3G standards. The GC4016 can downconvert two UMTS/CDMA2000-3x with 2x oversampling or one channel with 4x oversampling.

Key Features:
- Input rates up to 100 MSPS
- Four independent Digital Down Convert (DDC) channels
- Independent decimation and resampling, tuning, phase and gain controls
- Built-in diagnostics
- > -115 dBC spurious free dynamic range
- Low power: 115 mW (per GSM channel), up to 620 mW (per 3.84-MB UMTS channel)

Applications:
- Cellular base transceiver stations: macro, micro, and pico
- Repeaters
- Wireless local loop
- Cable headend and customer premise equipment

GC4016 DUC Block Diagram
DAC5686 Internal Block Diagram

DAC5686 in Single Sideband Mode

DAC5686 Performance Plot

16-BIT, 500-MSPS PROGRAMMABLE DUAL DAC

DAC5686

Get datasheets at:
www.ti.com/sc/device/dac5686

DAC5686 is designed to allow low data rate transfer from the ASIC to the DAC. The DAC5686's superior performance enables transmissions of up to four W-CDMA carriers at high intermediate frequencies. The DAC5686 can be used in three modes of operation.

A. Dual-Channel

The interpolation filters increase the DAC update rate, resulting in reduced sin x/x roll off. This greatly relaxes the requirements for analog-post filtering.

B. Quadrature Modulation Mode

This mode is used for baseband modulation or a two-channel digital IF system. While channel selection is done through complex mixing in the ASIC, the DAC5686 interpolates this incoming low-data-rate signal into higher-data rates. Then, on-chip mixing using a flexible 32-bit programmable NCO provides the final IF upconversion. Optional f/4 mixing is available for lower power operation.

C. Single Sideband Upconversion Mode

This mode gives users the best interface to an analog upconverter, such as the TRF3701, for low-cost transmit solution. Complex mixing using the NCO can be used to offset the baseband signal from the LO frequency. The LO feed through an unwanted side band can then be attenuated by IF filtering at RF.

Key Features:
- 500-MSPS maximum DAC update rate
- 71 dBC SNR in 100-kHz BW for f_{OUT} ≤ 40 MHz
- -82 dB IMD for four-tone CW input signal, each tone at -12 dBFS (f_{OUT} = 15.6, 15.8, 16.2, 16.4 MHz)
- Low power dissipation: 440 mW (SSB mode)
- Selectable 2x to 16x interpolation, dual-channel
- On-chip 2x–16x PLL clock multiplier, PLL bypass mode
- Differential scalable current outputs: 2 mA to 20 mA
- 1.8-V digital / 3.3-V analog supply
- 1.8-V / 3.3-V CMOS-compatible interface
- Packaging: 100-HTQFP (PowerPAD™)

W-CDMA ACPR Performance:
- W-CDMA 1 carrier:
  - 74-dBC baseband, 245.76 MSPS
  - 77-dBC IF = 30.72 MHz, 245.76 MSPS
  - 71-dBC IF = 61.44 MHz, 245.76 MSPS
- W-CDMA 2 carrier:
  - 74-dBC IF = 30.72 MHz, 245.76 MSPS
  - 71-dBC IF = 61.44 MHz, 245.76 MSPS
  - 67-dBC IF = 122.88 MHz, 491.52 MSPS
- W-CDMA 4 carrier:
  - 67-dBC IF = 61.44 MHz, 245.76 MSPS
  - 64-dBC IF = 122.88 MHz, 491.52 MSPS

Applications:
- Cellular BTS
  - CDMA: W-CDMA, CDMA2000, IS-95
  - TDMA: GSM, IS-136, EDGE/UWC-136
- Baseband I&Q transmit
- Low-data-rate interface for quadrature modulation
- Single sideband upconversion
- Diversity transmit

Read more about Wireless Infrastructure solutions at www.ti.com/wisolutionsguide
14-BIT, 400-MSPS DAC WITH 2X/4X INTERPOLATION

DAC5674

Get samples, datasheets, app reports and EVMs at: www.ti.com/sc/device/dac5674

The DAC5674 is a digital-to-analog converter integrated with a cascade of up to two 2x interpolation filters. The digital filtering option allows either a low pass or high pass mode which enables users to select the higher-order image for increased output frequency, potentially reducing an IF mixer stage. The low-pass interpolation mode provides excellent SFDR performance that enables multi-carrier architectures in the first Nyquist zone of up to 40-MHz IF with relaxed filter requirements.

Key Features:
- High W-CDMA ACPR:
  - 73 dB @ 15.36-MHz single carrier
  - 70 dB @ 46.08-MHz single carrier and 19.2-MHz dual carrier
- 2x or 4x interpolation with configurable low-pass/high-pass mode
- On-chip PLL with bypass option
- 1.8-V Digital and 3.3-V Analog supply operation
- 1.8-V/3.3-V CMOS-compatible interface
- Packaging: 48-lead PowerPAD™ HTQFP

DUAL DACS FOR I & Q PROCESSING

DAC2900, DAC2902, DAC2904

Get samples, datasheets, and EVMs at: www.ti.com/sc/device/partnumber
Replace partnumber in URL with dac2900, dac2902, or dac2904

The two integrated DAC channels of the DAC290x family enable the I and Q channels to have close gain matching to maintain low error-vector magnitudes. These channels also provide high performance at low cost and low power. The 10-, 12-, and 14-bit family is pin compatible, allowing easy resolution upgrades.

Key Features:
- High SFDR:
  - DAC2900: 68 dB at f_{OUT} = 20 MHz
  - DAC2902: 70 dB at f_{OUT} = 20 MHz
  - DAC2904: 78 dB at f_{OUT} = 10 MHz
- Power: 310 mW
- Power-down mode: 23 mW
- Low glitch: 2 pVs
- Internal reference
- Packaging: 48-lead TQFP

Applications:
- Cellular BTS:
  - CDMA: W-CDMA, CMDA2000, IS-95
  - TDMA: GSM, IS-136, EDGE/UWC-136
- Low-data-rate interface
- Wireless local loop

Dual-Carrier W-CDMA with ACPR of 70 dB @ 19.2 MHz

DAC5674 Internal Block Diagram

DAC290x in Baseband Sampling Transmitter System
ULTRA-LOW-POWER 12-BIT, 40-MSPS DUAL DAC
DAC2932

Get samples, datasheets, app reports and EVMs at: www.ti.com/sc/device/dac2932

The DAC2932 is a 12-bit 40-MSPS dual DAC with four integrated voltage output control DACs. This DAC can be used for I and Q in wireless applications. The additional four voltage output control DACs provide wireless system cost savings by allowing the designer to control transmit and receive path gain and adjust filter and local oscillator frequencies. The use of these four control DACs simplifies the system design, provides flexibility and can provide overall system cost savings.

Key Features:
- Dual 12-bit, 40-MSPS current output DACs
- Four 12-bit Vout DACs for signal path control
- Ultra low power: 29 mW
- Adjustable full-scale output: 0.5 mA to 2 mA
- 3.3-V supplies
- Power down mode: 25 μW
- Budgetary pricing: U.S. $7.95/1 KU
- Packaging: 48-lead TQFP

LOW-COST, SINGLE DAC FAMILY
DAC904/DAC902/THS5671A/THS5661A

Get samples, datasheets, and EVMs at: www.ti.com/sc/device/partnumber
Replace partnumber in URL with dac904, dac902, ths5671a, or ths5661a

The DAC90x and THS56x1A families are pin-compatible, single DACs with 8-bit, 10-bit, 12-bit, and 14-bit options. These are the lowest-cost DACs available on the market.

Key Features:
- Update rate of 165 MSPS (DAC90x); 125 MSPS (THS56x1A)
- Analog supply of 5 V; digital supply of 3 V or 5 V
- On-chip, 1.2-V reference
- Set-up and hold times of 1 ns
- Twos complement or binary input code format (THS56x1A)
- Differential current outputs of 2 mA to 20 mA
- SFDR > 60 dBc at 27.4 MHz IF at 165 MSPS
- Low power: 175 mW at 5 V
- Packaging: 28-pin SOIC, 28-pin TSSOP (10- and 8-bit versions are also available for both families)
QUADRATURE MODULATORS
TRF3701/TRF3702

Get datasheets at:
www.ti.com/sc/device/partnumber
Replace partnumber in URL with trf3701 or trf3702

TRF3701 and TRF 3702 are low-noise quadrature-direct modula-
tors capable of converting complex input signals from 0–250
MHz IF up to RF. An internal analog combiner sums the real and
imaginary components of the RF output. The modulators are
implemented as a double-balanced mixer. An internal LO phase
splitter accommodates a single LO input.

Key Features:
• TRF3701: IF to 900 MHz
• TRF3702: IF to 2 GHz
• Typical optimized carrier suppression > 50 dBc
• Typical optimized sideband suppression > 50 dBc
• Typical noise floor; -157 dBm/Hz at 700 to 900 MHz
• 5-V single supply

INTEGER-N RF PLL SYNTHESIZER
TRF3750

Get samples, datasheets, app reports and EVMs at:
www.ti.com/sc/device/trf3750

The TRF3750 is frequency synthesizer that can be used to imple-
ment local oscillators (LO) up to 3 GHz in the RF upconversion
and downconversion chains of wireless transmitters and
receivers. A complete Phase Locked Loop (PLL) can be imple-
mented using an external loop filter and a Voltage-Controlled
Oscillator (VCO) together with the TRF3750. The very wide fre-
quency range simplifies system complexity and reduces cost.

Key Features:
• Supports operation up to 3 GHz
• Supply voltage of 2.7 V to 5.5 V
• Programmable charge pump currents
• Programmable anti-backlash pulse width
• Analog and digital lock detect
• Low phase noise
• Extended VCO control range through independent VCP supply
• Hardware and software power down
• Packaging: 16-lead TSSOP

Applications:
• Cellular BTS:
  – CDMA: W-CDMA, CDMA2000, IS-95
  – TDMA: GSM, IS-136, EDGE/UWC-136
• Wireless local loop
• Wireless LAN 802.11
• LMDS, MMDS
12-BIT ADC WITH INTEGRATED DDC
AFE8201

Get samples, datasheets, app reports and EVMs at: www.ti.com/sc/device/afe8201

The AFE8201 is an 80-MSPS, 12-bit ADC that includes a digital downconverter (DDC) and user-programmable digital filters. It is designed to sample IF signals and digitally mix, filter, and decimate the signals to baseband. An integrated 12-bit DAC is included to control the gain of the IF block. This highly integrated device simplifies and reduces costs for receiver applications.

Key Features:
- 12-bit, 80-MSPS ADC
- Integrated digital down converter
- 32-bit NCO
- Digital filters
- User-programmable coefficients
- McBSP interface for TI DSPs
- 12-bit control DAC
- Budgetary pricing: U.S. $25/1 KU

LOWEST-POWER, LOWEST-COST ADC FOR BTS RECEIVERS
ADS5410

Get samples, datasheets, and EVMs at: www.ti.com/sc/device/ads5410

The 12-bit, 80-MSPS ADC offers the lowest power at this performance level. It is a low-cost alternative to expensive 14-bit ADCs and can be implemented in cost-reduction programs for existing systems or startup of 3G systems.

Key Features:
- 12 bit, 80 MSPS
- SFDR: 75 dB at 100-MHz IF
- SNR: 60 dB at 70-MHz IF
- Digital outputs from 1.6 V – 3.3 V in 2s complement
- Flexible clocking: Single-ended or differential
- Power: 360 mW

Applications:
- Performance supports across cellular standards
  - W-CDMA / CDMA2000 / GPRS / EDGE / GSM / IS-95
- Wireless local loop / LMDS / MMDS
- Point-to-point microwave
50-MHz TO 400-MHz CASCADEABLE IF AMPLIFIERS

THS9000/THS9001

Get samples, datasheets, app reports and EVMs at:
www.ti.com/partnumber
Replace partnumber in URL with ths9000 or ths9001

The THS9000 and THS9001 are medium power, cascadeable, gain block optimized for 50-MHz to 400-MHz IF frequencies. The amplifiers incorporate internal impedance matching to 50\,\Omega. The part mounted on the standard EVM achieves greater than 15\,\text{dB} input and output return loss from 50 MHz to 325 MHz with \(V_S = 5\,\text{V}, R_{\text{BIAS}} = 237\,\Omega, L_{\text{COL}} = 470\,\text{nH}\). Design requires only 2 dc blocking capacitors, 1 power supply bypass capacitor, 1 RF choke, and 1 bias resistor. The THS9000 comes in a very small 2x2-mm leadless MSOP package, and the THS9001 comes in a 6-pin SOT23 package. These devices make excellent choices for driving SAW filters, buffering LOs, or general-purpose IF amplifiers.

**Key Features:**
- \(O I P_3: 37\,\text{dBm} at 300 \text{MHz}\)
- Gain: 15.5\,\text{dB}
- Noise figure: 4.0\,\text{dB} at 300 \text{MHz}
- 1 dB compression: 20.6\,\text{dBm}

HIGH-SPEED, FULLY DIFFERENTIAL OP AMP

THS4502/THS4503

Get samples, datasheets, and EVMs at:
www.ti.com/sc/device/partnumber
Replace partnumber in URL with ths4502 or ths4503

The THS4502, featuring power-down capability, and the THS4503, without power-down capability, set new performance standards for fully differential amplifiers with unsurpassed linearity, supporting 14-bit operation through 40 MHz.

**Key Features:**
- 370-MHz bandwidth (\(V_{\text{CC}} = \pm 5\,\text{V}, R_f = 392\,\Omega, G = 0\,\text{dB}\))
- Slew rate: 2800\,\text{V/\mu s}
- \(O I P_3 = +38\,\text{dBm} at 30 \text{ MHz (G = 12 dB)}\)
- \(N F = 25\,\text{dB (G = 12 dB)}\)
- Differential input/differential output
- Output common-mode voltage control
- Balanced architecture rejects common-mode noise and reduces even order harmonic distortion

Applications:
- IF amplifier
- TDMA: GSM, IS-136, EDGE/UWE-136
- CDMA: IS-95, UMTS, CDMA2000
- Wireless local loop
- Wireless LAN: IEEE 802.11
- Radio links
### FIXED-GAIN, HIGH-SPEED OP AMP WITH POWER DOWN

**THS4302**

Get samples, datasheets, and EVMs at:  
[www.ti.com/sc/device/ths4302](http://www.ti.com/sc/device/ths4302)

The THS4302 is an ultra-low-distortion, single-supply-operation, wide-bandwidth, high-speed amplifier ideal for use with high-resolution data converters. These voltage feedback amplifiers can operate from a single 5-V power supply while delivering a performance level of -88 dBc third-order intermodulation distortion (IMD3) at 100 MHz.

**Key Features:**
- 2.4-GHz bandwidth
- G = 14 dB (non-inverting)
- Slew rate: 5500 V/µs
- NF = 16 dB
- OIP2 = 39 dBm at 100 MHz (RL = 100 Ω)
- High output drive, IO = ±180 mA (typ)
- V5 = 3 V to 5 V
- Evaluation module available
- Packaging: Leadless packages

### ULTRA-LOW-DISTORTION, HIGH-SPEED OP AMPS WITH SHUTDOWN

**THS4271/THS4275**

Get samples, datasheets, and EVMs at:  
[www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

Replace partnumber in URL with ths4271 or ths4275

The THS4271 and THS4275 are ultra-low distortion and noise, single-ended 5-V operation, wide-bandwidth, high-speed amplifiers. They are ideal for use with high-resolution data converters. These voltage-feedback amplifiers have a power supply range of 4.5 V to 15 V while delivering a performance level of -90 dB of harmonic distortion (THD) at 30 MHz.

**Key Features:**
- HD2 = -92 dBc (f = 30 MHz, RL = 150 Ω, V0 = IVPP)
- HD3 = -95 dBc (f = 30 MHz, RL = 150 Ω, V0 = IVPP)
- 3-nV/√Hz input noise voltage
- 1.4-GHz bandwidth (-3 dB, G = +1)
- Slew rate: 1000 V/µs
- 25-ns settling time (0.1%)
- High output drive, IO = 160 mA (typ)
- Wide range of power supplies: ±2.5 V to ±75 V

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**Bit Error Rate (BER) vs Frequency for a 10 Gbps Transmitter with a Thomson THS4275**

- **BER** vs Frequency
- **THS4275**
- **BER = 10^-12**
- **Frequency = 10 Gbps**
- **Transmitter Power = 0dBm**
- **THS4275**

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**Signal Chain**

- **General Overview**
- **Timing & Interface**
- **Logic**
- **Power Management**

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**Read more about Wireless Infrastructure solutions at [www.ti.com/wisolutionsguide](http://www.ti.com/wisolutionsguide)**
2-GHz, LOW DISTORTION, CURRENT FEEDBACK AMPLIFIER
THS3202

Get samples, datasheets, app reports and EVMs at: www.ti.com/sc/device/ths3202

The THS3202 is a low-distortion, high slew rate op amp ideally suited for applications driving loads sensitive to distortion at high frequencies. It provides well-regulated AC performance characteristics with a power supply range of 6.6 to 15 V. The device’s low differential gain/phase error makes it ideal for video line driver applications, test and measurement systems and RF and IF amplifier stages.

Key Features:
- Unity-gain bandwidth: 2 GHz
- High slew rate: 9000 V/µs
- IMD3 at 120 MHz: –89 dBc (ref measurement circuit)
- OIP3 at 120 MHz: 43 dBm (ref measurement circuit)
- NF = 175 dB (ref measurement circuit)
- High output current: ±115 mA into 20 Ω R_L
- Power supply voltage range: 6.6 V to 15 V
- Packaging: 6-lead SO, 8-lead MSOP

3–9-GHz GBW, ULTRA-LOW NOISE, VOLTAGE FEEDBACK OP AMPS
OPA846/OPA847

Get samples and datasheets at: www.ti.com/sc/device/partnumber

Replace partnumber in URL with opa846 or opa847

The OPA847 combines very-high-gain bandwidth and large signal performance with an ultra-low input noise voltage (0.85 nV/√Hz), while using only 18 mA of supply current. As a voltage gain stage, the OPA847 is optimized for a flat frequency response at a gain of +20 V/V and is stable down to gain as low as +12 V/V. New external compensation techniques allow the OPA847 to be used at any inverting gain with excellent frequency response control. Using this technique in a differential ADC interface application, as shown, can deliver one of the highest dynamic range interfaces available.

Applications:
- High dynamic range ADC preamps
- Wideband, high gain amplifiers
ULTRA-WIDE BAND, CURRENT FEEDBACK OP AMP WITH DISABLE
OPA695

Get samples and datasheets at: www.ti.com/sc/device/opa695

The OPA695 is a very-high bandwidth, current-feedback op amp that combines 4200-V/µs slew rate and low-input voltage noise to deliver a precision, low-cost, high-dynamic range IF amplifier. Optimized for high-gain operation, the OPA695 is ideally suited to buffering SAW filters.

Key Features:
- Gain = +2 bandwidth: 900 MHz
- Gain = +8 bandwidth: 420 MHz
- Ultra-high slew rate: 4200 V/µs
- 3rd order intercept: > 40 dBm (f < 50 MHz)

Applications:
- Very wideband ADC driver
- Video line driver
- ARB waveform output driver

WIDEBAND, ULTRA-LOW-NOISE, VOLTAGE FEEDBACK AMPLIFIER
OPA687

Get samples and datasheets at: www.ti.com/sc/device/opa687

The OPA687 combines a very high gain bandwidth and large signal performance with an ultra-low input noise voltage while dissipating only 18-mA supply current. The low input noise voltage and its very-high, two-tone intercept can be used as a fixed-gain IF amplifier.

Key Features:
- High gain bandwidth: 3.8 GHz
- Low input voltage noise: 0.95 nV/√Hz
- Stable for G ≥ 12
- Two-tone, 3rd-order intercept: 43 dBm

Applications:
- RF/IF amplifier
- Low-distortion ADC driver
16-BIT RISC FLASH MCU FOR ONLY $0.99

MSP430F11x1

Get samples, datasheet, application reports, and EVMs at: www.ti.com/sc/msp430

A new class of low-power, advanced RISC-architecture MCUs, TI’s family of Flash-based MSP430 MCUs consume just 250 micro-amps at 1 MHz and feature TI’s analog and digital signal processing expertise.

Key Features:
- Ultra-low-power consumption, 250-µA active, 0.8-µA standby at 2.2 V (typ)
- 16-bit RISC architecture enables new applications at a fraction of the code size
- Integrated analog comparator is ideal for precise mixed-signal measurement
- Multifunctional, 16-bit multichannel timer with PWM, capture, and compare capability
- In-system programmable Flash permits last-minute code changes, field upgrades, and data logging to Flash
- The MSP-FET430X110 offers a completely integrated development environment for only U.S. $49
- New, small 4×4-mm QFN packaging available 4Q 2003

16-BIT RISC FLASH MCU WITH INTEGRATED 12-BIT ADC, MULTIPLIER, AND USARTs

MSP430F14x

Get samples, datasheets, application reports, and EVMs at: www.ti.com/sc/msp430

Experience the ultimate SoC solution for low-power applications. The MSP430F14x features the combination of ultra-low power consumption and integrated high-performance analog peripherals ideal for cost, power, and space-sensitive applications.

Key Features:
- Ultra-low power consumption: 250-µA active mode, 0.8-µA standby mode at 2.2 V (typ)
- 16-bit RISC architecture enables new applications at a fraction of the code size
- High-performance integrated analog and digital peripherals including a 200-ksps, 12-bit A/D converter, to reduce system cost and speed time-to-market
- Serial communication interface (USART) functions as asynchronous UART or synchronous SPI interface
- Two 16-bit PWM timers allow highly flexible multichannel capture and compare
- In-system programmable Flash permits last-minute code changes, field upgrades, and data logging to Flash
- The MSP-FET430P140 offers a completely integrated development environment for only U.S. $99
### High-Speed Amplifiers

#### Voltage-Feedback Op Amps

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<th>Slew Rate (V/µs)</th>
<th>THD (dBc)</th>
<th>Gain/Phase (°)</th>
<th>VOS (mV)</th>
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#### Current-Feedback Op Amps

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<th>THD (dBc)</th>
<th>Gain/Phase (°)</th>
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1 Suggested resale price in U.S. dollars in quantities of 1,000.

Preview devices are listed in blue.
New devices are listed in red.
Continued on next page
### D/A CONVERTERS

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<th>Device Name</th>
<th>Resolution (Bits)</th>
<th>Supply (V)</th>
<th>Update Rate (MSPS)</th>
<th>Settling Time (ns)</th>
<th>Number of DACs</th>
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### A/D CONVERTERS

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<th>Sample Rate (MSPS)</th>
<th>Supply (V)</th>
<th>Analog Inputs</th>
<th>Power Typ (mW)</th>
<th>Analog Input BW (MHz)</th>
<th>DNL Max (±LSB)</th>
<th>INL Max (±LSB)</th>
<th>SNR (dB)</th>
<th>Pin/Package</th>
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* Suggested resale price in U.S. dollars in quantities of 1,000.
* AFE8201 integrates programmable DDC, PG4, and Control DAC. Directly interfaces to TI TMS320C5500™ and TMS320C6000™ DSP platforms with McBSP port.
## DIGITAL DOWNCONVERTERS/UPCONVERTERS (DDC/DUC)

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<th>Wideband Channels</th>
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<th>Power (max) / Channel</th>
<th>Special Features</th>
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1C = ROM, F = Flash
2Suggested resale unit price in U.S. dollars in quantities of 1,000.
3All devices support industrial temperature range.
4Planned release 1Q 2004.

## MSP430 ULTRA-LOW-POWER MICROCONTROLLERS

### Flash-Based Ft1xx Family (Vcc 1.8 to 3.6 V)

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<th>WDT</th>
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<th>SMS</th>
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1C = ROM, F = Flash
2Suggested resale unit price in U.S. dollars in quantities of 1,000.
3All devices support industrial temperature range.
4Planned release 1Q 2004.
TIMING AND INTERFACE PRODUCTS

Wireless Infrastructure (WI) systems will accommodate a wider range of technologies than ever before as the industry moves from 2G to 2.5G and 3G. Advanced wireless technologies like Bluetooth™ personal area networking (PAN), wireless local area networking (WLAN) with IEEE 802.11 technology, and leading wireless protocols like GSM, CDMA, and UMTS all place higher demands on WI systems for greater processing performance without jeopardizing power consumption or cost characteristics.

Designers realize that the increased data rates must be supported by base station and controller backplanes and the interconnections between these systems. Typically, this means the standard backplane either has to speed up or become wider, moving from 16-bit to 32-bit and beyond.

TI's timing and interface components simplify the generation of timing signals that are used to synchronize system activity and meet today's stringent clock-signal timing requirements. A wide selection of high-fan-out drivers, repeaters, and translators provide benefits like low propagation delay, low jitter, and reduced skew, in addition to driving high-performance clocking systems.

TI timing and interface products that support wireless infrastructure applications include:

- Serializer/Deserializer (SerDes) devices ranging from 100 Mbps to 3.125 Gbps, based on LVDS or LVPECL technology
- Repeaters, translators, and multiplexers transmitting at speeds up to 2.0 Gbps with less than 65-ps total jitter
- Single-ended and differential bi-directional transceivers supporting multipoint topologies
- Clock solutions that buffer, synchronize, divide, and multiply with low-phase noise
- PHY and link 1394 (FireWire™) solutions*
- Low-noise GTLP solutions

*See www.ti.com/connectivity for information

100-MHz to 600-MHz, 10-Bit LVDS Serializer/Deserializer (SerDes) Chipsets

TO KNOW MORE

For detailed information about timing and interface ICs for wireless infrastructure:
- Transceivers and receivers 25
- Clock drivers 28
- GTLP 30
- Product selection guides 31

[Diagram of 100-MHz to 600-MHz, 10-Bit LVDS Serializer/Deserializer (SerDes) Chipsets]
HIGH-SPEED, POINT-TO-POINT 8-CHANNEL GIGABIT ETHERNET TRANSCEIVERS

**TLK2208**

Get datasheets at: www.ti.com/sc/device/tlk2208

The TLK2208 is TI’s third generation of gigabit Ethernet transceivers that combines high-port density and ultra-low power in a small-form-factor footprint. The device provides for high-speed, full-duplex, point-to-point data transmissions based on the IEEE 802.3z 1000-Mbps Ethernet specification.

**Key Features:**
- New: eight-channel gigabit Ethernet transceiver
- Selectable 8-B/10-B encoding/decoding
- Two data sampling modes (multiplex mode or nibble mode) enable a reduced pin count for interfacing MAC, ASIC, or FPGA
- Each channel operates from 1.0 – 1.3 Gbps
- Provides a maximum total aggregated data bandwidth of 8.32 Gbps over a copper or optical media interface

GIGABIT ETHERNET- AND FIBRE CHANNEL-COMPLIANT TRANSCEIVERS

**TLK1201/TLK2201**

Get datasheets, samples, and application reports at: www.ti.com/sc/device/partnumber

Replace partnumber in URL with tlk1201 or tlk2201

TI’s TLK1201 and TLK2201 gigabit Ethernet- and fibre channel-compliant transceivers require 8-B/10-B encoded data on the parallel side. The devices can be run in either normal 10-bit mode or a reduced 5-bit mode, which clocks in data on the rising and falling clock edges (DDR mode).

**Key Features:**
- Low power consumption: <200 mW at 1.25 Gbps
- LVPECL compatible differential I/O on high-speed interface
- Single monolithic PLL design
- Receiver differential input thresholds 200 mV (min)
- IEEE 802.3 gigabit Ethernet compliant
- 2.5-V supply voltage for lowest-power operation
- 3.3-V tolerant on LVTTI inputs
- Hot-plug protection
- Industrial temperature range from -40°C to 85°C
- Packaging: 64-pin VQFP, thermally enhanced (PowerPAD™)

Applications:
- Building blocks for developing point-to-point baseband data transmission over controlled impedance media of 50 Ω
- BTS backplane
- Radio card-to-controller interconnect

**Applications:**
- High-port-density applications where board space and power are limited
- Point-to-point base station and controller backplane links (shown above)
LVDS SerDes BACKPLANE TRANSMITTER/RECEIVER CHIPSETS

SN65LV1021, SN65LV1023, SN65LV1212, SN65LV1224

Get datasheet and samples at: www.ti.com/sc/device/partnumber
Replace partnumber in URL with sn65lv1021, sv65lv1023, sn65lv1212, or sn65lv1224

TI’s SN65LV1021/1023 transmitter and SN65LV1212/1224 receiver family of devices is designed to provide BTS backplane solutions between 100 Mbps and 660 Mbps. The chipset has a 10-bit LVTTL parallel-side input/output and a high-speed LVDS serial-side input/output.

Key Features:
- 100-Mbps to 400-Mbps serial LVDS data payload bandwidth at 10-MHz to 40-MHz system clock (SN65LV1021/23)
- 300-Mbps to 660-Mbps serial LVDS data payload bandwidth at 30-MHz to 66-MHz system clock (SN65LV1212/24)
- Pin-compatible superset of NSM DS92LV1021/1212, NSM DS92LV1023/1224
- Chipset (serializer/deserializer) power consumption: <250 mW (typ) (Tx) and <400 mW (typ) (Rx)
- Synchronization mode for faster lock

16:1 SERIALIZER/DESERIALIZER TRANSCEIVERS WITH PRBS TESTABILITY

TLK1501, TLK2501, TLK2701, TLK2711, TLK3101, TLK4015

Get datasheets, samples, EVMs, and application reports at: www.ti.com/sc/device/partnumber
Replace partnumber in URL with tlk1501, tlk2501, tlk2701, tlk2711, tlk3101, or tlk4015

TI’s TLK1501, TLK2501, TLK2701, TLK2711, TLK3101, and TLK4015 provide a 16-to-1 serializer/deserializer (SerDes) function with supported data rates from 600 Mbps to 3.125 Gbps. The devices feature built-in 8-B/10-B encoding/decoding for easier design.

Key Features:
- Hot-plug protection
- 2.5-V power supply for low-power operation
- Programmable voltage output swing on serial output
- Interfaces to backplane, copper cables, or optical converters
- Rated for industrial temperature range
- On-chip 8-bit/10-bit encoding/decoding
- On-chip PLL provides clock synthesis from low-speed reference
- Receiver differential input thresholds 200 mV (min)
- Loss-of-signal (LOS) detection
- Packaging: 64-pin VQFP (PowerPAD™) (TLK1501, TLK2501, TLK2701, TLK3101), 80-pin Microstar Junior™ BGA (GQE) (TLK2711), BGA (TLK4015)

Applications:
- Radio-to-controller card links
- Antenna-to-receiver link
- BTS backplane

Single-Channel and Multichannel Devices for Radio-to-Controller Card Interfaces

Applications:
- Radio-to-controller card
- Antenna-to-receiver card
- BTS backplane
### 3- or 4-Channel, Point-to-Point Transmitter and Receiver Pair

**SN65LVDS96, SN65LVDS95, SN65LVDS93, SN65LVDS94**

Get datasheet, samples, EVMs, and application reports at: [www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

Replace partnumber in URL with sn65lvds96, sn65lvds95, sn65lvds93, or sn65lvds94

The SN65LVDS9x family of devices is a 3- or 4-channel (3 or 4 data channels, plus 1 clock channel) point-to-point transmitter and receiver pair which supports up to 1.365/1.820 Gbps of data throughput. It accepts 21/28 LVTTL inputs and outputs 3 or 4 LVDS lines in parallel with a clock signal.

### Key Features:
- Operates with a single 3.3-V supply
- 5-V tolerant input
- Rising-clock-edge-triggered outputs
- Wide phase-lock input frequency range
- Low-voltage TTL (LVTTL) logic output levels
- Pin compatible with NSC:
  - DS90CR213 → SN65LVDS95
  - DS90CR214 → SN65LVDS96
  - DS90CR285 → SN65LVDS93
  - DS90CR286 → SN65LVDS94
- Industrial temperature qualified: $T_A = -40°C$ to $85°C$

### LVPECL/CML/LVDS Repeaters/Translators and Crosspoint Switches

**SN65LVDS100, SN65LVDS101, SN65CML100, SN65LVDS122, SN65LVDS125, SN65LVCP22, SN65LVCP23**

Get samples, datasheets, and EVMs at: [www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

Replace partnumber in URL with sn65lvds100, sn65lvds101, sn65cml100, sn65lvds122, sn65lvds125, sn65lvcp22, or sn65lvcp23

These high-speed repeaters/translators and crosspoint switches feature internal differential signal paths maintain for very low pulse and channel-to-channel skews.

### Key Features:
- Total jitter < 65 ps
- Pulse skew < 50 ps
- All devices accept LVDS, CML, and LVPECL inputs
- 1:1 Translator repeaters
  - LVDS100 with LVDS output
  - LVDS101 with LVPECL output
  - CML100 with CML output
- Crosspoints
  - LVDS122 2×2 – LVDS output
  - LVDS125 4×4 – LVDS output
  - LVCP22 2×2 – LVDS output
  - LVCP23 2×2 – LVPECL output

---

**Applications:**
- Base station backplane
- Radio-to-controller card links

**Eye Pattern of LVDS100**

**Key Features:**
- Total jitter < 65 ps
- Pulse skew < 50 ps
- All devices accept LVDS, CML, and LVPECL inputs
- 1:1 Translator repeaters
  - LVDS100 with LVDS output
  - LVDS101 with LVPECL output
  - CML100 with CML output
- Crosspoints
  - LVDS122 2×2 – LVDS output
  - LVDS125 4×4 – LVDS output
  - LVCP22 2×2 – LVDS output
  - LVCP23 2×2 – LVPECL output

---

**Applications:**
- CML/LVPECL-to-LVDS translator
- LVDS/CML-to-LVPECL translator
- 2x2 Crosspoint and 2:1 Mux
- 4x4 Crosspoint, 4:1 Muxs

---

**Read more about Wireless Infrastructure solutions at [www.ti.com/wisolutionsguide](http://www.ti.com/wisolutionsguide)**
MULTIPOINT-LVDS FOR BACKPLANES AND CABLES
SN65MLVD080, SN65MLVD082, SN65MLVD200, SN65MLVD201, SN65MLVD202, SN65MLVD203, SN65MLVD204, SN65MLVD205, SN65MLVD206, SN65MLVD207

Add Clock Source, e.g., 8 kHz, 19 MHz ... X < 100 MHz

Applications:
- Clock distribution
- Base station control and data bus
- Synchronization signals
- PICMG 3.0 ATCA telephony clock interface

TI introduces the industry’s first family of transceivers compliant with the Multipoint Low-Voltage Differential Signaling (M-LVDS) specification TIA/EIA-899. The SN65MLVD20x parts are half- and full-duplex single-channel transceivers. The SN65MLVD08x devices are 8-channel half-duplex transceivers that can operate at 125 MHz with up to 32 devices.

Key Features:
- Half power, 10x speed of RS-485
- Complies with M-LVDS Standard (TIA/EIA-899) – also supported by alternative vendors
- Supports wired-OR configuration – ideal for control lines
- Hot-plugging capability enhances reliability and robustness
- Controlled rise times for longer stub lengths

LOW-VOLTAGE CLOCK DRIVERS FOR CLOCK-DISTRIBUTION APPLICATIONS
CDCLVP110/CDCLVD110

Get datasheets and application reports at: www.ti.com/sc/device/partnumber

Add partnumber in the URL with cdclvp110 or cdclvd110

TI’s CDCLVP110 and CDCLVD110 low-voltage clock drivers support low-skew, low-jitter differential LVDS/LVPECL or HSTL (selectable) inputs (CLK0, CLK1) to 10 pairs of differential LVPECL clock outputs with minimum skew.

Key Features:
CDCLVP110
- 2.5-V or 3.3-V support
- Selectable clock input through CLK_SEL
- Low-output skew (15 ps) max
- Cycle-to-cycle jitter less than 1 ps (rms)
- Packaging: 32-pin TQFP

CDCLVD110
- Accepts LVDS, LVTL, HSTL, CML, or LVPECL signaling levels
- Signaling-rate capability up to 1.1 GHz
- Full rail-to-rail common-mode range
- Low output skew (30 ps)
- Packaging: 32-pin LQFP (VF)

Applications:
- Base stations, BB card, LTU
- Cable modem headend
LOW-JITTER CLOCK MULTIPLIER WITH PROGRAMMABLE DELAY AND PHASE ALIGNMENT

CDCF5801

Get application notes and datasheets at: www.ti.com/sc/device/cdcf5801

The CDCF5801 provides clock multiplication from a reference clock (REFCLK) signal. It also allows delay or advance of the CLKOUT/CLKOUTB with steps of 2.6 mUI through a unique aligner.

Key Features:
- Low-jitter clock multiplier ×1, ×2, ×4 or ×8
  - Input frequency: 12.5 to 240 MHz
  - Output frequency: 25 to 280 MHz
- Low-jitter clock divider /2, /4 or /8
  - Input frequency: 12.5 to 240 MHz
  - Output frequency: 25 to 280 MHz
- 2.6-mUI programmable bidirectional delay steps
- One single-ended input and one differential output pair
- Output can drive LVPECL, LVDS and LVTTL
- Spread spectrum clock tracking ability to reduce EMI
- Industrial temperature range: –40°C to 85°C

3.3-V X4 CLOCK MULTIPLIER WITH 8 OUTPUTS

CDCVF25084

Get application notes and datasheets at: www.ti.com/sc/device/cdcvf25084

The CDCVF25084 is a high-performance, low-skew, low-jitter, phase-lock loop clock multiplier. It uses a PLL to precisely align, in both frequency and phase, the output clocks to the input clock signal including a multiplication factor of four. The CDCVF25084 operates from a nominal supply voltage of 3.3 V. The device also includes integrated series-damping resistors in the output drivers that make it ideal for driving point-to-point loads.

Key Features:
- Phase-locked loop-based zero-delay buffer
- Operating frequency range: 10 MHz to 200 MHz
- Low jitter (cycle-cycle)
- Distributes one clock input to two banks of four outputs
- Auto frequency detection to disable device (power-down mode)
- Consumes less than 20 µA in power-down mode
- Packaging: 16-pin TSSOP

Applications:
- Telecom
- Datacom
Gunning Transceiver Logic Plus
GTLP Family

TI provides backplane interface solutions for telecom/datacomm end equipment with the open-drain GTLP technology, which provides better signal integrity and overall system improvement over traditional logic, allowing you to drive heavily loaded backplanes.

Key Features:
- GTLP low-output-voltage swing reduces EMI
- Reduced-input GTLP threshold provides adequate noise margin
- I_{off}, power-up 3-state, and BIAS V_{CC} support live insertion
- Bi-directional interface between GTLP and LVTTL signal levels
- 5-V tolerant LVTTL I/Os allow mixed-voltage systems
- Up to 100-mA drive capability to drive heavily loaded backplanes
- Packaging: Space-saving TSSOP (DGG), TVSOP (DGV), and LFBGA (GKE/GKF) packages

Applications:
- Base stations
- Networking

Single-Bit Representation of a Multipoint Parallel Backplane

Signal Integrity: TI vs. Competition

† Unloaded backplane trace natural impedance (Z_0) is 45 Ω. 45 to 60 Ω is allowed with 50 Ω being ideal.
‡ Card stub natural impedance (Z_0) is 60 Ω.

Gunning Transceiver Logic Plus
GTLP Family

Get samples, datasheets, and application reports at:
www.ti.com/sc/gtlp

TI provides backplane interface solutions for telecom/datacomm end equipment with the open-drain GTLP technology, which provides better signal integrity and overall system improvement over traditional logic, allowing you to drive heavily loaded backplanes.

Key Features:
- GTLP low-output-voltage swing reduces EMI
- Reduced-input GTLP threshold provides adequate noise margin
- I_{off}, power-up 3-state, and BIAS V_{CC} support live insertion
- Bi-directional interface between GTLP and LVTTL signal levels
- 5-V tolerant LVTTL I/Os allow mixed-voltage systems
- Up to 100-mA drive capability to drive heavily loaded backplanes
- Packaging: Space-saving TSSOP (DGG), TVSOP (DGV), and LFBGA (GKE/GKF) packages

Applications:
- Base stations
- Networking
### SERIAL GIGABIT SOLUTIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Function</th>
<th>Data Rate</th>
<th>Serial I/F</th>
<th>Parallel I/F</th>
<th>Power</th>
<th>Special Features</th>
<th>Price1</th>
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<tr>
<td>TLK1501</td>
<td>Single-ch. 16:1 SerDes</td>
<td>0.6–1.5 Gbps</td>
<td>1 CML ch.</td>
<td>16 LVTTL lines</td>
<td>200 mW</td>
<td>Built-in testability</td>
<td>Web</td>
</tr>
<tr>
<td>TLK2501</td>
<td>Single-ch. 16:1 SerDes</td>
<td>1.6–2.5 Gbps</td>
<td>1 CML ch.</td>
<td>16 LVTTL lines</td>
<td>300 mW</td>
<td>Built-in testability</td>
<td>Web</td>
</tr>
<tr>
<td>TLK2701</td>
<td>Single-ch. 16:1 SerDes</td>
<td>1.6–2.5 Gbps</td>
<td>1 CML ch.</td>
<td>16 LVTTL lines</td>
<td>300 mW</td>
<td>Built-in testability and K character control</td>
<td>Web</td>
</tr>
<tr>
<td>TLK2711</td>
<td>Single-ch. 16:1 SerDes</td>
<td>1.6–2.5 Gbps</td>
<td>VML</td>
<td>16 LVTTL lines</td>
<td>350 mW</td>
<td>MicroStar Jr™ BGA packaging</td>
<td>Web</td>
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<tr>
<td>TLK3101</td>
<td>Single-ch. 16:1 SerDes</td>
<td>2.5–3.125 Gbps</td>
<td>1 VML ch.</td>
<td>16 LVTTL lines</td>
<td>350 mW</td>
<td>Built-in testability</td>
<td>Web</td>
</tr>
<tr>
<td>TLK1201</td>
<td>Single-ch. 10:1 gigabit Ethernet xcvr</td>
<td>0.6–1.3 Gbps</td>
<td>1 LVPECL ch.</td>
<td>10 LVTTL lines</td>
<td>200 mW</td>
<td>Industrial temperature</td>
<td>Web</td>
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<tr>
<td>TLK2201</td>
<td>Single-ch. 10:1 gigabit Ethernet xcvr</td>
<td>1.0–1.6 Gbps</td>
<td>1 LVPECL ch.</td>
<td>10 LVTTL lines</td>
<td>200 mW</td>
<td>JTAG; 5-bit DDR mode</td>
<td>Web</td>
</tr>
<tr>
<td>TLK2201I</td>
<td>Single-ch. 10:1 gigabit Ethernet xcvr</td>
<td>1.2–1.8 Gbps</td>
<td>1 LVPECL ch.</td>
<td>10 LVTTL lines</td>
<td>200 mW</td>
<td>JTAG; 5-bit DDR mode, industrial temp. qualified</td>
<td>Web</td>
</tr>
<tr>
<td>TLK2201JR</td>
<td>Single-ch. 10:1 gigabit Ethernet xcvr</td>
<td>1.0–1.6 Gbps</td>
<td>1 LVPECL ch.</td>
<td>10 LVTTL lines</td>
<td>200 mW</td>
<td>MicroStar Jr. 5 × 5 Land Grid Array (LGA)</td>
<td>Web</td>
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<tr>
<td>TLK2208</td>
<td>Eight-ch. of 10:1 or 8:1 gigabit Ethernet xcvr</td>
<td>1.0–1.3 Gbps</td>
<td>8 CML ch.</td>
<td>4/5-bit/ch (nibble DDR mode), 8/10-bit/ch (multiplex ch. mode)</td>
<td>1 W</td>
<td>JTAG, MDIO supported</td>
<td>Web</td>
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<tr>
<td>TLK4015</td>
<td>Four ch. of 16:1 xcvr</td>
<td>0.8–1.56 Gbps</td>
<td>4 CML ch.</td>
<td>16 LVTTL/ channel</td>
<td>1 W</td>
<td>Four-channel version of TLK1501</td>
<td>Web</td>
</tr>
<tr>
<td>SN65LVDS93/94</td>
<td>Four-ch. 28:4 TX/RX chipset</td>
<td>140–455 Mbps/ch.</td>
<td>4 LVDS</td>
<td>28 × LVTTL</td>
<td>250 mW/ chip</td>
<td>Supports up to 1.82-Gbps throughput</td>
<td>Web</td>
</tr>
<tr>
<td>SN65LVDS95/96</td>
<td>Four-ch. 21.3 TX/RX chipset</td>
<td>140–455 Mbps/ch.</td>
<td>4 LVDS</td>
<td>28 × LVTTL</td>
<td>250 mW/ chip</td>
<td>Supports up to 1.3-Gbps throughput</td>
<td>Web</td>
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<tr>
<td>SN65LV1021/SN65LV1212</td>
<td>Single-ch. 10:1 TX/RX chipset</td>
<td>100–400 Mbps</td>
<td>1 LVDS</td>
<td>10 × LVTTL</td>
<td>&lt;400 mW/ total</td>
<td>Low-power solution</td>
<td>Web</td>
</tr>
<tr>
<td>SN65LV1023/SN65LV1224</td>
<td>Single-ch. 10:1 TX/RX chipset</td>
<td>300–660 Mbps</td>
<td>1 LVDS</td>
<td>10 × LVTTL</td>
<td>&lt;400 mW/ total</td>
<td>Low-power solution</td>
<td>Web</td>
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<tr>
<td>SLK2501/SLK2511</td>
<td>Single-ch. 4:1 multirate SONET xcvr with CDR</td>
<td>OC-3/12/24/48</td>
<td>1 LVPECL</td>
<td>4 × 622 LVDS</td>
<td>900 mW</td>
<td>Auto-rate detection, local and remote loop back</td>
<td>Web</td>
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<tr>
<td>SLK2701/SLK2721</td>
<td>Single-ch. 4:1 multirate SONET xcvr with CDR</td>
<td>OC-3/12/24/48</td>
<td>PECL</td>
<td>4 × LVDS</td>
<td>900 mW</td>
<td>FEC rate is compatible, SLK2721 is optimized for jitter tolerance</td>
<td>Web</td>
</tr>
</tbody>
</table>

1Please check www.ti.com for current pricing on these products.
## LVDS LINE DRIVERS AND RECEIVERS

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<th>Device</th>
<th>Max Drvr/Rcvr tp&lt;sub&gt;d&lt;/sub&gt; (ns)</th>
<th>Max Speed (Mbps)</th>
<th>Max Supply Current (mA)</th>
<th>HBM ESD Protection (kV)</th>
<th># Inputs</th>
<th># Outputs</th>
<th>Output Skew (ps)&lt;sup&gt;2&lt;/sup&gt;</th>
<th>Pulse Skew (ps)&lt;sup&gt;2&lt;/sup&gt;</th>
<th>Package Options</th>
<th>Comments</th>
<th>Price&lt;sup&gt;1&lt;/sup&gt;</th>
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<td>SN65LVDS1</td>
<td>3.1</td>
<td>630</td>
<td>8</td>
<td>15</td>
<td>1 LVTTL</td>
<td>1 LVDS</td>
<td>300 typ</td>
<td>300 max</td>
<td>5-pin SOT-23,</td>
<td>Single driver</td>
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<td>8-pin SOIC</td>
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<td>SN65LVDS2</td>
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<td>400</td>
<td>7</td>
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<td>1 LVTTL</td>
<td>600 max</td>
<td>200 typ</td>
<td>5-pin SOT-23,</td>
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<td>8-pin SOIC</td>
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<td>SN65LVDS22</td>
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<td>400</td>
<td>20</td>
<td>12</td>
<td>2 LVDS</td>
<td>2 LVDS</td>
<td>160 typ</td>
<td>200 typ</td>
<td>16-pin SOIC,</td>
<td>2.2 MUX (crosspoint)</td>
<td>3.01</td>
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<td>16-pin TSSOP</td>
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<td>8</td>
<td>4 LVTTL</td>
<td>4 LVDS</td>
<td>300 max</td>
<td>300 max</td>
<td>16-pin SOIC,</td>
<td>Quad driver</td>
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<tr>
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<td>3</td>
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<td>4 LVTTL</td>
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<td>4 LVTTL</td>
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<td>SN65LVDS047</td>
<td>2.8</td>
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<td>26</td>
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<td>4 LVDS</td>
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<td>10</td>
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<td>4 LVTTL</td>
<td>500 max</td>
<td>450 max</td>
<td>16-pin SOIC,</td>
<td>Quad receiver</td>
<td>1.83</td>
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<td>16-pin TSSOP</td>
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<td>SN65LVDS386&lt;sup&gt;3&lt;/sup&gt;</td>
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<td>4</td>
<td>16 LVDS</td>
<td>16 LVTTL</td>
<td>400 max</td>
<td>600 max</td>
<td>16-pin TSSOP</td>
<td>16-ch. receiver</td>
<td>5.55</td>
</tr>
<tr>
<td>SN65LVDS387</td>
<td>2.9</td>
<td>630</td>
<td>95</td>
<td>15</td>
<td>16 LVTTL</td>
<td>16 LVDS</td>
<td>150 max</td>
<td>500 max</td>
<td>16-pin TSSOP</td>
<td>16-ch. receiver</td>
<td>5.55</td>
</tr>
<tr>
<td>SN75LVDS388A&lt;sup&gt;3&lt;/sup&gt;</td>
<td>4</td>
<td>300</td>
<td>40</td>
<td>4</td>
<td>8 LVDS</td>
<td>8 LVTTL</td>
<td>400 max</td>
<td>600 max</td>
<td>38-pin TSSOP</td>
<td>Octal receiver</td>
<td>3.25</td>
</tr>
<tr>
<td>SN65LVDS389</td>
<td>2.9</td>
<td>300</td>
<td>70</td>
<td>4</td>
<td>8 LVTTL</td>
<td>8 LVDS</td>
<td>150 max</td>
<td>500 max</td>
<td>38-pin TSSOP</td>
<td>Octal driver</td>
<td>3.25</td>
</tr>
</tbody>
</table>

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.
<sup>2</sup>R<sub>L</sub> = 100 Ω, C<sub>L</sub> = 10 pF with max. spec.
<sup>3</sup>Integrated termination option.

## LVDS/LVPECL/CML REPEATERS/TRANSLATORS AND CROSSPOINTS

<table>
<thead>
<tr>
<th>Device</th>
<th>Max Drvr/Rcvr tp&lt;sub&gt;d&lt;/sub&gt; (ns)</th>
<th>Max Speed (Mbps)</th>
<th>Max Supply Current (mA)</th>
<th>HBM ESD Protection (kV)</th>
<th># Inputs</th>
<th># Outputs</th>
<th>Output Skew (ps)</th>
<th>Pulse Skew (ps)</th>
<th>Packaging</th>
<th>Comments</th>
<th>Price&lt;sup&gt;1&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN65LVDS100</td>
<td>0.9</td>
<td>2000</td>
<td>90</td>
<td>5</td>
<td>1 LVDS/CML/LVPECL</td>
<td>1 LVDS</td>
<td>50</td>
<td>8-pin SOIC, VSSOP</td>
<td>Translator/Repeater</td>
<td>2.52</td>
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<tr>
<td>SN65LVDS101</td>
<td>0.9</td>
<td>2000</td>
<td>90</td>
<td>5</td>
<td>1 LVDS/CML/LVPECL</td>
<td>1 LVPECL</td>
<td>50</td>
<td>8-pin SOIC, VSSOP</td>
<td>Translator/Repeater</td>
<td>2.52</td>
<td></td>
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<tr>
<td>SN65CML100</td>
<td>0.8</td>
<td>1500</td>
<td>30</td>
<td>5</td>
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<td>1 CML</td>
<td>50</td>
<td>8-pin SOIC, VSSOP</td>
<td>Translator/Repeater</td>
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<tr>
<td>SN65LVDS122</td>
<td>0.9</td>
<td>1500</td>
<td>100</td>
<td>4</td>
<td>2 LVDS/CML/LVPECL</td>
<td>2 LVDS</td>
<td>40</td>
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<td>2×2 Crosspoint</td>
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<tr>
<td>SN65LVCP22</td>
<td>0.8</td>
<td>1000</td>
<td>85</td>
<td>8</td>
<td>2 LVDS/CML/LVPECL</td>
<td>2 LVDS</td>
<td>20</td>
<td>16-pin SOIC, TSSOP</td>
<td>2×2 Crosspoint</td>
<td>3.89</td>
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<tr>
<td>SN65LVCP23</td>
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<td>2000</td>
<td>65</td>
<td>5</td>
<td>2 LVDS/CML/LVPECL</td>
<td>2 LVPECL</td>
<td>20</td>
<td>16-pin SOIC, TSSOP</td>
<td>2×2 Crosspoint</td>
<td>4.95</td>
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<tr>
<td>SN65LVDS125</td>
<td>1</td>
<td>1500</td>
<td>100</td>
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<td>4 LVDS/CML/LVPECL</td>
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<td>50</td>
<td>38-pin TSSOP</td>
<td>4×4 Crosspoint</td>
<td>8.70</td>
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</tr>
</tbody>
</table>

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.
## GTLP Transceivers

<table>
<thead>
<tr>
<th>Device</th>
<th>Description</th>
<th>Status</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74GTLP1394</td>
<td>2-bit LVTTL-to-GTLP adjustable-edge-rate bus Xcvr w/ split LVTTL port, feedback path, and selectable polarity</td>
<td>Active</td>
<td>2.73</td>
</tr>
<tr>
<td>SN74GTLP1395</td>
<td>Two 1-bit LVTTL/GTLP adjustable-edge-rate bus Xcvrs w/ split LVTTL port, feedback path, and selectable polarity</td>
<td>Active</td>
<td>1.75</td>
</tr>
<tr>
<td>SN74GTLP2033</td>
<td>8-bit LVTTL-GTLP adjustable-edge-rate registered transceiver with split LVTTL port and feedback path</td>
<td>Active</td>
<td>3.85</td>
</tr>
<tr>
<td>SN74GTLP2034</td>
<td>8-bit LVTTL-GTLP adjustable-edge-rate registered transceiver with split LVTTL port and feedback path</td>
<td>Active</td>
<td>3.85</td>
</tr>
<tr>
<td>SN74GTLP21395</td>
<td>Two 1-bit LVTTL/GTLP adjustable-edge-rate bus Xcvrs with split LVTTL port, feedback path, and selectable polarity</td>
<td>Active</td>
<td>1.75</td>
</tr>
<tr>
<td>SN74GTLP22033</td>
<td>8-bit LVTTL-GTLP adjustable-edge-rate registered transceiver with split LVTTL port and feedback path</td>
<td>Active</td>
<td>3.85</td>
</tr>
<tr>
<td>SN74GTLP22034</td>
<td>8-bit LVTTL-GTLP adjustable-edge-rate registered transceiver with split LVTTL port and feedback path</td>
<td>Active</td>
<td>3.85</td>
</tr>
<tr>
<td>SN74GTLPH1817</td>
<td>GTLP-to-LVTTL 1-to-6 fanout driver</td>
<td>Active</td>
<td>2.45</td>
</tr>
<tr>
<td>SN74GTLPH1612</td>
<td>18-bit LVTTL-GTLP adjustable-edge-rate universal bus transceiver</td>
<td>Active</td>
<td>5.95</td>
</tr>
<tr>
<td>SN74GTLPH1616</td>
<td>17-bit LVTTL-GTLP adjustable-edge-rate universal bus transceiver with buffered clock outputs</td>
<td>Active</td>
<td>5.95</td>
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<tr>
<td>SN74GTLPH1645</td>
<td>16-bit LVTTL-GTLP adjustable-edge-rate bus transceiver</td>
<td>Active</td>
<td>2.45</td>
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<tr>
<td>SN74GTLPH1655</td>
<td>16-bit LVTTL-GTLP adjustable-edge-rate universal bus transceiver</td>
<td>Active</td>
<td>4.90</td>
</tr>
<tr>
<td>SN74GTLPH16612</td>
<td>18-bit LVTTL-GTLP universal bus transceiver</td>
<td>Active</td>
<td>4.62</td>
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<tr>
<td>SN74GTLPH16812</td>
<td>18-bit LVTTL-GTLP universal bus transceiver</td>
<td>Active</td>
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<tr>
<td>SN74GTLPH16916</td>
<td>17-bit LVTTL-GTLP universal bus transceiver with buffered clock outputs</td>
<td>Active</td>
<td>4.90</td>
</tr>
<tr>
<td>SN74GTLPH16945</td>
<td>16-bit LVTTL-GTLP bus transceiver</td>
<td>Active</td>
<td>2.10</td>
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<tr>
<td>SN74GTLPH306</td>
<td>8-bit LVTTL-GTLP bus transceiver</td>
<td>Active</td>
<td>3.08</td>
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<tr>
<td>SN74GTLPH3245</td>
<td>32-bit LVTTL-GTLP adjustable-edge-rate bus transceiver</td>
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<td>3.71</td>
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<tr>
<td>SN74GTLPH32912</td>
<td>36-bit LVTTL-GTLP universal bus transceiver</td>
<td>Active</td>
<td>7.00</td>
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<tr>
<td>SN74GTLPH32945</td>
<td>32-bit LVTTL-GTLP bus transceiver</td>
<td>Active</td>
<td>3.15</td>
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1Suggested resale price in U.S. dollars in quantities of 1,000.

## M-LVDS Transceivers

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Description</th>
<th>No. of Tx</th>
<th>No. of Rx</th>
<th>Input Signal</th>
<th>Output Signal</th>
<th>RX Type</th>
<th>TX Skew</th>
<th>Part-to-Part Skew (ps)</th>
<th>Signal Rate Mbps</th>
<th>Rx tpd</th>
<th>Icc (mA)</th>
<th>ESD (HBM) (kV)</th>
<th>Supply Voltage (V)</th>
<th>Pin/Package</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN65MLV200</td>
<td>Half-duplex M-LVDS xcvr</td>
<td>1</td>
<td>1</td>
<td>LVTTL, M-LVDS</td>
<td>LVTTL, M-LVDS</td>
<td>1</td>
<td>2500</td>
<td>100</td>
<td>2.3</td>
<td>4.6</td>
<td>26</td>
<td>3</td>
<td>3.3</td>
<td>8-pin SOP</td>
<td>1.84</td>
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<tr>
<td>SN65MLV201</td>
<td>Half-duplex M-LVDS xcvr</td>
<td>1</td>
<td>1</td>
<td>LVTTL, M-LVDS</td>
<td>LVTTL, M-LVDS</td>
<td>1</td>
<td>1000</td>
<td>200</td>
<td>1.5</td>
<td>4.0</td>
<td>24</td>
<td>3</td>
<td>3.3</td>
<td>8-pin SOP</td>
<td>2.10</td>
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<tr>
<td>SN65MLV202</td>
<td>Full-duplex M-LVDS xcvr</td>
<td>1</td>
<td>1</td>
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<td>LVTTL, M-LVDS</td>
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<td>2500</td>
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<td>2.3</td>
<td>4.6</td>
<td>26</td>
<td>3</td>
<td>3.3</td>
<td>14-pin SOP</td>
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<tr>
<td>SN65MLV203</td>
<td>Full-duplex M-LVDS xcvr</td>
<td>1</td>
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<td>LVTTL, M-LVDS</td>
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<td>1000</td>
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<td>1.5</td>
<td>4.0</td>
<td>24</td>
<td>3</td>
<td>3.3</td>
<td>14-pin SOP</td>
<td>2.10</td>
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<tr>
<td>SN65MLV204</td>
<td>Half-duplex M-LVDS xcvr</td>
<td>1</td>
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<td>2500</td>
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<td>2.3</td>
<td>4.6</td>
<td>26</td>
<td>3</td>
<td>3.3</td>
<td>8-pin SOP</td>
<td>1.84</td>
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<tr>
<td>SN65MLV205</td>
<td>Full-duplex M-LVDS xcvr</td>
<td>1</td>
<td>1</td>
<td>LVTTL, M-LVDS</td>
<td>LVTTL, M-LVDS</td>
<td>1</td>
<td>2500</td>
<td>100</td>
<td>2.3</td>
<td>4.6</td>
<td>26</td>
<td>3</td>
<td>3.3</td>
<td>14-pin SOP</td>
<td>1.84</td>
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<tr>
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<td>Half-duplex M-LVDS xcvr</td>
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<td>1</td>
<td>LVTTL, M-LVDS</td>
<td>LVTTL, M-LVDS</td>
<td>2</td>
<td>1000</td>
<td>200</td>
<td>1.5</td>
<td>4.0</td>
<td>24</td>
<td>3</td>
<td>3.3</td>
<td>8-pin SOP</td>
<td>2.10</td>
</tr>
<tr>
<td>SN65MLV207</td>
<td>Full-duplex M-LVDS xcvr</td>
<td>1</td>
<td>1</td>
<td>LVTTL, M-LVDS</td>
<td>LVTTL, M-LVDS</td>
<td>2</td>
<td>1000</td>
<td>200</td>
<td>1.5</td>
<td>4.0</td>
<td>24</td>
<td>3</td>
<td>3.3</td>
<td>14-pin SOP</td>
<td>2.10</td>
</tr>
<tr>
<td>SN65MLV080</td>
<td>Half-duplex M-LVDS xcvr</td>
<td>8</td>
<td>8</td>
<td>LVTTL, M-LVDS</td>
<td>LVTTL, M-LVDS</td>
<td>1</td>
<td>600</td>
<td>250</td>
<td>1.5</td>
<td>4</td>
<td>180</td>
<td>8</td>
<td>3.3</td>
<td>64-pin TSSOP</td>
<td>4.50</td>
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<td>SN65MLV082</td>
<td>Half-duplex M-LVDS xcvr</td>
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<td>8</td>
<td>LVTTL, M-LVDS</td>
<td>LVTTL, M-LVDS</td>
<td>2</td>
<td>600</td>
<td>250</td>
<td>1.5</td>
<td>4</td>
<td>180</td>
<td>8</td>
<td>3.3</td>
<td>64-pin TSSOP</td>
<td>4.50</td>
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</tbody>
</table>

1Suggested resale unit price in U.S. dollars in quantities of 1,000. Please check www.ti.com for current pricing on these products.
## CLOCK DISTRIBUTION CIRCUITS

<table>
<thead>
<tr>
<th>Device</th>
<th>Description</th>
<th>Package Options</th>
<th>I/O Levels (Input/Output)</th>
<th>Frequency (MHz)</th>
<th>VCC (V)</th>
<th>Output Skew tsk(o) max (ns)</th>
<th>Price</th>
</tr>
</thead>
</table>
| **Buffer-Based Clock Distribution**
| CDCVF111 | 1:9 diff LVPECL | 28-pin PLCC | LVPECL/LVPECL | 0–650 | 3.3 | 0.05 | Web |
| CDC318A | 1:8 clock driver with IO control interface | 48-pin SSOP | LVTTI/LVTTI, TTL | 0–100 | 3.3 | 0.25 | Web |
| CDC341 | 1:8 w/ fast tf fanout | 20-pin SOIC | TTL/TTL | 0–80 | 5 | 0.6 | Web |
| CDC351/2351 | 1:10 w/ fast tf fanout, 3-state outputs | 24-pin SOIC/SSOP | LVTTIL/LVTTIL | 0–100 | 3.3 | 0.5 | Web |
| CDC391 | 1:8 clock driver with selectable polarity and 3-state outputs | 16-pin SOIC | TTL/TTL | 0–100 | 5 | 0.5 | Web |
| CDCLD110 | 1:10 programmable low-voltage LVDS clock driver | 32/TQFP | LVDS/LVDS | 900 | 2.5 | 30 ps typ | Web |
| CDCLP110 | 1:10 low-voltage LVPECL HSTL with selectable input clock driver | 32/LQFP | LVPECL or HSTL/LVPECL | 3.5 GHz | 2.5/3.3 | 30 ps | Web |
| CDCV304 | 1:4 fanout for PCI-X and general apps. | 8-pin TSSOP | LVTTI/CMOS | 0–140 | 3.3 | 0.17 | Web |
| CDCVF2310 | 1:10 clock driver w/ 2 banks for general-purpose applications | 24-pin TSSOP | LVTTI/LVTTI | 0–170 (VCC=2.3–2.7 V) | 2.5/3.3 | 170 ps @ 2.5 V | Web |
| CDCM1804 | 1:3 LVPECL clock buffer and addl. LVCMOS output and programmable divider | 24/MLF | LVPECL/ LVPECL or LVCMOS | to 800 MHz for LVPECL to 200 MHz for LVCMOS | 3.3 | – | Web |
| SN65LVDS104 | 1:4 diff LVDS | 16-pin SOIC/TSSOP | LVDS/LVDS | 0–315 | 3.3 | 0.1 | 2.22 |
| SN65LVDS105 | 1:4 diff LVDS | 16-pin SOIC/TSSOP | LVDS/LVDS | 0–315 | 3.3 | 0.1 | 2.22 |
| KN65LVDS108 | 1:8 diff LVDS | 38-pin TSSOP | LVDS/LVDS | 0–311 | 3.3 | 0.3 | 4.55 |
| SN65LVDS116 | 1:8 LVDS | 64-pin TSSOP | LVDS/LVDS | 0–311 | 3.3 | 0.3 | 5.97 |
| **PLL-Based Clock Distribution**
| CDC516/25162 | 1:16 PLL clock driver | 48-pin TSSOP | LVTTI/LVTTI | 25–125 | 3.3 | 0.2 | Web |
| CDC536/25362 | 1:6 PLL clock driver w/ (3) at 1/2× or 2× output, 3-state outputs | 28-pin SSOP | LVTTI/LVTTI | 25–100 | 3.3 | 0.5 | Web |
| CDC582/25822 | 1:12 LV diff PECL PLL clock driver w/ (9) at 1/2× or 2× output, 3-state outputs | 52-pin TQFP | LVPECL/LVTTI | 25–100 | 3.3 | 0.5 | Web |
| CDC586/25862 | 1:12 PLL clock driver w/ (9) at 1/2× or 2× output, 3-state outputs | 52-pin TQFP | LVTTI/LVTTI | 25–100 | 3.3 | 0.5 | Web |
| CDC5801 | Clock multiplier/divider w/ programmable delay and phase alignment | 24/SSOP | LVTTI/ LVPECL or LVDS or LVTTI | 150–500 / 12.5–62.5 | 3.3 | – | Web |
| CDC7005 | High-performance clock synthesizer | 64/BGA | LVTTI/LVPECL | 10–650 | 3.3 | 200 ps | Web |
| CDC5801 | Multiplier/divider with programmable delay and phase alignment | 24/SSOP | LVCMOS/ LVPECL or LVDS or LVTTI | 12.5 to 240 / 25 to 280 | 3.3 | – | Web |
| CDCVF2505 | 1:5 PLL clock driver for general purpose, SSC | 8-pin TSSOP/SSOP | LVTTI/LVTTI | 24–200 | 3.3 | 0.15 | Web |
| CDCVF2508 | 1:8 low-power PLL clock driver with two banks, SSC | 16-pin TSSOP/SSOP | LVTTI/LVTTI | 10–170 | 2.5/3.3 | 0.15 | Web |
| CDCVF25084 | 1:8 low-power 4´ multiplier with two banks, SSC | 16-pin TSSOP | LVTTI/LVTTI | 10 to 180 | 3.3 | 150 | Web |
| CDCVF2509 | 1:19 low-power PLL clock driver for PC 133 and beyond application, SSC | 24-pin TSSOP | LVTTI/LVTTI | 50–175 | 3.3 | 0.1 | Web |
| CDCVF2510 | 1:10 low-power PLL clock driver for PC 133 and beyond application, SSC | 24-pin TSSOP | LVTTI/LVTTI | 50–175 | 3.3 | 0.1 | Web |
| **PLL-Based Clocks for Memory Applications**
| CDC950 | 1:10 PLL clock driver for DDR SDRAM application, SSC compatible with two-line serial interface | 48-pin TSSOP | HCSL, Universal (except ECL)/SSTL-II | 60–140 | 2.5/3.3 | 0.075 | Web |
| CDC955 | 1:4 (plus feedback pair) PLL differential clock driver for DDR applications, SSC | 28-pin TSSOP | SSTL-II/ SSTL-II, LVTTI | 60–180 | 2.5 | 0.75 | Web |
| CDC957B | 1:10 PLL differential clock driver for DDR applications, SSC | 48-pin TSSOP | SSTL-II/SSTL-II | 60–200 | 2.5 | 0.75 | Web |

1. Suggested resale price in U.S. dollars in quantities of 1,000. Please check www.ti.com for current pricing on these products. Preview devices are listed in blue.

2. With series output resistors.

Notes: For more information regarding test conditions used to obtain measurements, see datasheet. Converted from V/ns datasheet value to ns value, based on 0.4- to 2-V voltage rise/fall.
LOGIC

As wireless infrastructure designers look to increase data throughput, reduce power consumption, and shrink form factors, TI’s logic portfolio is constantly advancing while, at the same time, the company is dedicated to providing legacy logic devices.

As the leading provider of logic, TI’s latest technologies are targeted for the fast moving market of wireless infrastructure systems. Advanced CMOS families and functions, like the LVC and ALVC are optimized at 3.3-V \( V_{CC} \). And the CBT and CBTLV families of bus switches offer designers a broad portfolio to meet diverse switching needs.

Logic Product Life Cycle
16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS
SN74ALVC16244A/SN74LVC16244A

Get samples and datasheets at:
www.ti.com/sc/device/partnumber
Replace partnumber in the URL with sn74alvc16244a or sn74lvc16244a

Ideal for base station and networking applications, both the LVC and ALVC families of logic technologies offer solutions for speed-critical 3.3-V system designs. The LVC family is a high-performance version with 0.8-µ CMOS process technology. With typical propagation delays of less than 2 ns, ALVC provides 24 mA of current drive and static power consumption.

Key Features:
- 3.6-ns max $t_{pd}$ at 3.3 V (ALVC)
- 5.2-ns max $t_{pd}$ at 3.3 V (LVC)
- $I_{off}$ circuitry (LVC)
- Packaging: BGA

### ALVC PARAMETRICS

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>SN74ALVC16244A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage nodes (V)</td>
<td>3.3, 2.7, 2.5, 1.8</td>
</tr>
<tr>
<td>$V_{CC}$ range (V)</td>
<td>2.3 to 3.6</td>
</tr>
<tr>
<td>Input level</td>
<td>LVTTL</td>
</tr>
<tr>
<td>Output level</td>
<td>LVTTL</td>
</tr>
<tr>
<td>Output drive (mA)</td>
<td>-24/24</td>
</tr>
<tr>
<td>$t_{pd}$ max (ns)</td>
<td>3.6</td>
</tr>
<tr>
<td>Static current</td>
<td>0.04</td>
</tr>
</tbody>
</table>

### LOW-VOLTAGE QUADRUPLE-FET BUS SWITCH
SN74CBTLV3125

Get samples and datasheets at:
www.ti.com/sc/device/sn74cbtlv3125

The CBTLV family of bus switches operate at the low-voltage 3.3-V operating node. These high-speed bus-connect devices benefit designs with greater system speed and reduced power consumption. The SN74CBTLV3125 quadruple-FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is high.

Key Features:
- Standard SN74CBTLV3125-type pinout
- 5-Ω switch connection between two ports
- Isolation under power-off conditions
- Latch-up performance exceeds 100 mA per JESD 78, Class II

Applications:
- Base stations
- Networking

### CBTLV3125 PARAMETERS

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>SN74CBTLV3125</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage nodes (V)</td>
<td>3.3, 2.5</td>
</tr>
<tr>
<td>$V_{CC}$ range (V)</td>
<td>2.3 to 3.6</td>
</tr>
<tr>
<td>No. of bits</td>
<td>4</td>
</tr>
<tr>
<td>$r_{on}$ max (ohms)</td>
<td>7</td>
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<tr>
<td>$t_{pd}$ max (ns)</td>
<td>0.25</td>
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## SN74CBLTV31x BUS SWITCHES

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Package</th>
<th>Pins</th>
<th>Temp (°C)</th>
<th>Status</th>
<th>Pack Quantity</th>
<th>Price&lt;sup&gt;1&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74CBLTV31250</td>
<td>D</td>
<td>14</td>
<td>-40 to 85</td>
<td>Active</td>
<td>50</td>
<td>0.81</td>
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<tr>
<td>SN74CBLTV31250BQR</td>
<td>DGG</td>
<td>16</td>
<td>-40 to 85</td>
<td>Active</td>
<td>2500</td>
<td>0.81</td>
</tr>
<tr>
<td>SN74CBLTV31250GVR</td>
<td>DGV</td>
<td>14</td>
<td>-40 to 85</td>
<td>Active</td>
<td>2000</td>
<td>0.81</td>
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<tr>
<td>SN74CBLTV31250DR</td>
<td>D</td>
<td>14</td>
<td>-40 to 85</td>
<td>Active</td>
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<td>0.81</td>
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<tr>
<td>SN74CBLTV3125NSR</td>
<td>NS</td>
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<td>-40 to 85</td>
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<td>0.81</td>
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<tr>
<td>SN74CBLTV3125PWR</td>
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<sup>1</sup>Suggested resale price in U.S. dollars.

## ALVC BUFFER/DRIVERS

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Package</th>
<th>Pins</th>
<th>Temp (°C)</th>
<th>Status</th>
<th>Pack Quantity</th>
<th>Price&lt;sup&gt;1&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74ALVC16244ADGG</td>
<td>DGG</td>
<td>48</td>
<td>-40 to 85</td>
<td>Active</td>
<td>2000</td>
<td>1.12</td>
</tr>
<tr>
<td>SN74ALVC16244ADG</td>
<td>DL</td>
<td>48</td>
<td>-40 to 85</td>
<td>Active</td>
<td>25</td>
<td>1.12</td>
</tr>
<tr>
<td>SN74ALVC16244ADLR</td>
<td>DL</td>
<td>48</td>
<td>-40 to 85</td>
<td>Active</td>
<td>1000</td>
<td>1.12</td>
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<tr>
<td>SN74ALVC16244AGQLR</td>
<td>GQL</td>
<td>56</td>
<td>-40 to 85</td>
<td>Active</td>
<td>1000</td>
<td>1.23</td>
</tr>
</tbody>
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<sup>1</sup>Suggested resale price in U.S. dollars.

## LVC PRODUCTS

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Package</th>
<th>Pins</th>
<th>Temp (°C)</th>
<th>Status</th>
<th>Pack Quantity</th>
<th>Price&lt;sup&gt;1&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74LVC16244ADG</td>
<td>DGG</td>
<td>48</td>
<td>-40 to 85</td>
<td>Active</td>
<td>2000</td>
<td>1.01</td>
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<tr>
<td>SN74LVC16244ADGV</td>
<td>DGV</td>
<td>48</td>
<td>-40 to 85</td>
<td>Active</td>
<td>2000</td>
<td>1.01</td>
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<tr>
<td>SN74LVC16244ADL</td>
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<td>-40 to 85</td>
<td>Active</td>
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<td>1.01</td>
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<tr>
<td>SN74LVC16244ADLR</td>
<td>DL</td>
<td>48</td>
<td>-40 to 85</td>
<td>Active</td>
<td>1000</td>
<td>1.01</td>
</tr>
<tr>
<td>SN74LVC16244AGQLR</td>
<td>GQL</td>
<td>56</td>
<td>-40 to 85</td>
<td>Active</td>
<td>1000</td>
<td>1.12</td>
</tr>
</tbody>
</table>

<sup>1</sup>Suggested resale price in U.S. dollars.
Wireless infrastructure (WI) systems require that designers consider a wide range of power management technology. From discrete devices to modular approaches, WI designers must select technology that addresses the technical challenge of the system and offers ancillary benefits in terms of ease-of-use and supply chain reliability and efficiency.

Much of TI's broad range of power management products has been targeted at wireless infrastructure applications. Based on extensive experience with power technology, TI's solutions address application challenges that designers face daily. With solutions for both portable and board power applications, TI has a comprehensive array of power management solutions. In addition, its market-proven record of expertise has made TI's power technology very easy to use for designers. A wide range of both discrete devices and isolated and non-isolated modular power technology is available.

Some of the products specific to wireless infrastructure applications include the following:

- **DC/DC Controllers and Converters**: These devices will generate regulated supply rails. The TPS54xxx (SWIFT™) family of converters integrates the output FETs to simplify design and the family provides output currents up to 9 A. New controllers, such as the TPS40K™ series, are ideal for a broader range of input voltages and output currents.

- **Isolated Plug-In Modules**: A number of products are specifically designed for 48-V bus applications. Many devices feature multiple channels for improved integration and lower system cost.

- **Non-Isolated Plug-In Modules**: Modules specifically designed for point-of-load applications come in high-performance packaging. A broad range of voltage and current options make these devices ideal for wireless infrastructure systems.

- **Hot Swap Power Managers**: New TPS2490, TPS2491 and TPS2350 hot swap devices are specifically designed for the 48-V bus used in infrastructure systems. These new devices add to the family of TPS239x hot swap devices.

- **MOSFET Gate Drivers**: A powerful family of gate driver ICs, featuring a combined bipolar and MOSFET manufacturing process, delivering fast switching transitions and high current output capability.

- **PWM Controllers and Special Functions**: The industry's largest selection of controllers and an extensive selection of support ICs facilitate the efficient design of discrete power supplies.

- **Linear Regulators**: For the lowest-cost power solution, a broad range of LDOs support currents ranging from 10 mA to 7 A.
**POINT-OF-LOAD POWER MODULES OFFER AUTO-TRACK™ SEQUENCING**

**PTH Series of Point-of-Load Modules**

Get samples and datasheets at: www.ti.com/sc/device/part number

Replace part number in the URL with pthxx000, pthxx050, pthxx060, pthxx010, pthxx020, pthxx030

where xx = input voltage = 03, 05, or 12

The PTHxx series of plug-in power modules will support step-down DC/DC conversion from a 3.3 V, 5 V or 12 V input with adjustable output voltages from 0.8 V to 5.5 V at output currents up to 30 A. The power modules incorporate an innovative new Auto-Track sequencing technology, which allows multiple modules to be powered up and down in sequence without external circuitry.

**Key Features:**
- Auto-Track sequencing
- Margin-up/down controls
- Pre-bias startup capability
- Output current up to 30 A
- Efficiencies up to 96%
- Point-of-Load Alliance (POLA) compatible
- Packaging: Low-profile DIP module

**75-W/100-W CONVERTERS OFFER 90% EFFICIENCY**

**PT4410**

Get samples and datasheets at: www.ti.com/sc/device/pt4410

The PT4410 series of power modules are single-output isolated DC/DC converters housed in a compact 21-pin low-profile (12-mm) package. These modules are rated up to 75 W with load currents as high as 30 A. The output voltage is set within a predefined range via a 5-bit input code and is adjustable.

**Key Features:**
- 90% efficiency
- Output power: 75 W or 100 W
- 36-V to 75-V input
- 5-bit programmable output voltage
- 1500-V DC isolation
- On/off control
- Over-current protection
- Differential remote sense
- Output over-voltage protection
- Over-temperature shutdown
- Under-voltage lockout
- Space-saving solderable copper case
- Packaging: Low profile, 12 mm

---

**Applications:**
- Wireless infrastructure
- Telecom
- Networking

---

**Applications:**
- Wireless infrastructure
- Telecom
- Networking
TRIPLE-OUTPUT MODULES FEATURE 50% SMALLER FOOTPRINT PLUS SEQUENCING
TP4820/PT4850

Get samples and datasheets at:
www.ti.com/sc/device/partnumber
Replace partnumber in the URL with pt4820 or pt4850

The TP4820 and PT4850 Excalibur™ power modules are a series of isolated triple-output DC/DC converters that operate from a standard (-48 V) central office supply. These modules are rated for a combined output of up to 12 A or 25 A and are designed for powering mixed-logic applications. Output voltage options include a low-voltage output for a DSP or ASIC core and two additional supply voltages for the I/O and other functions.

Key Features:
- Three independently regulated outputs
- Internal power-up and power-down sequencing
- Output power: 35 W or 75 W
- Input voltage range: 36 V to 75 V
- 1500-V DC isolation
- Dual logic-on/off control
- Short-circuit protection (all outputs)
- Over-temperature shutdown

-48 V, 8-PIN, HOT SWAP CONTROLLERS
TPS2390/TPS2391

Get samples and datasheets at:
www.ti.com/sc/device/partnumber
Replace partnumber in the URL with tps2390 or tps2391

The TPS2390 and TPS2391 Hot Swap power managers are optimized for use in nominal -48 V systems. Designed for supply voltage ranges up to -80 V, they are rated to withstand spikes to -100 V. In conjunction with an external N-channel FET and sense resistor, these controllers can be used to enable the live insertion of plug-in cards and modules in powered systems.

Key Features:
- Wide input supply range: -36 V to -80 V
- Transient rating to -100 V
- Programmable current limit and current slew rate
- Enable input (EN)
- Fault timer to eliminate nuisance trips
- Open-drain fault output
- Requires few external components
- Packaging: 8-pin MSOP

Applications:
- Wireless infrastructure
- Telecom
- Networking

PT4820/50 Block Diagram

TPS2390/91 Block Diagram

<table>
<thead>
<tr>
<th>Device</th>
<th>Auto-Retry</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS2350</td>
<td>Yes</td>
<td>PG</td>
</tr>
<tr>
<td>TPS2390</td>
<td>No</td>
<td>Fault</td>
</tr>
<tr>
<td>TPS2391</td>
<td>Yes</td>
<td>Fault</td>
</tr>
<tr>
<td>TPS2392</td>
<td>No</td>
<td>PG/Fault</td>
</tr>
<tr>
<td>TPS2393</td>
<td>Yes</td>
<td>PG/Fault</td>
</tr>
<tr>
<td>TPS2398</td>
<td>No</td>
<td>PG</td>
</tr>
<tr>
<td>TPS2399</td>
<td>Yes</td>
<td>PG</td>
</tr>
<tr>
<td>TPS2490</td>
<td>No</td>
<td>PG</td>
</tr>
<tr>
<td>TPS2491</td>
<td>Yes</td>
<td>PG</td>
</tr>
</tbody>
</table>
**TPS4000x Block Diagram**

Applications:
- Wireless infrastructure
- Networking equipment
- Telecom equipment
- Base stations
- DSP power

**HIGH-EFFICIENCY SYNCHRONOUS BUCK DC/DC CONTROLLERS**

**TPS4000x**

Get samples and datasheets at: power.ti.com

The TPS4000x are controllers for low-voltage, non-isolated synchronous buck regulators and drive N-channel power MOSFETs. They control the delays from main switch-off to rectifier turn-on and from rectifier turn-off to main switch turn-on, minimizing diode losses (both conduction and recovery) in the synchronous rectifier with TI’s proprietary Predictive Gate Drive™ technology.

**Key Features:**
- Input voltage range: 2.25 V to 5.5 V
- Output voltage as low as 0.7 V
- 1% internal 0.7-V reference
- Predictive Gate Drive N-channel MOSFET drivers for higher efficiency
- Externally adjustable soft-start and overcurrent limit
- Fixed-frequency, 300-kHz or 600-kHz voltage-mode control
- Packaging: 10-lead MSOP PowerPAD™ for higher performance

**TPS54916 Block Diagram**

**SYNCHRONOUS BUCK DC/DC CONVERTERS WITH INTEGRATED MOSFETS**

**TPS54916**

For datasheets, samples, app notes, EVMs, and software, go to: power.ti.com/swift

**Key Features:**
- Input voltage range: 3.0 V to 6.0 V
- Internal MOSFET switches for high efficiency at full load output current
- Adjustable output voltage range down to 0.9 V with 1.0% accuracy
- Wide PWM frequency: Fixed 350 kHz, 550 kHz, or adjustable 280 kHz to 700 kHz
- Load protected by peak current limit and thermal shutdown
- PowerGood, enable, and slow-start
- Reduces board area and component count
- Packaging: 28-pin HTSSOP

**Applications:**
- Low-voltage, high-density distributed power
- Point-of-load regulation for high-performance DSPs, FPGAs, ASICs, and microprocessors
- Broadband, networking, and optical communications infrastructure

---

<table>
<thead>
<tr>
<th>Part Number</th>
<th>I_{OUT} (A)</th>
<th>V_{IN} (V)</th>
<th>V_{OUT} (V)</th>
<th>Price¹</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS54910</td>
<td>9</td>
<td>3–4</td>
<td>Adj. to 0.9 V</td>
<td>5.20</td>
<td></td>
</tr>
<tr>
<td>TPS54810</td>
<td>8</td>
<td>4–6</td>
<td>Adj to 0.9 V</td>
<td>4.90</td>
<td></td>
</tr>
<tr>
<td>TPS5461x</td>
<td>6</td>
<td>3–6</td>
<td>0.9, 1.2, 1.5, 1.8, 2.5, 3.3 V adj.</td>
<td>4.65</td>
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<tr>
<td>TPS5431x*</td>
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<td>3–6</td>
<td>0.9, 1.2, 1.5, 1.8, 2.5, 3.3 V adj.</td>
<td>3.45</td>
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</table>

*20-pin HTSSOP package

¹Suggested resale price in U.S. dollars in quantities of 1,000.
TRACKING SWITCHER WITH INTEGRATED FETS FOR SEQUENCING
TPS54680

Get datasheets, EVMs, samples, application notes, and software tools at:
www.ti.com/sc/device/tps54680

System designers must consider the timing and voltage differences between core and I/O power supplies (i.e., power supply sequencing) during power up and power down. The TPS54680 solution easily accomplishes simultaneous power-up and power-down without the need of additional complex sequencing circuitry.

Key Features:
• Power-up/down tracking
• Input voltage range: 3.0 V to 6.0 V
• Internal 30-mΩ, 12-A peak MOSFET switches for high efficiency at 6-A continuous output
• Switching frequency fixed at 350 kHz or adjustable from 280 kHz to 700 kHz
• PowerGood and enable functions
• Load protected by peak current limit and thermal shutdown
• Packaging: 28-pin HTSSOP PowerPAD™

95% EFFICIENT, 600-mA, STEP-DOWN CONVERTERS
TPS6200x

Get datasheets and samples at:
www.ti.com/sc/device/partnumber
Replace partnumber in URL with tps62000, tps62001, tps62002, tps62003, tps62004, tps62005, tps62006, tps62007, or tps62008

The TPS6200x high-efficiency, synchronous step-down converters are ideal for high-efficiency power conversion in sub-systems with input voltages between 2.0 V and 5.5 V.

Key Features:
• 2.0-V to 6.0-V input voltage range
• Adjustable-output voltage range from 0.8 V to \( V_I \)
• Fixed-output voltage options available
• Up to 600-mA output current
• Synchronizable to external clock signal up to 1 MHz
• Highest efficiency over wide-load current range due to PFM powersave mode
• 50-µA quiescent current (typ)
• Packaging: 3 × 5 mm² MSOP-10

Applications:
• DSPs, FPGAs, ASICs, and microprocessors that require simultaneous start up
• Broadband, datacom, and optical communications infrastructure
• Precision point-of-load regulation
UCC27323 Block Diagram

Applications:
- Switch-mode power supplies:
  - Off-line power supplies
  - DC/DC converters
  - Board mount power supplies

DUAL, 4-AMP, MOSFET GATE DRIVER
UCC27323

Get samples and datasheets at:
www.ti.com/sc/device/ucc27323

The UCC27323/4/5 family of high-speed dual-MOSFET drivers can deliver large peak currents into capacitive loads, typical of a power MOSFET gate. Three standard logic options are offered – dual-inverting, dual-noninverting, and one inverting and one non-inverting driver.

Key Features:
- High current drive capability of ±4 A at the Miller Plateau region
- Industry-standard pin-out
- Efficient constant-current sourcing using a unique bipolar and CMOS output stage
- TTL-/CMOS-compatible inputs independent of supply voltage
- 4-V to 15-V supply voltage
- Packaging: Thermally enhanced MSOP PowerPAD™ with 4.7 C/W $\theta_{jc}$

UCC29002 Typical Low-Side Current-Sensing Application

System Configurations:
- Modules with remote sense capability
- Modules with adjust input
- Modules with both remote sense and adjust input
- In conjunction with the internal feedback E/A of OEM power supply units

Applications:
- Paralleled solution for DC/DC distribution
  - Redundant power supplies
  - SMPS for (web) servers
  - Server, workstation, and telecom systems

LOADSHARE CONTROLLER FOR PARALLEL POWER SUPPLIES
UCC29002

Get samples and datasheets at:
www.ti.com/sc/device/ucc29002

The UCC29002 is an advanced, high-performance, low-cost LoadShare controller that provides all necessary functions to parallel multiple independent power supplies or DC-to-DC modules. Targeted for high-reliability applications in telecom distributed-power systems, the controller is suitable for N+1 redundant systems or high-current applications where off-the-shelf power supplies need to be paralleled.

Key Features:
- High accuracy, better than 1% current share error at full load
- High-side or low-side (GND reference) current-sense capability
- Ultra-low offset current-sense amplifier
- Single-wire LoadShare bus
- Full scale adjustability
- Intel® SSI LoadShare specification compliant
- Disconnect from LoadShare bus at stand-by
- LoadShare bus protection against shorts to GND or to the supply rail
- Packaging: 8-pin MSOP minimizes space
- Lead-free assembly
LOW-INPUT-VOLTAGE, OUTPUT-CAP-FREE, 1-A LDOS FOR SIMPLE, HIGHLY EFFICIENT REGULATION

TPS725xx/TPS726xx

Get samples, datasheets, and EVMs at: power.ti.com

The TPS725xx/726xx families of Low-Dropout Regulators (LDOs) help you achieve as high as 83% efficiency with the low-input-voltage feature, rivaling a switch-mode solution. These devices offer simplicity, minimized component count, and low-noise performance in post-regulation applications, as shown in the diagram.

Key Features:
- Supports input voltages as low as 1.8 V (and up to 5.5 V), allowing up to 83% efficiency
- No output capacitor required for stability
- 1-A LDO with integrated SVS (50-ms delay), TPS725xx
- 1-A LDO with integrated SVS (200-ms delay), TPS726xx
- 1.5-/1.6-/1.8-/2.5-V fixed-output, and adjustable-output versions available
- Dropout voltage typically 170 mV at 1 A
- Less than 1-µA quiescent current in shutdown mode
- Packaging: SOT-223-5, DDPAK

ULTRA-LOW-NOISE, HIGH-PSRR, FAST-RF LDO IN SOT-23

TPS791xx/TPS792xx/TPS793xx/TPS794xx/TPS795xx/TPS796xx/TPS786xx

Get samples, datasheets, and EVMs at: power.ti.com

The TPS79xxx family of Low-Dropout Regulators (LDOs) features extremely high PSRR and ultra-low-noise performance to support noise-sensitive applications such as powering RF amplifiers.

Key Features:
- Output current: 100 mA to 1.5 A (see table at right)
- Input voltage: 2.7 V to 5.5 V
- Output capacitor: 1.0-µF or 2.2-µF ceramic
- High PSRR: 70 dB at 10 kHz
- Ultra-low noise: 15 µVRMS (TPS791xx)
- Fast start time: 50 µs (TPS792xx)
- Dropout voltage: 38 mV at 100 mA (TPS791xx)
- Packaging: SOT-23-5, MSOP-8, SOT-223-5, DDPAK

Applications:
- RF
- VCOs
- DSP/FPGA/ASIC/microprocessor supplies

Applications:
- Post-regulation of switch-mode supplies
- Powering core voltages of DSPs, FPGAs, ASICs, and microprocessors

TPS725xx Application Diagram

TP791xx PSRR Performance

<table>
<thead>
<tr>
<th>Device (^1)</th>
<th>I(_0) (mA)</th>
<th>(V_{in}) (V)</th>
<th>Peak Current (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS791xx</td>
<td>100</td>
<td>1.8/2.5/3.0/3.3</td>
<td>285</td>
</tr>
<tr>
<td>TPS792xx</td>
<td>100</td>
<td>2.5/2.8/3.0/3.3</td>
<td>285</td>
</tr>
<tr>
<td>TPS793xx</td>
<td>200</td>
<td>2.5/2.8/3.0/3.3</td>
<td>285</td>
</tr>
<tr>
<td>TPS794xx</td>
<td>250</td>
<td>1.8/2.5/2.8/3.0</td>
<td>700</td>
</tr>
<tr>
<td>TPS795xx</td>
<td>500</td>
<td>1.8/2.5/2.8/3.0</td>
<td>2400</td>
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<tr>
<td>TPS796xx</td>
<td>1000</td>
<td>1.8/2.5/3.0/3.3</td>
<td>2400</td>
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<tr>
<td>TPS786xx</td>
<td>1500</td>
<td>1.8/2.5/2.8/3.0</td>
<td>2400</td>
</tr>
</tbody>
</table>

\(^1\)xx represents the 2 digits of output voltage.
## Wireless Infrastructure Solutions Guide

**DC/DC CONVERTERS (INTEGRATED SWITCH)**

<table>
<thead>
<tr>
<th>Device</th>
<th>Input Bus Voltage (V)</th>
<th>P&lt;sub&gt;OUT&lt;/sub&gt; or I&lt;sub&gt;LOUT&lt;/sub&gt;</th>
<th>Isolated Outputs</th>
<th>V&lt;sub&gt;D&lt;/sub&gt; Range (V)</th>
<th>V&lt;sub&gt;D&lt;/sub&gt; Adjustable</th>
<th>Price&lt;sup&gt;2&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Low Power Step Down (Buck) Converters — up to 1.2 A</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPS56220</td>
<td>3.3</td>
<td>15 A, 22 A, 30 A, 6 A, 10 A</td>
<td>No</td>
<td>0.8 to 2.5</td>
<td>Yes</td>
<td>14.00, 18.13, 24.63, 9.10, 11.20</td>
</tr>
<tr>
<td>TPS56021</td>
<td>5</td>
<td>15 A, 18 A, 26 A, 12 A, 8 A</td>
<td>No</td>
<td>0.8 to 3.6</td>
<td>Yes</td>
<td>14.00, 18.13, 24.63, 9.10, 11.20</td>
</tr>
<tr>
<td>TPS56010</td>
<td>12</td>
<td>18 A, 26 A, 8 A</td>
<td>No</td>
<td>1.2 to 5.5</td>
<td>Yes</td>
<td>14.00, 18.13, 24.63, 9.10, 11.20</td>
</tr>
</tbody>
</table>

<sup>1</sup>Disabled sinking during start-up.
<sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

**SWIFT™ Step Down (Buck) Converters — up to 9 A**

<table>
<thead>
<tr>
<th>Device</th>
<th>Input Bus Voltage (V)</th>
<th>P&lt;sub&gt;OUT&lt;/sub&gt; or I&lt;sub&gt;LOUT&lt;/sub&gt;</th>
<th>Isolated Outputs</th>
<th>V&lt;sub&gt;D&lt;/sub&gt; Range (V)</th>
<th>V&lt;sub&gt;D&lt;/sub&gt; Adjustable</th>
<th>Price&lt;sup&gt;2&lt;/sup&gt;</th>
</tr>
</thead>
</table>

<sup>1</sup>See power.ti.com for a complete product offering.
<sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.
# LOW DROPOUT REGULATORS (LDOs)

<table>
<thead>
<tr>
<th>Device</th>
<th>$I_D$ (mA)</th>
<th>$V_{OQ}$ @ $I_D$ (mV)</th>
<th>$I_{Q}$ (µA)</th>
<th>Out Voltage (V)</th>
<th>Adj.</th>
<th>Features 1</th>
<th>Comments</th>
<th>Price 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>UC3851xx</td>
<td>1000</td>
<td>3.3, 5.5</td>
<td>4</td>
<td>1.5, 1.8, 2.5</td>
<td>✔</td>
<td></td>
<td></td>
<td>0.25</td>
</tr>
<tr>
<td>UC3850xx</td>
<td>500</td>
<td>3.3, 5.5</td>
<td>2</td>
<td>1.5, 1.8, 2.5</td>
<td>✔</td>
<td></td>
<td></td>
<td>0.32</td>
</tr>
<tr>
<td>UC3849xx</td>
<td>1000</td>
<td>3.3, 5.5</td>
<td>2</td>
<td>1.5, 1.8, 2.5</td>
<td>✔</td>
<td></td>
<td></td>
<td>0.36</td>
</tr>
<tr>
<td>UC3848xx</td>
<td>500</td>
<td>3.3, 5.5</td>
<td>2</td>
<td>1.5, 1.8, 2.5</td>
<td>✔</td>
<td></td>
<td></td>
<td>0.39</td>
</tr>
</tbody>
</table>

1. $PG = \text{PowerGood}$, $EN = \text{Active High Enable}$, $/EN = \text{Active Low Enable}$, $SVS = \text{Supply Voltage Supervisor}$
2. $C = \text{Ceramic}$, $T = \text{Tantalum}$, $\text{No Cap} = \text{Capacitor Free LDO}$

## MOSFET DRIVER

<table>
<thead>
<tr>
<th>Device</th>
<th>No. of Outputs</th>
<th>Output Type</th>
<th>$I_D$ Source/Sink (A)</th>
<th>Rise/Fall Time (ns)</th>
<th>$V_{CC}$ Range (V)</th>
<th>Prop Delay (ns)</th>
<th>Input Threshold</th>
<th>Enable</th>
<th>Dead Time Control</th>
<th>Protection Features</th>
<th>Internal Regulator</th>
<th>Price 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>UC37323</td>
<td>2</td>
<td>Inverting</td>
<td>TrueDrive</td>
<td>4.0</td>
<td>25/25</td>
<td>4 to 15</td>
<td>TTL/CMOS</td>
<td>No</td>
<td>No</td>
<td>—</td>
<td>No</td>
<td>0.99</td>
</tr>
</tbody>
</table>

1. Suggested resale price in U.S. dollars in quantities of 1,000.

## LOADSHARE CONTROLLERS

<table>
<thead>
<tr>
<th>Device</th>
<th>$V_{IN}$ (min)</th>
<th>$V_{IN}$ (max)</th>
<th>Reference Accuracy (%)</th>
<th>Share Bus</th>
<th>Pin Count</th>
<th>Supply Current (mA)</th>
<th>Price 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>UC29002</td>
<td>4</td>
<td>15</td>
<td>100</td>
<td>Single Ended</td>
<td>8</td>
<td>2.5</td>
<td>0.89</td>
</tr>
</tbody>
</table>

1. Suggested resale price in U.S. dollars in quantities of 1,000.
## DUAL-OUTPUT LDOs

<table>
<thead>
<tr>
<th>Device</th>
<th>Iq1 @ Vin1 (mA)</th>
<th>Iq2 @ Vin2 (mA)</th>
<th>Vref @ Iq1 (V)</th>
<th>Vref @ Iq2 (V)</th>
<th>Voltage (V)</th>
<th>Adj.</th>
<th>Accuracy (%)</th>
<th>PWP Package</th>
<th>Min V0 (V)</th>
<th>Max V0 (V)</th>
<th>/EN</th>
<th>PG</th>
<th>SVS</th>
<th>Seq</th>
<th>Low Noise</th>
<th>Min V0 (µA)</th>
<th>Max V0 (µA)</th>
<th>C0</th>
<th>Description</th>
<th>Price²</th>
</tr>
</thead>
<tbody>
<tr>
<td>PT503xx</td>
<td>250</td>
<td>150</td>
<td>83</td>
<td>—</td>
<td>95</td>
<td>✔</td>
<td>✔ ✔</td>
<td>✔ ✔ ✔ ✔</td>
<td>3.3/2.5, 3.3/1.8, 3.3/1.5, 3.3/1.2</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>2.7</td>
<td>5.5</td>
<td>10 µF</td>
<td>T</td>
<td>Dual-output LDO with sequencing</td>
<td>1.91</td>
</tr>
<tr>
<td>PT504xx</td>
<td>250</td>
<td>150</td>
<td>83</td>
<td>—</td>
<td>95</td>
<td>✔</td>
<td>✔ ✔</td>
<td>✔ ✔ ✔ ✔</td>
<td>3.3/2.5, 3.3/1.8, 3.3/1.5, 3.3/1.2</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>2.7</td>
<td>5.5</td>
<td>10 µF</td>
<td>T</td>
<td>Dual-output LDO with independent enable</td>
<td>1.91</td>
</tr>
<tr>
<td>PT505xx</td>
<td>500</td>
<td>250</td>
<td>170</td>
<td>—</td>
<td>95</td>
<td>✔</td>
<td>✔ ✔</td>
<td>✔ ✔ ✔ ✔</td>
<td>3.3/2.5, 3.3/1.8, 3.3/1.5, 3.3/1.2</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>2.7</td>
<td>5.5</td>
<td>10 µF</td>
<td>T</td>
<td>Dual-output LDO with sequencing</td>
<td>2.17</td>
</tr>
</tbody>
</table>

## PLUG-IN POWER SOLUTIONS

### Isolated Multiple Output

<table>
<thead>
<tr>
<th>Device</th>
<th>Input Bus Voltage (V)</th>
<th>Description</th>
<th>POUT or IOUT</th>
<th>Isolated Outputs</th>
<th>V0 Range (V)</th>
<th>V0 Adjustable</th>
<th>Price²</th>
</tr>
</thead>
<tbody>
<tr>
<td>PT8420</td>
<td>48</td>
<td>35-W 48-V Input Triple Low-Voltage Isolated DC/DC Converter</td>
<td>35 W</td>
<td>Yes</td>
<td>1.2 to 5.0</td>
<td>Yes</td>
<td>64.83</td>
</tr>
<tr>
<td>PT8450</td>
<td>48</td>
<td>75-W 48-V Input Triple Low-Voltage Isolated DC/DC Converter</td>
<td>75 W</td>
<td>Yes</td>
<td>1.2 to 3.3</td>
<td>Yes</td>
<td>96.64</td>
</tr>
</tbody>
</table>

### Isolated Single Output

<table>
<thead>
<tr>
<th>Device</th>
<th>Description</th>
<th>POUT or IOUT</th>
<th>Isolated Outputs</th>
<th>V0 Range (V)</th>
<th>V0 Adjustable</th>
<th>Price²</th>
</tr>
</thead>
<tbody>
<tr>
<td>PT4140</td>
<td>100-W 30-A 48-V Input Isolated Programmable DC/DC Converter</td>
<td>100 W</td>
<td>Yes</td>
<td>1.05 to 5.7</td>
<td>5-bit programmable</td>
<td>70.20</td>
</tr>
</tbody>
</table>

## HOT SWAP CONTROLLERS (EXTERNAL FET)

### Device

<table>
<thead>
<tr>
<th>Device</th>
<th>Target Applications</th>
<th>Channels</th>
<th>Vin (V)</th>
<th>Enable/Shutdown</th>
<th>Power Good or UVLO Reporting</th>
<th>Ramp</th>
<th>Automatic Retry/Latch</th>
<th>Average Power Limiting</th>
<th>Price¹</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS2390</td>
<td>–48-V Telecom</td>
<td>1</td>
<td>–36 to –80</td>
<td>1H</td>
<td>UVLO</td>
<td>Current</td>
<td>Latch</td>
<td>No</td>
<td>1.15</td>
</tr>
<tr>
<td>TPS2391</td>
<td>–48-V Telecom</td>
<td>1</td>
<td>–36 to –80</td>
<td>1H</td>
<td>UVLO</td>
<td>Current</td>
<td>AutoRetry</td>
<td>No</td>
<td>1.15</td>
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</tbody>
</table>

## DC/DC CONTROLLERS

### Performance Processor Power Supply Controllers (Synchronous Rectification)

<table>
<thead>
<tr>
<th>Device</th>
<th>VIN (V)</th>
<th>V0 (max) (V)</th>
<th>V0 (min) (V)</th>
<th>Vref Tol (%)</th>
<th>Driver Current (A)</th>
<th>Output Current (A)</th>
<th>Multiple Outputs</th>
<th>Adaptive Voltage Positioning</th>
<th>Protection²</th>
<th>Comments</th>
<th>Price³</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS40000</td>
<td>2.25 to 5.5</td>
<td>4</td>
<td>0.7</td>
<td>1.5</td>
<td>1</td>
<td>15</td>
<td>No</td>
<td>No</td>
<td>OCP, UVLO</td>
<td>300-kHz low input sync buck, source only</td>
<td>0.99</td>
</tr>
<tr>
<td>TPS40001</td>
<td>2.25 to 5.5</td>
<td>4</td>
<td>0.7</td>
<td>1.5</td>
<td>1</td>
<td>15</td>
<td>No</td>
<td>No</td>
<td>OCP, UVLO</td>
<td>300-kHz low input sync buck, source/sink except SS</td>
<td>0.99</td>
</tr>
<tr>
<td>TPS40002</td>
<td>2.25 to 5.5</td>
<td>4</td>
<td>0.7</td>
<td>1.5</td>
<td>1</td>
<td>15</td>
<td>No</td>
<td>No</td>
<td>OCP, UVLO</td>
<td>600-kHz low input sync buck, source only</td>
<td>0.99</td>
</tr>
<tr>
<td>TPS40003</td>
<td>2.25 to 5.5</td>
<td>4</td>
<td>0.7</td>
<td>1.5</td>
<td>1</td>
<td>15</td>
<td>No</td>
<td>No</td>
<td>OCP, UVLO</td>
<td>600-kHz low input sync buck, source/sink except SS</td>
<td>0.99</td>
</tr>
<tr>
<td>TPS40050</td>
<td>8 to 40</td>
<td>30</td>
<td>0.7</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>20</td>
<td>No</td>
<td>No</td>
<td>OCP, UVLO</td>
</tr>
<tr>
<td>TPS40051</td>
<td>8 to 40</td>
<td>30</td>
<td>0.7</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>20</td>
<td>No</td>
<td>No</td>
<td>OCP, UVLO</td>
</tr>
<tr>
<td>TPS40053</td>
<td>8 to 40</td>
<td>30</td>
<td>0.7</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>20</td>
<td>No</td>
<td>No</td>
<td>OCP, UVLO</td>
</tr>
<tr>
<td>TPS40060</td>
<td>10 to 55</td>
<td>40</td>
<td>0.7</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>10</td>
<td>No</td>
<td>No</td>
<td>OCP, UVLO</td>
</tr>
<tr>
<td>TPS40061</td>
<td>10 to 55</td>
<td>40</td>
<td>0.7</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>10</td>
<td>No</td>
<td>No</td>
<td>OCP, UVLO</td>
</tr>
</tbody>
</table>

¹Current levels of this magnitude and beyond can be supported.
²OCP — over-current protection; UVLO — under-voltage lockout
³Suggested resale price in U.S. dollars in quantities of 1,000.

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1See power.ti.com for a complete product offering.
2Suggested resale price in U.S. dollars in quantities of 1,000.

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