Understanding the Clock Architecture of the OMAP4430 - Public -

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ABSTRACT

This application note describes the clock architecture of OMAP4430 from the perspective of the PRCM. A single diagram of the clock architecture summarizes all of the clock signals including the PRCM register bits that affect them. Using this diagram, SW developers can quickly understand and find the relevant register bits necessary for configuring the clocks within the OMAP4430.

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History

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Version	Date	Author	Notes
1.0	Aug/23/2010	A0783816	1

1. Created Document

1 Introduction

This application note provides an overview of the clock architecture for OMAP4430. A power reset clock manager (PRCM) module has multiple registers that are used to control the clocks for each module in the OMAP device. It is useful to find which bits should be set to enable a module.

2 How to use this clock architecture diagram

Please read the important information in this section before using the diagram.

2.1 Supported Silicon Revision

This figure supports OMAP4430 ES2.0. It doesn't support OMAP4430 ES1.0.

2.2 Multiple Instances of a Module

OMAP4430 has multiple instances of some modules. For example, there are multiple instances for the GPIO, McBSP and GPTimer modules. For simplicity's sake, these modules are combined. However some modules are not assigned to the same power domain, so they are drawn separately. For example, GPIO1 & GPIO2-6 are drawn separately since they are in different power domains.

2.3 Power Domain Colors

Background colors show the assigned power domain. The color details are as follows:

Rose	: Always-on Core domain
Light Green	: Core domain
Sky Blue	: Wakeup domain
Purple	: MPU domain
Light Purple	: Always-on MPU domain
Red	: DSP domain
Orange	: IVA domain
Light Orange	: Always-on IVA domain
Lavender	: L3-INIT domain
Pink	: SGX domain
Yellow	: CAM domain
Green	: DSS domain
Gray	: L4-PER domain
Blue	: ABE domain
Dark Green	: STD-eFuse domain
Blown	: EMU domain

2.4 Not supported in the figure

This figure does not support all clock control features for the OMAP4430 because some modules have an internal clock that is not controlled by the PRCM. This figure comes from the PRCM's standpoint.

For example: DSI PLLx output can be used for DSIx_FCLK. It is controlled by DSIx_CLK_SWITCH bit in DSS.

3 Figure of the Clock configuration

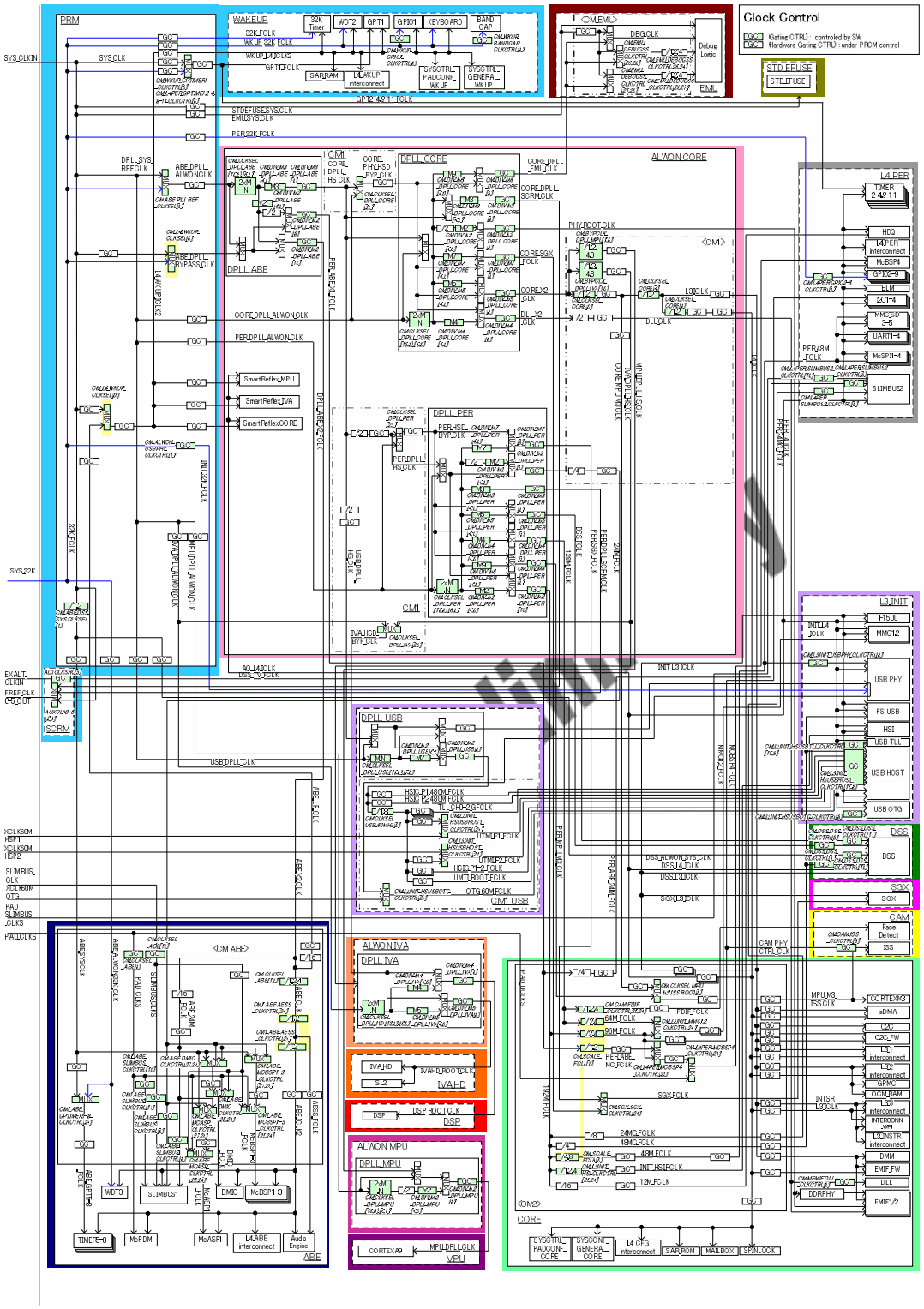

Figure 1. OMAP4430 Clock Architecture

References

The style "References Text" is used for the text below. You must manually apply the italics to the document title, as shown below. If you are referencing a TI document, include the basic literature number (with no revision letter) in parentheses after the title.

1. *Understanding the OMAP3630 Clock Architecture* (SWPA167)
2. *OMAP4430 ES2.0 NDA TRM v.I*
3. *CTT-OMAP4430ES1.0-v1.7.0.1*

OMAP4430 Disclaimer

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