WHITE PAPER

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TEXAS INSTRUMENTS

# Leveraging the Benefits of Symmetric Multiprocessing (SMP) in Mobile Devices

## Introduction

*Mobile devices, such as Smartphones and Mobile Internet Devices (MIDs), are beginning to deliver advanced functions, such as PC-like web browsing, high-definition (HD) video record and playback, digital SLR-like imaging and 3D graphics. To be able to deliver these functions, plus traditional phone services, such as voice, SMS, Bluetooth® and GPS, all in a small form factor with all day battery life, advanced processing techniques combined with power management techniques are needed to move mobile devices to this next level of service.*

*Symmetric Multiprocessing (SMP) has traditionally been used in PCs to extend performance. SMP is coming to mobile devices to provide a dramatic increase in on-demand processing performance along with power scalability. Texas Instruments' new OMAP™ 4 platform is able to deliver outstanding mobile computing and multimedia performance at low power levels, thanks in part to the included dual-core ARM® Cortex™-A9 MPCore with SMP general-purpose processing working in conjunction with power-efficient, heterogeneous processing engines for demanding multimedia. TI is leading the way in bringing SMP to mobile devices to power the next generation of high-performance, low-power applications.*

## What is SMP and why do you need it?

Symmetric Multiprocessing (SMP) has been used extensively in the PC market to bring high performance to the desktop PC. SMP allows multiple identical processing subsystems on a single chip, all running the same instruction set and with equal access to memory, I/Os and external interrupts. A single copy of the operating system (OS) controls all the cores to allow any processor to run any thread, be it a kernel, application or interrupt service.

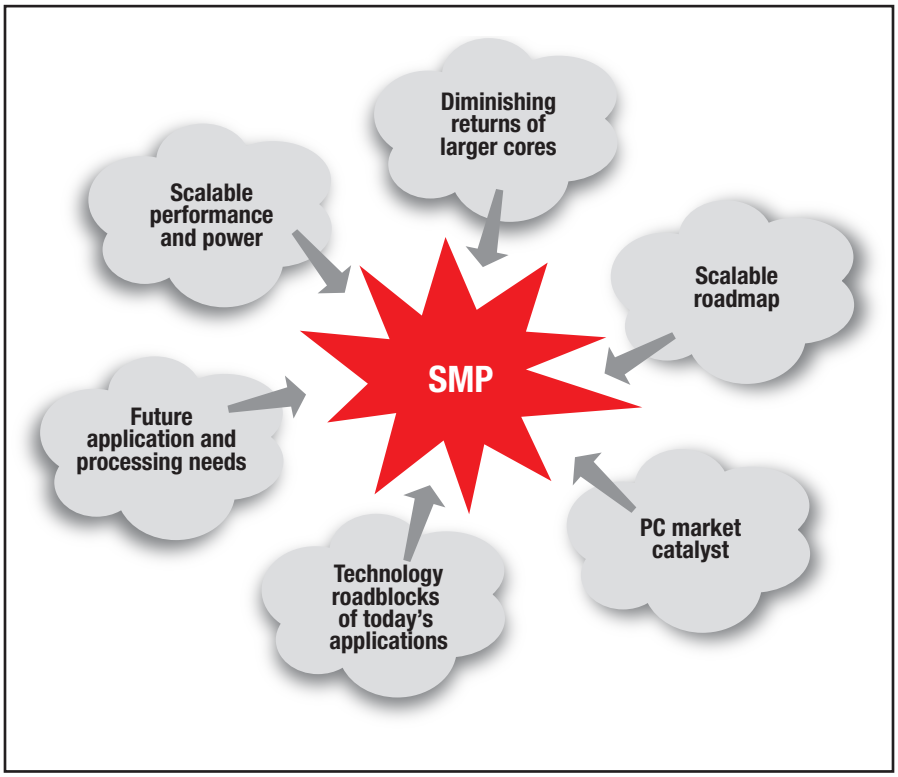


**Figure 1:** *Many factors are driving the need for SMP in mobile devices*

SMP will allow advances in mobile applications and devices not possible using today's unicore solutions. By activating the specific core or cores needed to perform a task, SMP allows OEMs to realize scalable performance and power to meet the challenges of today's most popular applications and tomorrow's yet-to-be-imagined applications.

The multitudes of new applications, such as uncompromising web browsing, are increasing the peak computing performance needed on mobile devices. Current unicore solutions are unable to meet this need; only SMP will be able deliver the performance needed within the space and power constraints of mobile devices. While it is possible to increase the size of the unicore solution to meet performance needs, the increase in power consumption is unacceptable in mobile devices. SMP is one architectural technique used to meet this need.

Advanced mobile applications are expected to be as complex as existing PC applications, and threading techniques developed in the PC world are expected to be migrated to the mobile handset. The same challenges that forced the PC processors (i.e., smaller increases in performance with substantially increased silicon complexity for a unicore die) to move to a multicore architecture are found in mobile handsets as well. In addition, delivering higher performance on a larger unicore solution is expensive and requires more complexity, resulting in a longer time to market with a more complex design and validation process.

The PC market has been a catalyst to SMP acceptance and many PCs today have 2 or 4 cores included. ARM Ltd. has been driving SMP into the handheld market with the introduction of its Cortex™-A9 MPCore architecture. In support of this new family of SMP cores, operating systems such as Linux and Symbian have added support for SMP.

SMP will allow a scalable roadmap for products with one to four cores or more into the future. With a scalable roadmap from low to high tier devices, SMP will leverage the developer's software investment to deliver products that meet the varying levels of performance needed for different markets.

## *Mobile constraints*

The mobile device itself has many constraints that SMP must overcome to be successful. The most obvious constraints are size, cost and power consumption. Consumers expect their mobile devices to be a small form factor that will easily fit in a pocket or purse and to have all-day performance on a single battery charge. The cost of the mobile handset must also be one that the market will bear. SMP helps to overcome these mobile constraints, delivering a device that satisfies the consumer's desires. SMP will allow advanced applications to be run efficiently, but care must be taken so that the additional cores do not negatively affect low power consumption. New techniques must be used to allow unicore-like power consumption in a SMP device.

With the integration into the mobile handset of functions that were formally only found on PCs, such as web browsing, multimedia and WLAN connectivity, as well as the integration of standard mobile functions, like voice and Bluetooth, the need for performance is ever increasing. But, in a mobile environment, the increased performance must be done efficiently and on-demand to deliver the power performance needed. Optimization of power and performance for each use case will deliver the maximum

battery life and performance. SMP allows smartphones to integrate both PC and traditional phone services into a single mobile device at the power and performance demanded by users.

ARM has a dominant position in mobile devices today. With this dominance comes the need for legacy code support as well as great tools. Going forward, SMP will require that legacy code be made SMP-safe for proper operation and to realize the power and performance savings available.

A final mobile constraint that must be addressed is balancing the need to minimize die size, but providing large enough memory cache to keep multiple cores from being stalled. If a single core device requires N amount of cache, up to 4*N cache may be required to achieve good performance in a multicore device. Other memory design issues include data coherence and system memory consistency, to ensure processors all have access to the current data at the correct time.

## *ARM Cortex-A9 MPCore*

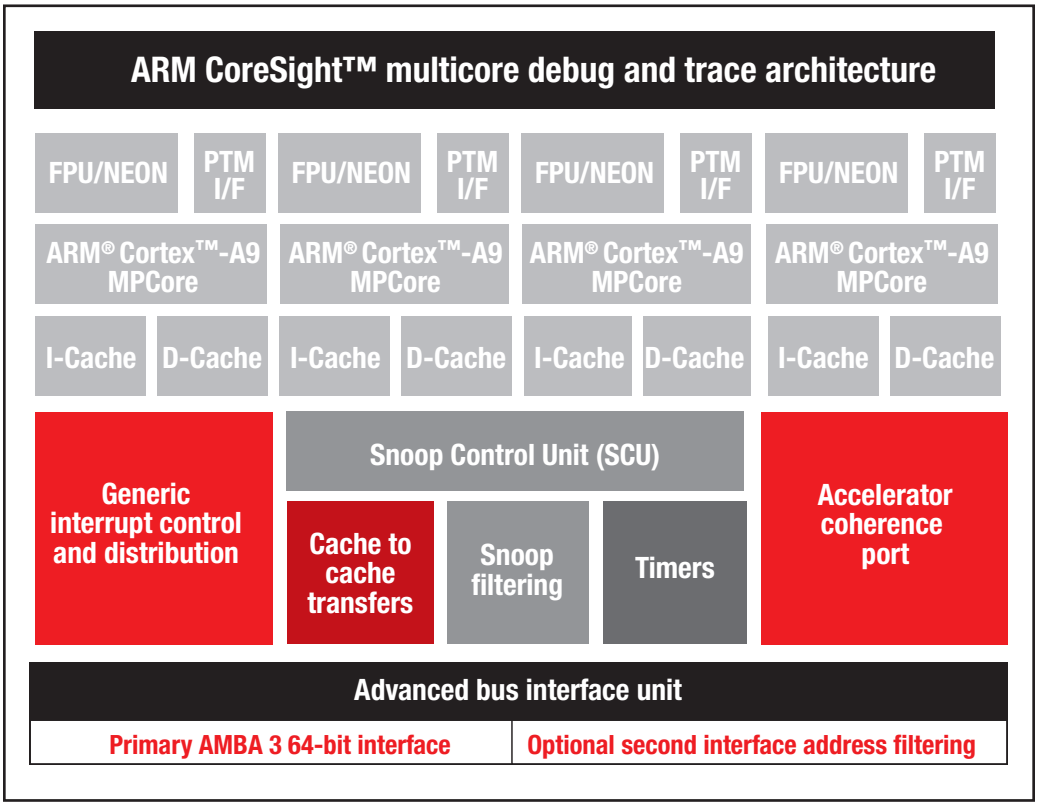


**Figure 2:** *ARM® Cortex™-A9 MPCore™ delivers scalable power and performance for mobile devices*

To meet the needs of the mobile handset market for scalable power and performance, ARM has introduced the Cortex-A9 MPCore architecture. The Cortex-A9 MPCore is able to deliver 20% higher processing efficiency (IPC) than the ARM Cortex-A8, allowing designers to do more with less MHz.

The Cortex-A9 MPCore can support up to 4 cores in a cluster, giving customers the flexibility to design products for their specific need. The Cortex-A9 MPCore includes a rich set of features, including:

- High-efficiency superscalar pipeline for outstanding peak performance at low power
- NEON media processing engine for accelerated media processing functions
- Floating point unit with double the performance of the previous ARM FPU
- Optimized Level 1 caches to minimize latencies and power consumption
- Thumb®-2 technology for up to a 30 percent reduction in memory requirements
- TrustZone® technology for reliable security applications
- L2 cache controller for low latency, high bandwidth memory access
- CoreSight™ multi-core debug and trace architecture for improved visibility during development and debug

The Cortex-A9 MPCore is a smaller core than the Cortex-A8 and uses less power but at the same time yields a higher processing efficiency. The scalable peak performance along with advanced power management allows the Cortex-A9 MPCore to exceed the performance of comparable single-core architectures, giving multicore designs a distinct advantage. The Cortex-A9 MPCore is able to provide a single platform that can be scaled across multiple markets while taking advantage of common software development to lower research and development costs while speeding time to market.

## *SMP benefits to applications and products*

Manufacturers today want to invest in a platform that they can leverage and scale across tiers of products as well as into the future. SMP is able to deliver this with real performance scalability. Unlike previous solutions that scaled the speed of just one core, SMP will allow true scalability across multiple cores to deliver the right mix of performance and power consumption for every product.

SMP will allow manufacturers to support future products, such as netbooks, at a higher performance with a single platform. Once software has been developed for SMP, designers can add as many processors as needed to meet future needs and it will be transparent to the software. Designing with SMP gives manufacturers a solid foundation for future applications.

## *SMP software implications*

SMP delivers performance increases at any level of software. In software that is not SMP aware, parallelism is gained by using the OS task manager to launch a process on each core. Performance is inherently increased from parallel process execution and though it is not as efficient as thread-level processing, it does not pose any extra burden on the applications' developers.

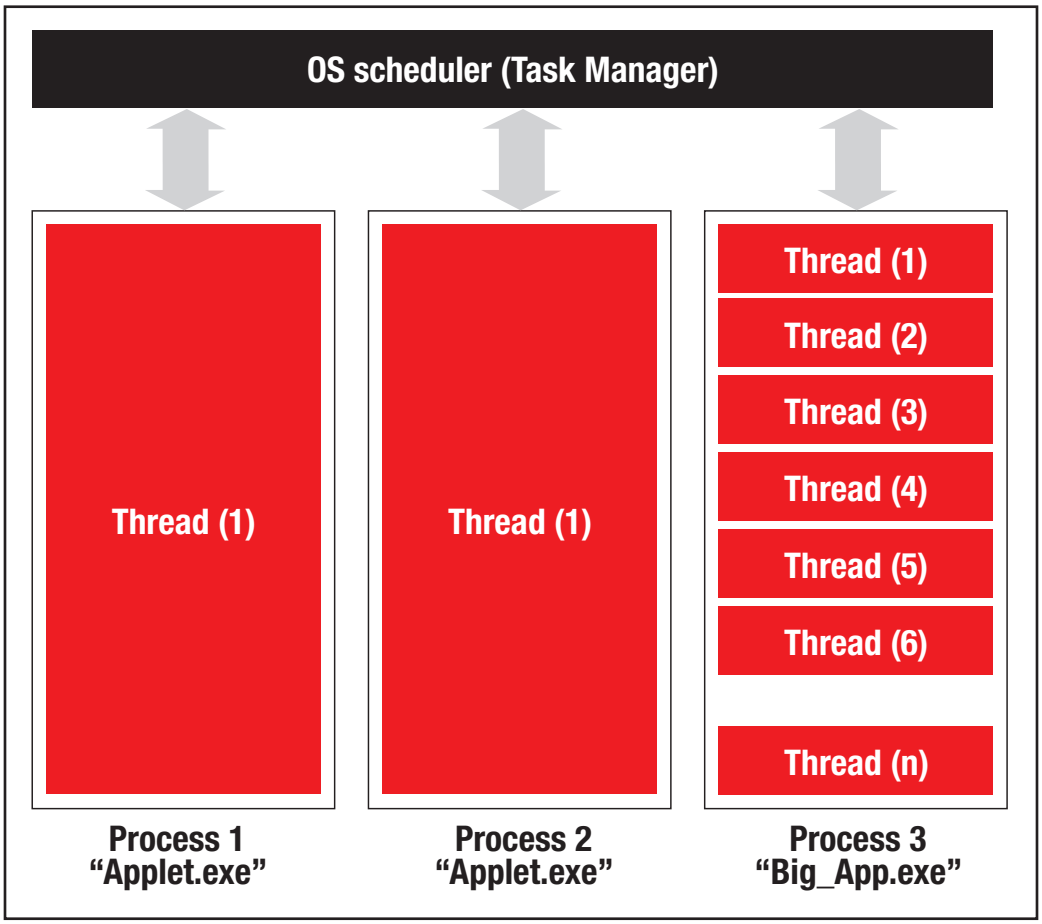


**Figure 3:** *SMP delivers performance increases at the process and thread levels of software*

With the increased performance available in mobile devices, user applications are growing in complexity, and as such, will need to be written in a more parallel way (e.g., with threads). This makes them ideal to realize the true benefits and gains of SMP. Threads make up the processes and do not need to keep going back to the OS for resources. The applications' developer has to design the software in terms of "parallelism" and must pay attention to how threads within a process may interact.

Certain applications are inherently multi-threaded allowing SMP to provide increased performance, faster response times and an overall better user experience. Web browsers, such as Google's Chrome browser, use multiple threading, making them highly complementary to SMP technology. It is expected the techniques used for these PC web browsers will be brought to the mobile world as well.

Symbian and Linux mobile OSes have both added support for SMP. This support has been optimized for the mobile environment and will allow a single OS image across all the processor cores as well as load balancing within the scheduler to help determine which task or thread to run on which core.

When dealing with legacy software, care must be taken to synchronize tasks correctly to avoid any system lock-ups. In an SMP system, the OS can schedule low-priority tasks to run on a different core at the same time a higher priority task is running on another core. If the software includes any implicit synchronization, false assumptions could be made resulting in lock conditions. With the use of "good practice" software techniques, such as semaphores, mutexes and spinlocks, programming software for SMP cores will allow full realization of the benefits of SMP.

Tools for development and debug on SMP systems will be critical. Designers will need greater visibility into the chip to be able to follow the software processing. With multiple threads all running at the same time on multiple cores, powerful new tools will help manufacturers bring amazing new products to market quickly.

## *Advanced power management for SMP*

SMP delivers a scalable power benefit with the ability to scale the core frequency as well as the number of active cores. The Cortex-A9 MPCore has the ability to turn individual cores on and off. If cores are on, they must both be run at the same clock rate. So to effectively use power management in SMP cores, testing must be done to determine performance and power consumption benchmarks for two options: running the process on one core at maximum clock rate while other cores are off or using multiple cores running at the same reduced clock rate.

Other power management techniques used with SMP include dynamic voltage and frequency scaling (DVFS) which allows the frequency and voltage of the system to be adjusted to match the performance required. The ability of the OS to do load balancing also contributes to the power management and allows the designer to optimize the system for power consumption.

TI's OMAP 4 platform is one of the first dual-core, ARM Cortex-A9 MPCore based architectures balanced with specialized processing engines for unsurpassed mobile multimedia performance.

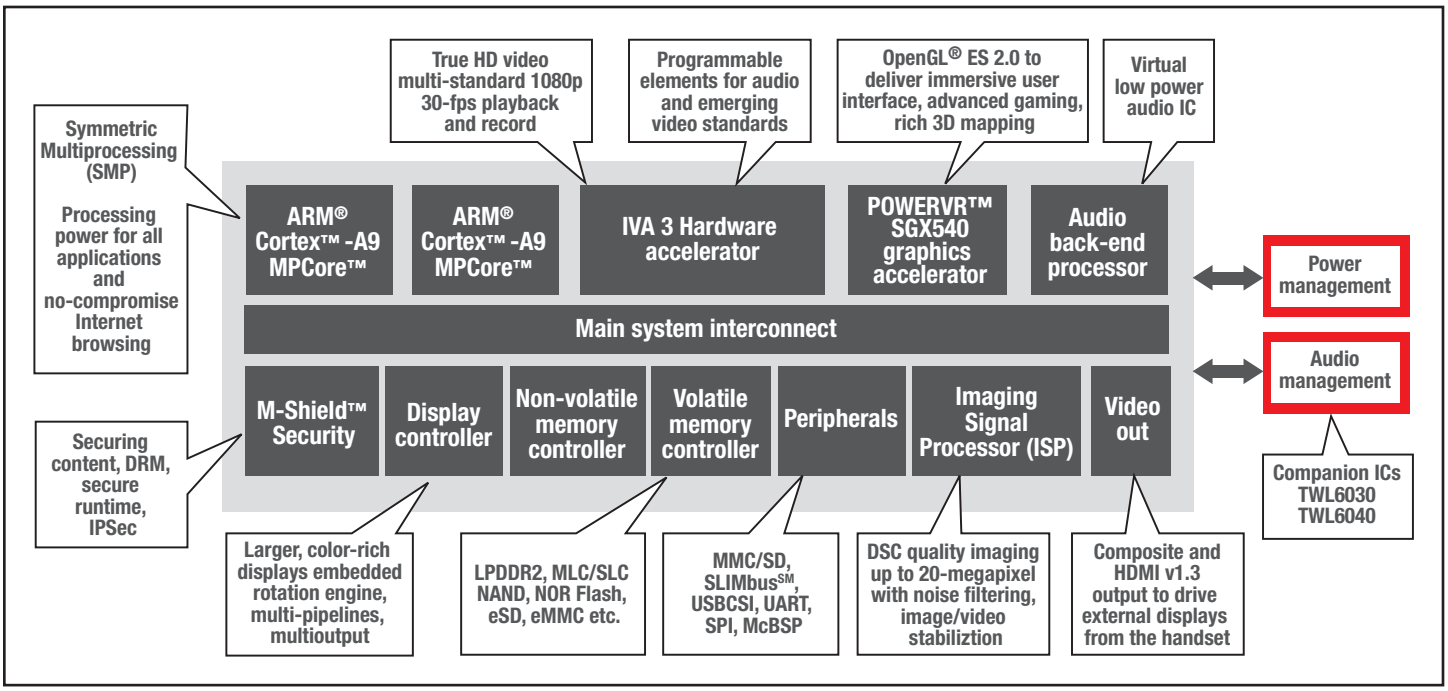


**Figure 4:** *TI's new OMAP 4 platform delivers SMP for mobile devices*

***Key features of the OMAP 4 platform include:***

- Dual-core ARM Cortex-A9 MPCore SMP general-purpose processors for higher performance and efficiency
- IVA 3 Hardware accelerator to deliver true 1080p multi-standard HD record and playback
- Image Signal Processor (ISP) for high-quality image and video capture, delivering digital SLR-like performance with 20 megapixel still image capture
- Imagination Technologies POWERVR™ SGX540 3D graphics core for 3D user interfaces with larger displays, life-like graphics and intuitive touch screens
- Audio back end (ABE) processor provides a virtual low power audio chip for significant power savings
- Flexible system support
  - Composite TV output
  - HDMI v1.3 output to drive HD displays
  - Larger, color rich display support
  - Peripheral interfaces: MIPI serial camera and serial display interfaces, MIPI® SLIMbus℠, MMC/SD, USB 2.0 On-The-Go High Speed, UART, SPI, and more
- Support for all major OSes: Linux (including Android and LiMo), Microsoft Windows Mobile and Symbian
- 45-nm mobile process technology for improved performance and power efficiency
- Optimized power and audio management companion chips: TWL6030 and TWL6040

TI is the only company that is supporting SMP with all the major mobile OSes, including Symbian, Linux and Microsoft Windows Mobile. The OMAP 4 platform is leading the mobile industry in the transition to SMP and was specifically architected for optimal SMP performance. For example, design considerations went into the memory architecture as well as the cache size and memory interface to provide the best performance

with the least amount of latency. TI's comprehensive software suite, included in the OMAP 4 platform, was written specifically for SMP and makes full use of the processing performance increases and power savings available with a SMP architecture.

The OMAP 4 platform leverages the most advanced and effective power management techniques in the market to gain additional power conservation. The processors make extensive use of TI's SmartReflex™ 2 power and performance management technologies, which include a broad range of intelligent and adaptive hardware and software techniques that dynamically control voltage, frequency and power based on device activity, modes of operation and temperature, including:

- Dynamic Voltage and Frequency Scaling (DVFS)
- Adaptive Voltage Scaling (AVS)
- Dynamic Power Switching (DPS)
- Static Leakage Management (SLM)
- Adaptive Body Bias (ABB)
  - Forward Body Bias (FBB) for slower devices
  - Reverse Body Bias (RBB) for leakage reduction of faster devices

The OMAP 4 platform takes full advantage of TI's expertise and long track record in mobile devices to deliver a new SMP based processor for the applications of today and tomorrow.

## *OMAP 4 SMP in action*

In order to understand the benefits of SMP in a mobile device and how OMAP 4 can be used, two use cases will be examined. The first use case involves a web browser. Tomorrow's mobile devices will deliver PC-like web browsing directly on a handset. Web browsers are inherently multi-threaded applications and a good fit for SMP. In this case, the OS scheduler would use both cores at a lower frequency to deliver a fast web browsing experience.

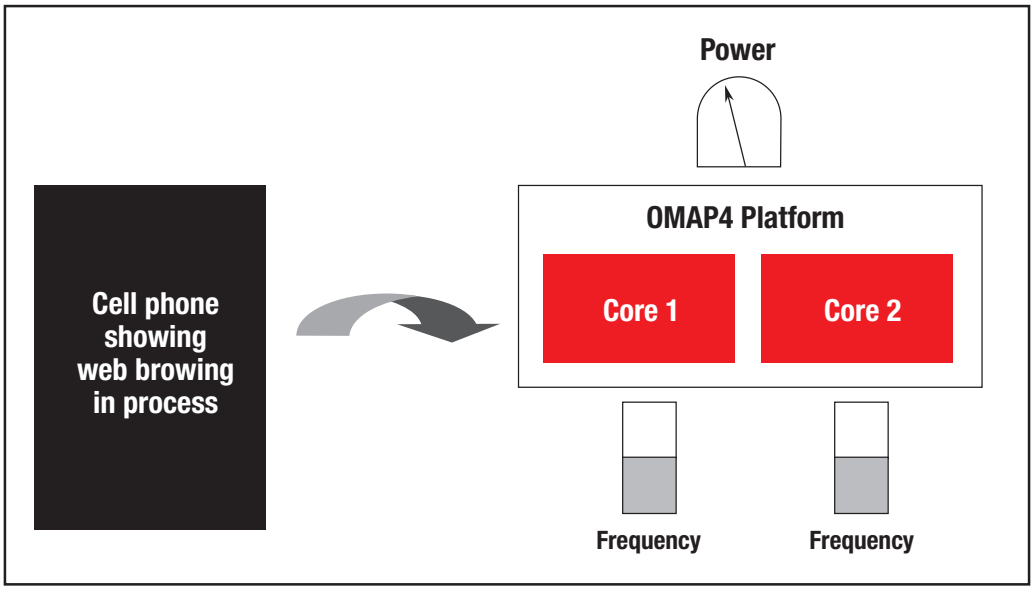


**Figure 5:** *OMAP 4 SMP helps to deliver PC-like web browsing experiences*

In a second use case, a consumer is viewing H.264 video on their handset. Multimedia cases, such as this, do not thread well and would be better suited for single core use. In this case, the OMAP 4 would turn off one of the cores and run the other core at a higher frequency to deliver outstanding multimedia content. Because only one core is active, power consumption savings can be realized.

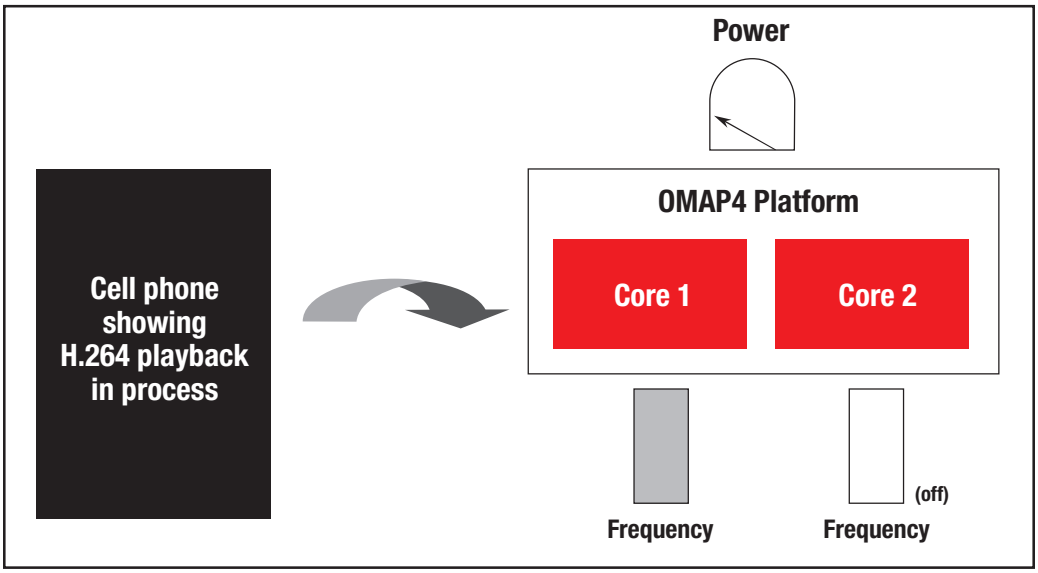


**Figure 6:** *OMAP 4 delivers outstanding multimedia content*

## Conclusions

SMP will be important to meet the high performance and low power requirements of next-generation mobile devices. The scalable power and performance abilities of SMP give it a unique advantage over unicore solutions. Future applications will make more use of multithreading, making SMP the platform of choice.

TI's OMAP 4 platform is the first device to offer SMP for scalable general-purpose processing performance, while still increasing functionality and capability in the multimedia processing domains (imaging, graphics, audio and video). It is important to note that SMP does not absorb the functionality of these multimedia domains which require specialized engines to provide the highest performance at the lowest power. The OMAP 4 platform provides an optimal mix of SMP and will work together with asymmetric multiprocessing (AMP).

TI's OMAP 4 platform is leading the way for SMP in mobile devices to power fantastic applications of the future. By investing in SMP today, future software re-use will be seamless, and OEMs will be able to scale their designs across product tiers as well as into the future.

*References:*

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