WHITE PAPER

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TEXAS INSTRUMENTS

Designing for the Use Case:

Using the OMAP™ 4 platform to overcome the challenges with integrating multiple applications

Introduction

Today's wireless mobile devices offer a wealth of applications, everything from Internet browsing to video playback and record to CD-quality audio playback. In addition, mobile phones are offering applications requiring multiple antennas, such as FM, GPS, Bluetooth® and WLAN. Designing a platform that can successfully incorporate all of these applications as well as the next generation of applications, such as HD video, high-fidelity audio and digital SLR-like imaging is a challenge.

To create the best possible user experience, it takes a whole new way of looking at the design of the device. Handsets are no longer just for making a phone call and perhaps receiving a text. A use case might look like this: You are in the middle of watching a movie streaming over WLAN when a call comes through. The best use case would be for the phone to automatically switch to the call using your Bluetooth headset, pausing the movie, and then when the caller hangs up automatically switching back to the movie and resume playing from where you left off.

Designing for these complex use cases requires breaking it down into the system components, such as Bluetooth, video encode/decode, image processing, audio, etc. Each component can then be optimized as well as the interaction between components and the system. The OMAP™ 4 processor platform from TI has been designed with this philosophy to make customer development faster and easier by removing any roadblocks before the actual handset design starts.

Complex use-case challenges

When designing for the best user experience, there are four main complex use-case challenges that have to be overcome. The first of these is designing for sufficient bandwidth. The system must have enough memory, bus and processing bandwidth to handle the amount of information coming in and going out of the system without experiencing any system hangs.

The next challenge is latency. Users expect to have applications open instantly and to move between applications with no delay. Designing for the smallest possible latency in a system requires efficient resource sharing as well as highly optimized software.

The third challenge to designing for the use case is achieving seamless transitions between applications – in other words, having multiple applications in the same handset all sharing resources without interfering or interrupting each other. It is a significant challenge to design applications with maximum performance while maintaining coexistence.

The final challenge is designing for all-day battery life. Designing within the confines of today's available battery power while providing the performance needed for today's top applications, is a challenge. To find the optimal balance between power consumption and performance, a platform has to be designed with a holistic power management approach, one that looks at the entire system and not just on a chip-by-chip basis.

In order to meet these use-case challenges, the handset must be architected at the system level, not just at the chip level. TI has achieved this in designing the OMAP 4 platform for maximum performance and efficiency at the chip, software and system level. Pre-integrated OMAP 4 applications software, including everything up to the applications layer, provides high optimization and faster time to market. By designing the OMAP 4 platform to the most complex use case, TI has made HD multimedia as well as a host of other high-performance applications achievable.

Designing for bandwidth

The next generation of mobile devices will be expected to deliver full 1080p high-definition (HD) video playback at 30 frames per second (fps) with high-fidelity audio in-sync with the

video. Without enough bandwidth, not only would the audio be out of sync with the video, but the handset would also not be able to deliver the full 30 fps and you might only get 22 fps, at which point the human eye can detect the choppiness of the video. Additionally, if the system does not have enough bandwidth, applications such as Internet browsing will not deliver the PC-like experience users expect.

TI has designed the OMAP 4 platform to meet the bandwidth requirements of even the most complex use cases. The OMAP 4 platform includes a dual-core ARM® Cortex™-A9 MPCore symmetric multiprocessing (SMP) core to deliver higher peak computing performance than unicore solutions. With more than sufficient processing bandwidth for the most complex case, the OMAP 4 platform is also able to provide efficiency as well as flexibility to scale down to the simplest task.

In order to take advantage of this increase in processing bandwidth, higher bandwidth memory interfacing is required. The OMAP 4 platform integrates a 2-channel Low-Power Double Data Serial Communication Rate 2 (LPDDR2) memory interface, allowing 1080p video performance with concurrent system activity. A powerful DRAM Memory Manager (DMM) provides bandwidth optimization by providing virtual memory management for all the multimedia accelerators on the OMAP 4 platform as well as providing memory interleaving management.

Other improvements in the individual OMAP 4 subsystems help to deliver outstanding bandwidth. The video subsystem uses several bandwidth reduction techniques as well as incorporating its own on-chip high-bandwidth shared L2 memory. Some of the bandwidth reduction techniques include:

- Compression of the motion estimation search window luma data
- Motion estimation search window management
- Motion compensation bounding box to combine loads into one larger load
- Increased internal shared L2 buffer to reduce data traffic to DDR

An integrated graphics accelerator from Imagination Technologies, delivers outstanding 3D graphics on the OMAP 4 platform. The POWERVR™ SGX540, core is designed for mobile use and with its unique, tile-based, deferred rendering shading architecture is able to reduce memory bandwidth while doubling throughput of the shader and the iteration/texture pipe to allow immersive user interfaces, advanced gaming and rich 3D mapping applications at 4x sustained performance compared to their previous core. Also included is a 128-bit internal memory bus to meet the higher system bandwidth requirements and increased processing performance. The display subsystem of the OMAP 4 platform also includes an upgraded 128-bit OCP system interface to support the bandwidth increase.

A final example of the OMAP 4 platform's design for bandwidth is in the imaging subsystem. Delivering digital SLR-like performance with up to 20 megapixels at one second shot-to-shot delay requires a significant amount of processing bandwidth. The OMAP 4 platform's Image Signal Processor (ISP) provides fine bandwidth control for memory to memory operation to give 200-megapixels/second throughput at 200 MHz. A high-performance DMA engine further improves the ISP bandwidth.

All of these improvements together help to increase the OMAP 4 system performance and bandwidth to deliver the applications that users want at the performance level they demand.

Mobile handset users expect applications on their devices to run smoothly and with no delay when switching between applications. For example, if you are watching a video over WLAN and a call comes in, you expect to be able to take the call over your *Bluetooth* headset without any delay. If you are using the handset's built in camera, you expect to be able to take a picture and be able to take the next picture quickly, without having to wait for the handset to catch-up. Latency issues can be reduced with high-performance processors and high system bandwidth.

The OMAP 4 platform from TI incorporates a dual-core ARM Cortex-A9 SMP processor to deliver the highest performance, with a 150 percent increase in performance over previous ARM Cortex-A8 processors. Designers have re-architected the memory controller subsystem and bus system to enable more efficient multithreading for SMP applications. This new OMAP 4 platform enables better user experiences with smoother, more responsive UI's, faster handset startup, quicker application launch time and seamless multi-tasking across applications.

TI has taken other steps to ensure high performance and low latency on the OMAP 4 platform, including a hardwired video accelerator for mainstream video codecs that is able to deliver 1080p, 30 fps encode/decode for multiple standards. The high-speed ISP reduces shot-to-shot delay while still delivering up to 20-megapixel quality shots with a dedicated CPU for imaging applications.

By integrating an improved SDRAM controller, the OMAP 4 platform improves performance and therefore latency with techniques such as:

- Re-ordering commands for maximize overall memory usage
- Delayed writes to limit read-to-write or write-to-read transitions
- Support for single request/multiple data transactions on the OCP interface to effectively increase the look- ahead FIFO depth and allow more effective re-ordering of commands

A very important step that TI has taken to improve latency is the optimization and pre-integration of software up to the application level. This helps to reduce latencies early in the design process for maximum performance and system-level optimization to deliver low-latency applications to end users.

Designing for seamless transitions

With the integration of more and more applications onto a single platform, the complexity of seamless transition has become a critical design issue. For example, when a user is watching a video streaming over WLAN and listening to it over *Bluetooth* headphones, and receives a phone call, It is essential that the user be able to pause the movie, answer the call, and be able to return seamlessly to the movie without an delay, or experience dropped video frames or loss of sync of the audio and video.

The challenge is having multiple applications running at the same time and sharing resources without impacting responsiveness or in the worst case shutting down the system. It is important to manage the resources that are shared by the multiple cores on the device.

There are three major aspects to consider for resource sharing: bandwidth, processor load, and memory. Each of the high-performance use cases needs guaranteed headroom to enable the launching of another

application simultaneously. When starting an application you are not running at peak performance and need to ensure the handover of resources does not result in a degradation in performance that is perceptible by the user.

To combat these transition issues between applications issues, TI has pre-integrated operating system (OS) and multimedia applications software to test the interaction of the IC and the HLOS to ensure that seamless transitions are possible. This complex testing methodology ensures that issues have been found and corrected before going into the customer's design. This highly optimized software increases the system throughput and responsiveness, while ensuring that all applications can operate simultaneously with no issues.

Designing for power

The power use case for next-generation phones continues to become more extensive as more powerful applications are added onto the devices. Users expect an all day Internet experience on a single charge or to have over 100+ hours of audio playback in airplane mode. All of these applications require more advanced power management technologies to deliver the performance users want.

The OMAP 4 platform integrates SmartReflex™ 2 technologies from TI for advanced power management and optimized performance. SmartReflex 2 technology delivers hardware and software support for the most advanced power management techniques, including Dynamic Voltage & Frequency Scaling (DVFS), Adaptive Voltage Scaling (AVS), Dynamic Power Switching (DPS), Static Leak Management (SLM) and Adaptive Body Bias (ABB).

DVFS dynamically adjusts the voltage and frequency to adapt to the performance needed in the system for that particular application. With independent DVFS support on multiple voltage domains, the OMAP 4 platform is able to run at the most adequate voltage and frequency, minimizing power consumption while allowing the core domain to be kept at a fixed frequency or scaled down for the very low power use cases.

AVS maintains high performance while minimizing voltage with a complete hardware closed loop that continuously adapts the domain voltage based on the silicon process and temperature conditions. AVS ensures that every voltage domain will always run at the minimum possible voltage at every operating/performance point (OPP).

DPS and SLM both work to reduce the leakage power on a silicon chip. DPS dynamically switches between power modes based on system activity while SLM allows the lowest standby power mode compatible with the required system responsiveness to reduce leakage power. These two technologies help to solve the chip-level leakage power challenge that is exacerbated at smaller, deep-submicron process geometries, like the 45-nm process of the OMAP 4 platform.

ABB can be broken down into two different techniques, Forward Body Bias (FBB) for up to a 15 percent performance boost of slow devices and Reverse Body Bias (RBB) for leakage reduction of fast devices by as much as 40 percent. FBB and RBB enable small modifications in the transistor threshold voltages after the device has been manufactured and is in operation to gain performance and reduce leakage.

All of these advanced power management techniques, along with pre-integrated interface, OS and multimedia applications software ensures that every power optimization has been made that is available on the OMAP 4 platform.

Successfully designed for the complex use case

In order to design successful handsets in the future, OEMs must take into account very complex use cases. This requires breaking down each use case into system-level components and optimizing each component as well as the overall system. While there are multiple use cases, there are four key design challenges to overcome: bandwidth, latency, seamless transitions and power. Handsets designed without consideration of these challenges will fail to meet the demands of next-generation handset design.

TI has designed the OMAP 4 platform at the chip, software and system level to address these challenges and to meet the needs of next-generation handsets. With power and performance optimization already incorporated in the OMAP 4 platform, customers are free to design the next generation of applications and handsets.

For more information

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