

## 3-V TO 5.5-V MULTICHANNEL RS-232 1-MBit/s LINE DRIVER/RECEIVER

Check for Samples: [MAX3237E](#)

### FEATURES

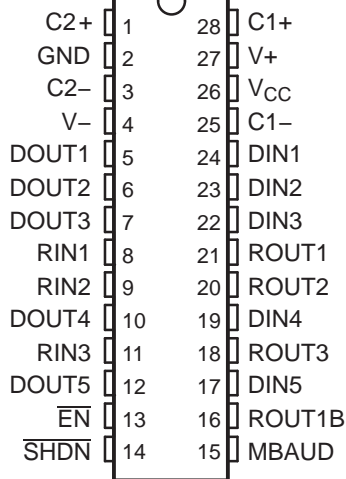
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V  $V_{CC}$  Supply
- Operates From 250 kbit/s to 1 Mbit/s
- Low Standby Current . . . 1  $\mu$ A Typical
- External Capacitors . . . 4 x 0.1  $\mu$ F
- Accepts 5-V Logic Input With 3.3-V Supply
- Designed to Be Interchangeable With Maxim MAX3237E
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

- ESD Protection for RS-232 I/O Pins
  - $\pm$ 15 kV – Human-Body Model (HBM)
  - $\pm$ 8 kV – IEC61000-4-2, Contact Discharge
  - $\pm$ 15 kV – IEC61000-4-2, Air-Gap Discharge

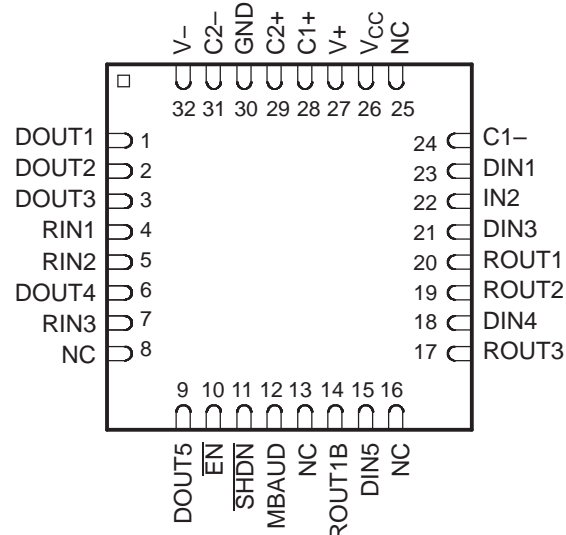
### APPLICATIONS

- Battery-Powered, Hand-Held, and Portable Equipment
- PDAs and Palmtop PCs
- Notebooks, Sub-Notebooks, and Laptops
- Digital Cameras
- Mobile Phones and Wireless Devices

DB, DW, OR PW PACKAGE  
(TOP VIEW)



QFN PACKAGE  
(TOP VIEW)



### DESCRIPTION

The MAX3237E consists of five line drivers, three line receivers, and a dual charge-pump circuit with  $\pm$ 15-kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. This device operates at data signaling rates of 250 kbit/s in normal operating mode (MBAUD = GND) and 1Mbit/s when MBAUD =  $V_{CC}$ . The driver output slew rate is a maximum of 30 V/ $\mu$ s.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

The MAX3237E transmitters are disabled and the outputs are forced into high-impedance state when the device is in shutdown mode ( $\overline{\text{SHDN}} = \text{GND}$ ) and the supply current falls to less than 1  $\mu\text{A}$ . Also, during shutdown, the onboard charge pump is disabled;  $V_+$  is lowered to  $V_{\text{CC}}$ , and  $V_-$  is raised toward GND. Receiver outputs also can be placed in the high-impedance state by setting enable (EN) high. ROUT1B remains active all the time, regardless of the EN and SHDN condition.

The MAX3237EC is characterized for operation from 0°C to 70°C. The MAX3237EI is characterized for operation from –40°C to 85°C.

#### AVAILABLE OPTIONS<sup>(1)</sup>

$T_A$	PACKAGED DEVICES <sup>(2)</sup>
0°C to 70°C	MAX3237ECDBR
	MAX3237ECPWR
	MAX3237ECRHBR (QFN package)
	MAX3237ECDWR
–40°C to 85°C	MAX3237EIDBR
	MAX3237EIPWR
	MAX3237EIRHBR (QFN package)
	MAX3237EIDWR

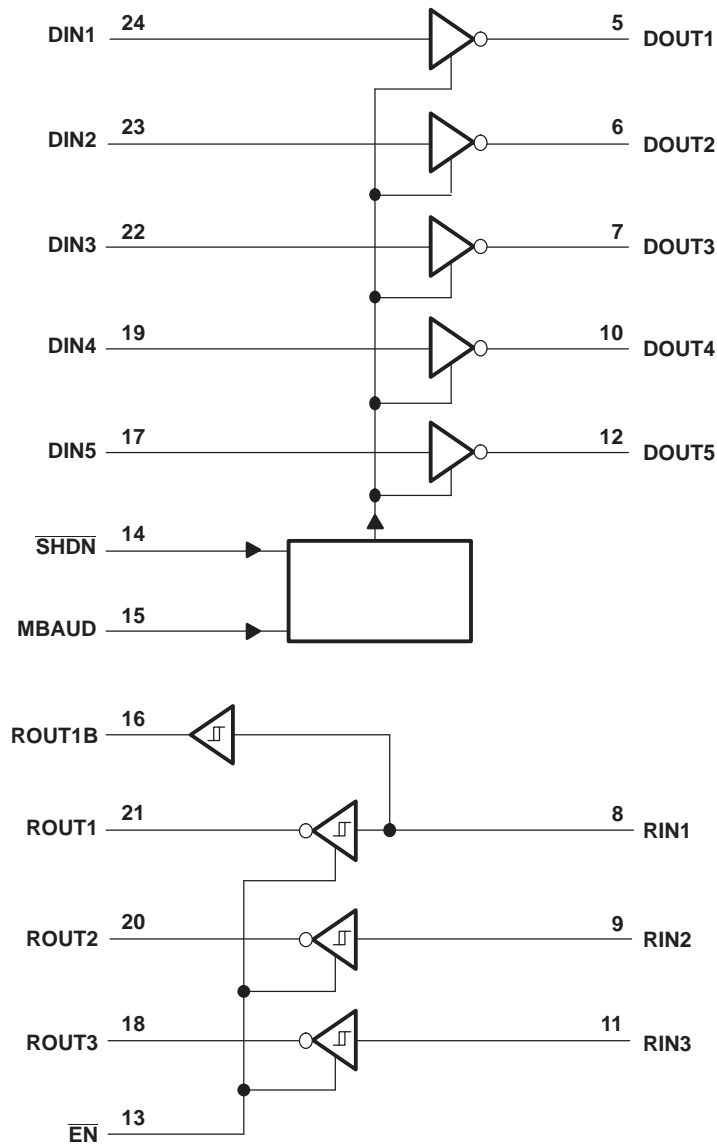
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

**Table 1. FUNCTION TABLE**

INPUTS		OUTPUTS		
$\overline{\text{SHDN}}$	$\overline{\text{EN}}$	DOUT	ROUT	ROUT1B
0	0	Z <sup>(1)</sup>	Active	Active
0	1	Z <sup>(1)</sup>	Z <sup>(1)</sup>	Active
1	0	Active	Active	Active
1	1	Active	Z <sup>(1)</sup>	Active

- (1) Z = high impedance (off)

LOGIC DIAGRAM (POSITIVE LOGIC)



## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range <sup>(2)</sup>	-0.3	6	V	
V+	Positive-output supply voltage range <sup>(2)</sup>	-0.3	7	V	
V-	Negative-output supply voltage range <sup>(2)</sup>	0.3	-7	V	
V+ – V-	Supply voltage difference <sup>(2)</sup>		13	V	
V <sub>I</sub>	Input voltage range	Driver ( $\overline{\text{SHDN}}$ , MBAUD, $\overline{\text{EN}}$ )	-0.3	6	V
		Receiver	-25	25	
V <sub>O</sub>	Output voltage range	Driver	-13.2	13.2	V
		Receiver	-0.3	V <sub>CC</sub> + 0.3	
	Short-circuit duration	DOUT to GND		Unlimited	
θ <sub>JA</sub>	Package thermal impedance <sup>(3)</sup>		62	°C/W	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

See [Figure 5](#)

		MIN	NOM	MAX	UNIT	
Supply voltage		V <sub>CC</sub> = 3.3 V	3	3.3	3.6	V
		V <sub>CC</sub> = 5 V	4.5	5	5.5	
V <sub>IH</sub>	Driver and control high-level input voltage	DIN, $\overline{\text{SHDN}}$ , MBAUD, $\overline{\text{EN}}$	V <sub>CC</sub> = 3.3 V	2	5.5	V
			V <sub>CC</sub> = 5 V	2.4	5.5	
V <sub>IL</sub>	Driver and control low-level input voltage	DIN, $\overline{\text{SHDN}}$ , MBAUD, $\overline{\text{EN}}$		0	0.8	V
V <sub>I</sub>	Receiver input voltage	-25		25	V	
T <sub>A</sub>	Operating free-air temperature	MAX3237EC	0	70	°C	
		MAX3237EI	-40	85		

- (1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3 V to 5 V.

## ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
I <sub>I</sub>	Input leakage current	DIN, $\overline{\text{SHDN}}$ , MBAUD, $\overline{\text{EN}}$		9	18	μA
I <sub>CC</sub>	Supply current (T <sub>A</sub> = 25°C)	No load, $\overline{\text{SHDN}} = V_{CC}$		0.5	2	mA
		Shutdown supply current	$\overline{\text{SHDN}} = \text{GND}$	1	10	μA
		$\overline{\text{SHDN}} = \text{RIN} = \text{GND}$ , DIN = GND or V <sub>CC</sub>		10	300	nA

- (1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3 V to 5 V.
- (2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## DRIVER SECTION ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	DOUT at R <sub>L</sub> = 3 kΩ to GND,	DIN = GND	5	5.4		V
V <sub>OL</sub>	Low-level output voltage	DOUT at R <sub>L</sub> = 3 kΩ to GND,	DIN = V <sub>CC</sub>	-5	-5.4		V
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = V <sub>CC</sub>			±0.01	±1	μA
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> at GND			±0.01	±1	μA
I <sub>OS</sub>	Short-circuit output current <sup>(3)</sup>	V <sub>CC</sub> = 3.6 V or 3.3 V,	V <sub>O</sub> = 0 V			±60	mA
r <sub>o</sub>	Output resistance	V <sub>CC</sub> , V+, and V- = 0 V,	V <sub>O</sub> = ±2 V	300	50k		Ω

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3 V to 5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

## DRIVER SECTION SWITCHING CHARACTERISTICS<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(2)</sup>	MAX	UNIT
Maximum data rate	C <sub>L</sub> = 1000 pF, MBAUD = GND	R <sub>L</sub> = 3 kΩ, 1 DIN switching, See <a href="#">Figure 1</a>		250			kbit/s
	C <sub>L</sub> = 1000 pF, V <sub>CC</sub> = 4.5 V to 5.5 V, MBAUD = V <sub>CC</sub>			1000			
	C <sub>L</sub> = 250 pF, V <sub>CC</sub> = 3 V to 4.5 V, MBAUD = V <sub>CC</sub>			1000			
t <sub>sk(p)</sub>	Pulse skew <sup>(3)</sup>	C <sub>L</sub> = 150 pF to 2500 pF, R <sub>L</sub> = 3 kΩ to 7 kΩ, MBAUD = V <sub>CC</sub> or GND, See <a href="#">Figure 2</a>			100		ns
SR(tr)	Slew rate, transition region (see <a href="#">Figure 1</a> )	V <sub>CC</sub> = 3.3 V, R <sub>L</sub> = 3 kΩ to 7 kΩ, T <sub>A</sub> = 25°C	C <sub>L</sub> = 150 pF to 1000 pF	MBAUD = GND	6	30	V/μs
				MBAUD = V <sub>CC</sub>	24	150	
			C <sub>L</sub> = 150 pF to 2500 pF,	MBAUD = GND	4	30	

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3 V to 5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

## RECEIVER SECTION ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -1 mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.1		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 1 mA			0.4	V
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 3.3 V		1.5	2.4	V
		V <sub>CC</sub> = 5 V		2	2.4	
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>CC</sub> = 3.3 V	0.6	1.1		V
		V <sub>CC</sub> = 5 V	0.8	1.5		
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )			0.5		V
I <sub>oz</sub>	Output leakage current	$\overline{\text{EN}} = V_{\text{CC}}$		±0.05	±10	µA
r <sub>i</sub>	Input resistance	V <sub>i</sub> = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 mF at V<sub>CC</sub> = 3 V to 5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## RECEIVER SECTION SWITCHING CHARACTERISTICS<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP <sup>(2)</sup>	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	C <sub>L</sub> = 150 pF, See <a href="#">Figure 3</a>	150	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output	C <sub>L</sub> = 150 pF, See <a href="#">Figure 3</a>	150	ns
t <sub>en</sub>	Output enable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See <a href="#">Figure 4</a>	2.6	µs
t <sub>dis</sub>	Output disable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See <a href="#">Figure 4</a>	2.4	µs
t <sub>sk(p)</sub>	Pulse skew <sup>(3)</sup>	See <a href="#">Figure 3</a>	50	ns

(1) Test conditions are C1–C4 = 0.1 µF at V<sub>CC</sub> = 3 V to 5 V.

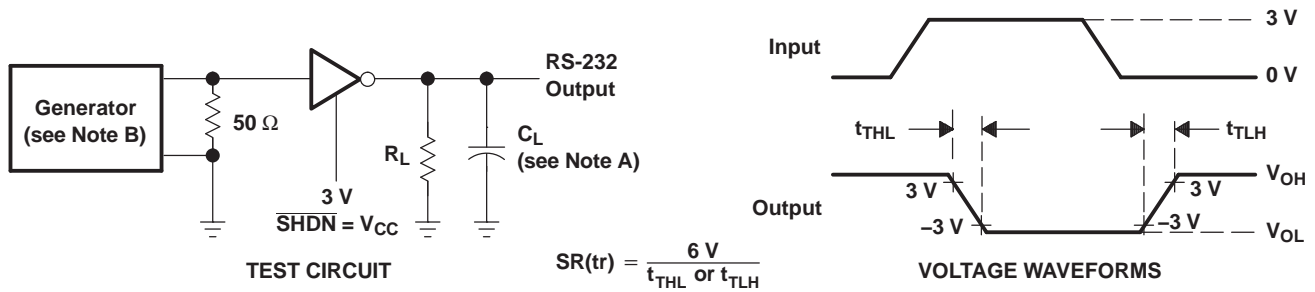
(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> - t<sub>PHL</sub>| of each channel of the same device.

## ESD PROTECTION

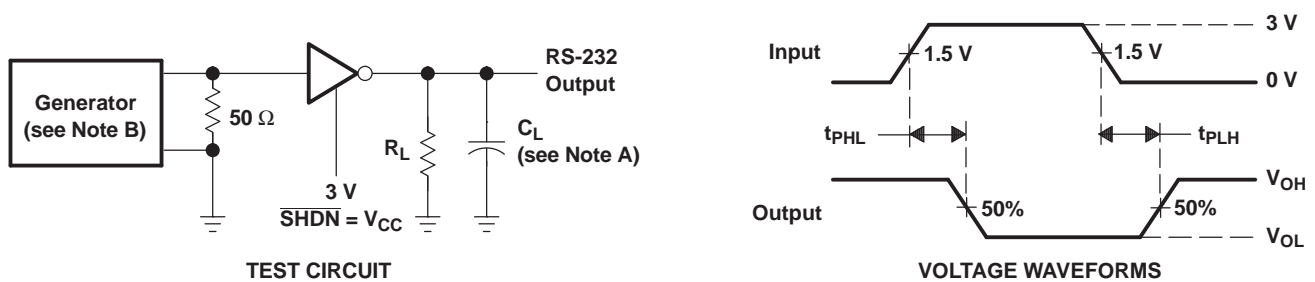
PIN	TEST CONDITIONS	TYP	UNIT
DOUT, RIN	HBM	±15	kV
	IEC61000-4-2, Contact Discharge	±8	
	IEC61000-4-2, Air-Gap Discharge	±15	

PARAMETER MEASUREMENT INFORMATION



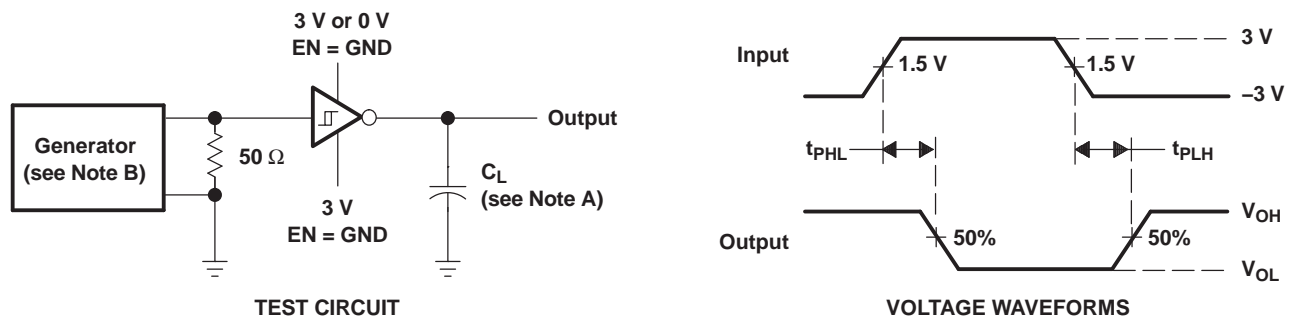
NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

Figure 1. Driver Slew Rate



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

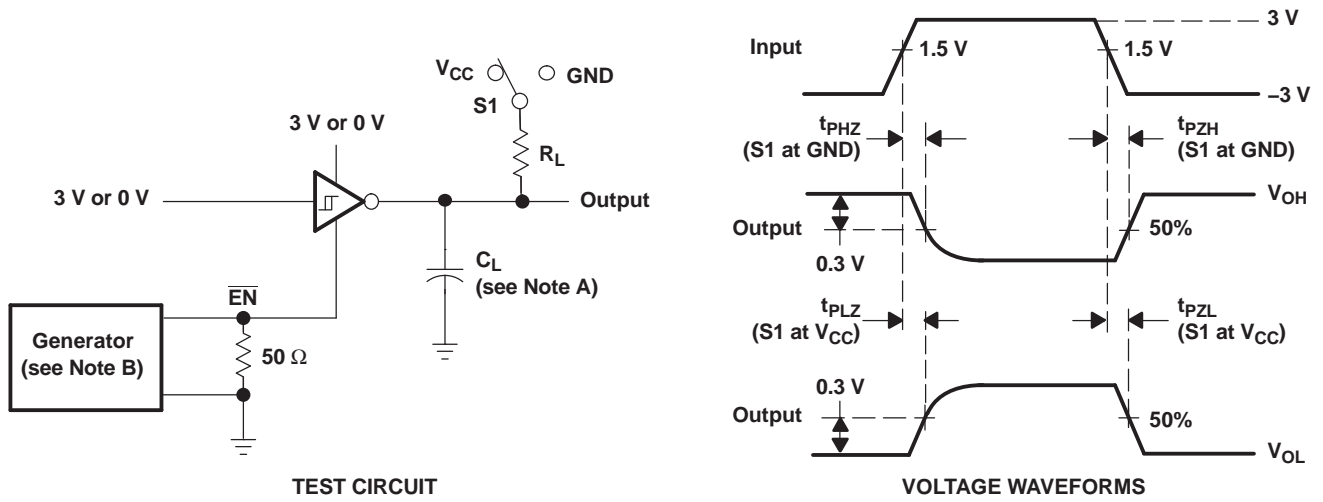
Figure 2. Driver Pulse Skew



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

Figure 3. Receiver Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION (continued)

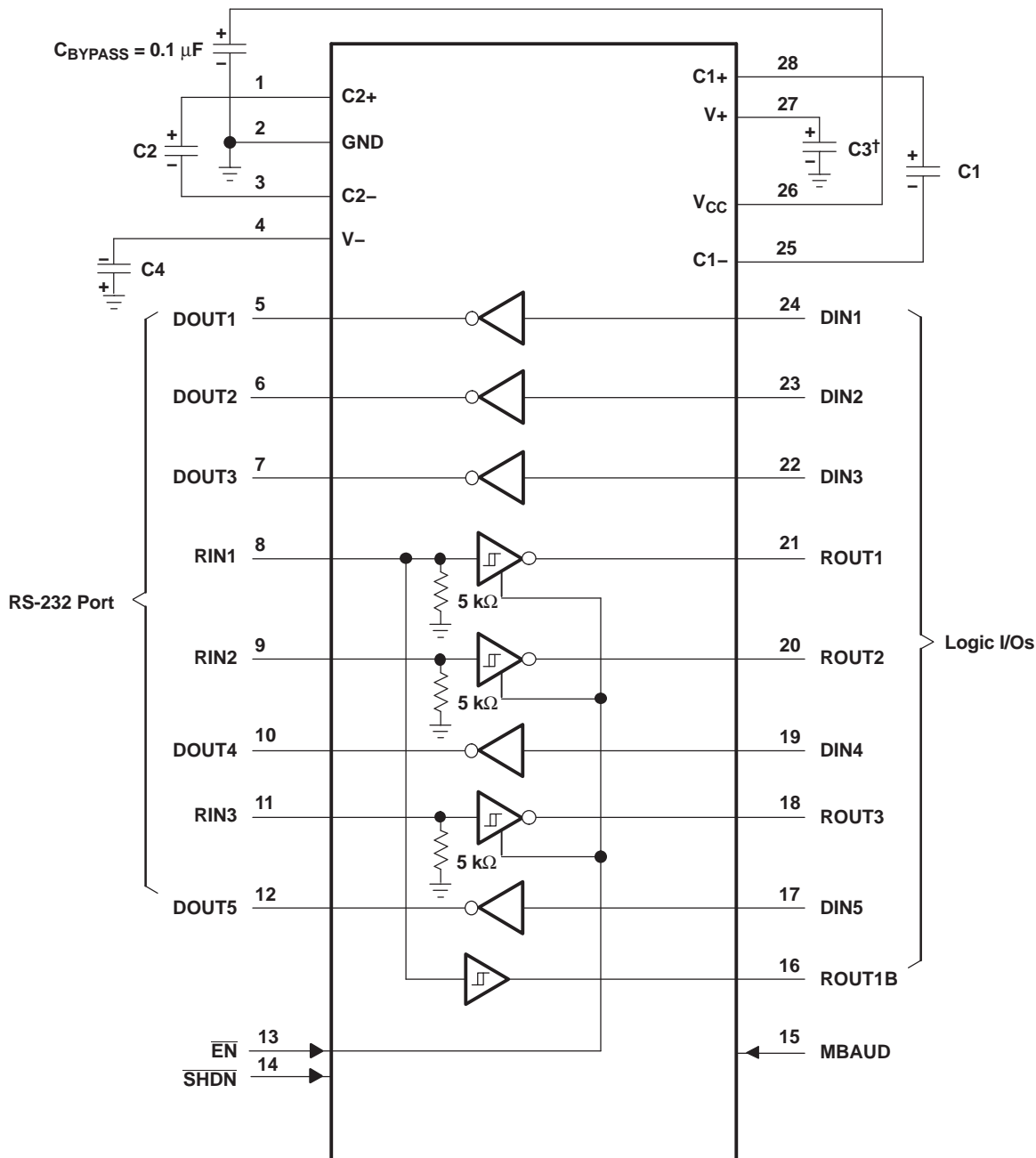


- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .  
 C.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 D.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

Figure 4. Receiver Enable and Disable Times



APPLICATION INFORMATION



† C3 can be connected to V<sub>CC</sub> or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V<sub>CC</sub> vs CAPACITOR VALUES

V <sub>CC</sub>	C1	C2, C3, and C4
3.3 V ± 0.15 V	0.1 μF	0.1 μF
3.3 V ± 0.3 V	0.22 μF	0.22 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.22 μF	1 μF

Figure 5. Typical Operating Circuit and Capacitor Values

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3237ECDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3237EC	<a href="#">Samples</a>
MAX3237ECDW	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3237EC	<a href="#">Samples</a>
MAX3237ECDWG4	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3237EC	<a href="#">Samples</a>
MAX3237ECDWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3237EC	<a href="#">Samples</a>
MAX3237ECPWR	NRND	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP237EC	
MAX3237EIDB	NRND	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3237EI	
MAX3237EIDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3237EI	<a href="#">Samples</a>
MAX3237EIDW	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3237EI	<a href="#">Samples</a>
MAX3237EIPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP237EI	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3237ECDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
MAX3237ECDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
MAX3237ECPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MAX3237EIDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
MAX3237EIPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3237ECDBR	SSOP	DB	28	2000	356.0	356.0	35.0
MAX3237ECDWR	SOIC	DW	28	1000	350.0	350.0	66.0
MAX3237ECPWR	TSSOP	PW	28	2000	356.0	356.0	35.0
MAX3237EIDBR	SSOP	DB	28	2000	356.0	356.0	35.0
MAX3237EIPWR	TSSOP	PW	28	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
MAX3237ECDW	DW	SOIC	28	20	506.98	12.7	4826	6.6
MAX3237ECDWG4	DW	SOIC	28	20	506.98	12.7	4826	6.6
MAX3237EIDB	DB	SSOP	28	50	530	10.5	4000	4.1
MAX3237EIDW	DW	SOIC	28	20	506.98	12.7	4826	6.6

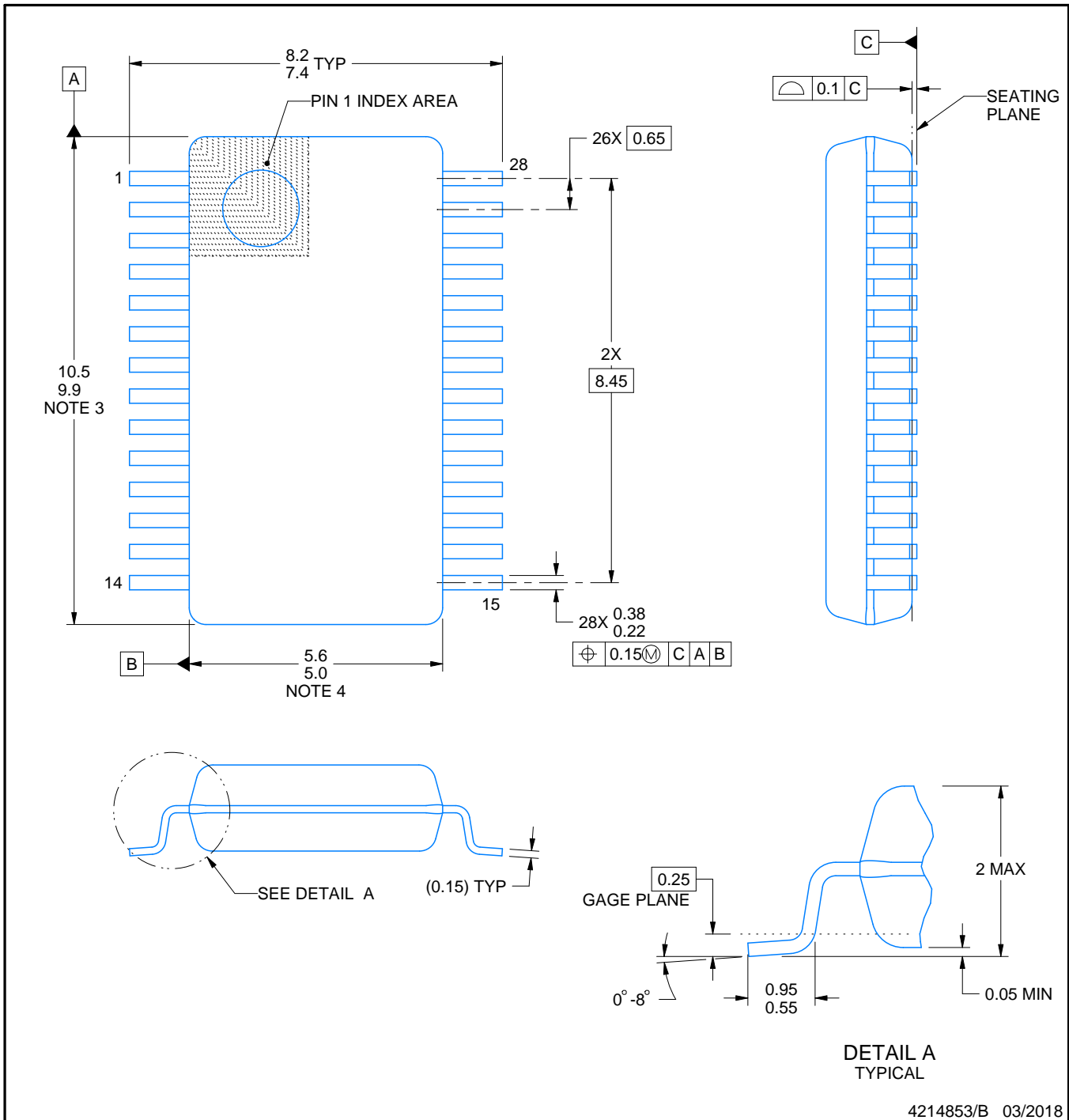
# DB0028A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214853/B 03/2018

### NOTES:

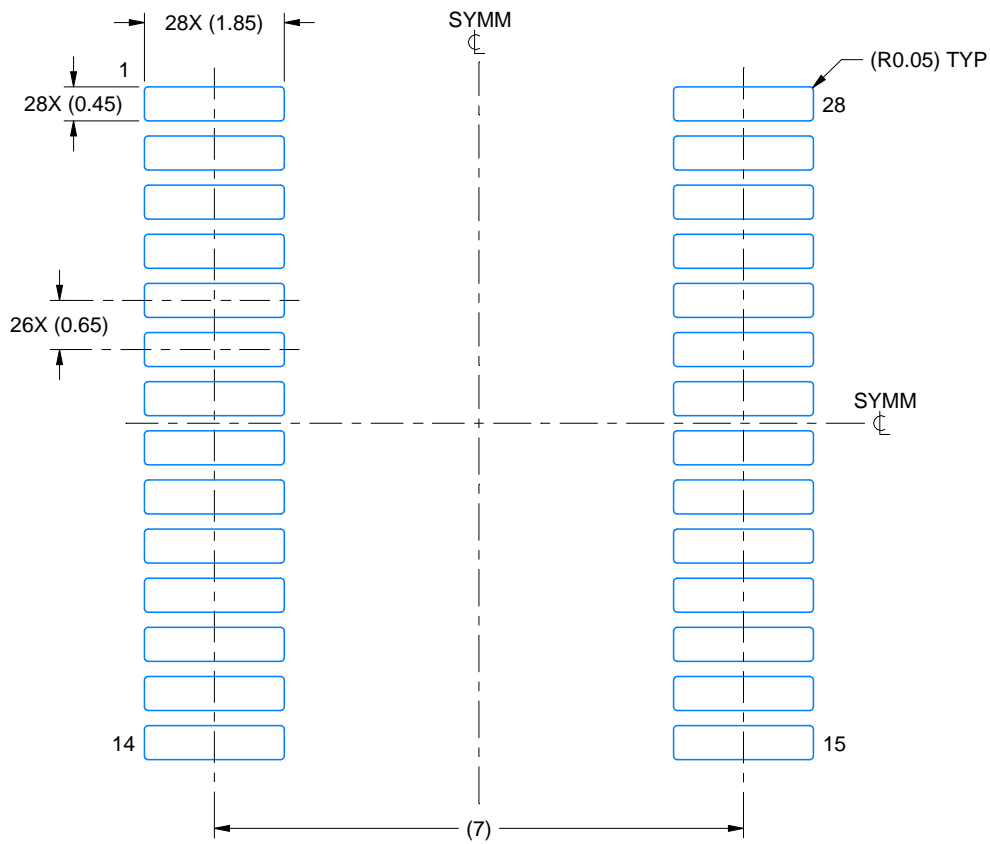
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

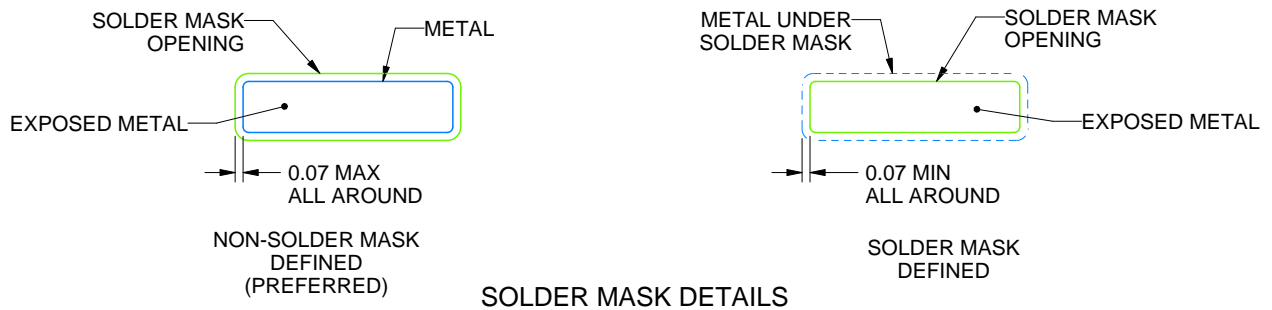
DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214853/B 03/2018

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

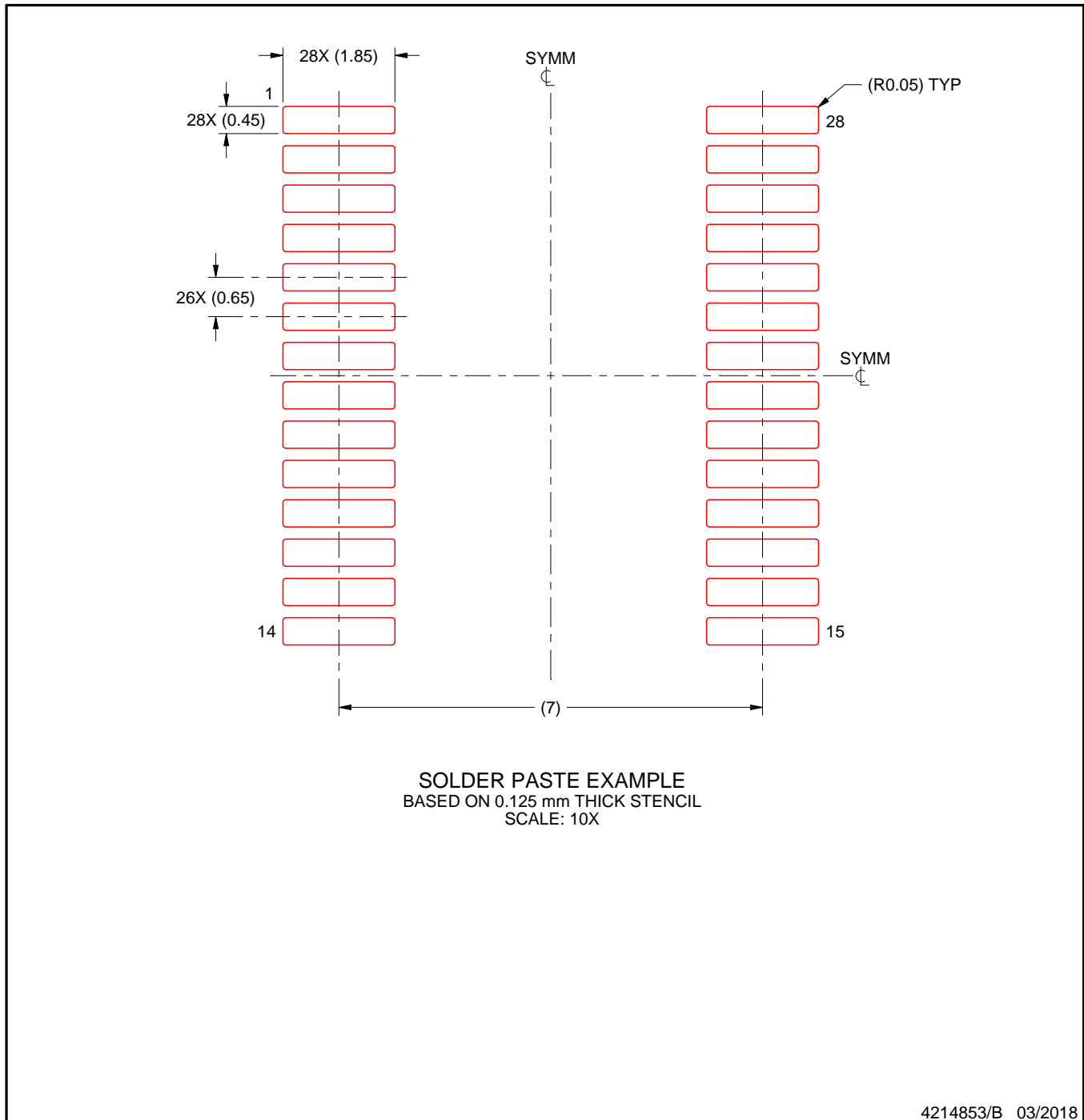


# EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

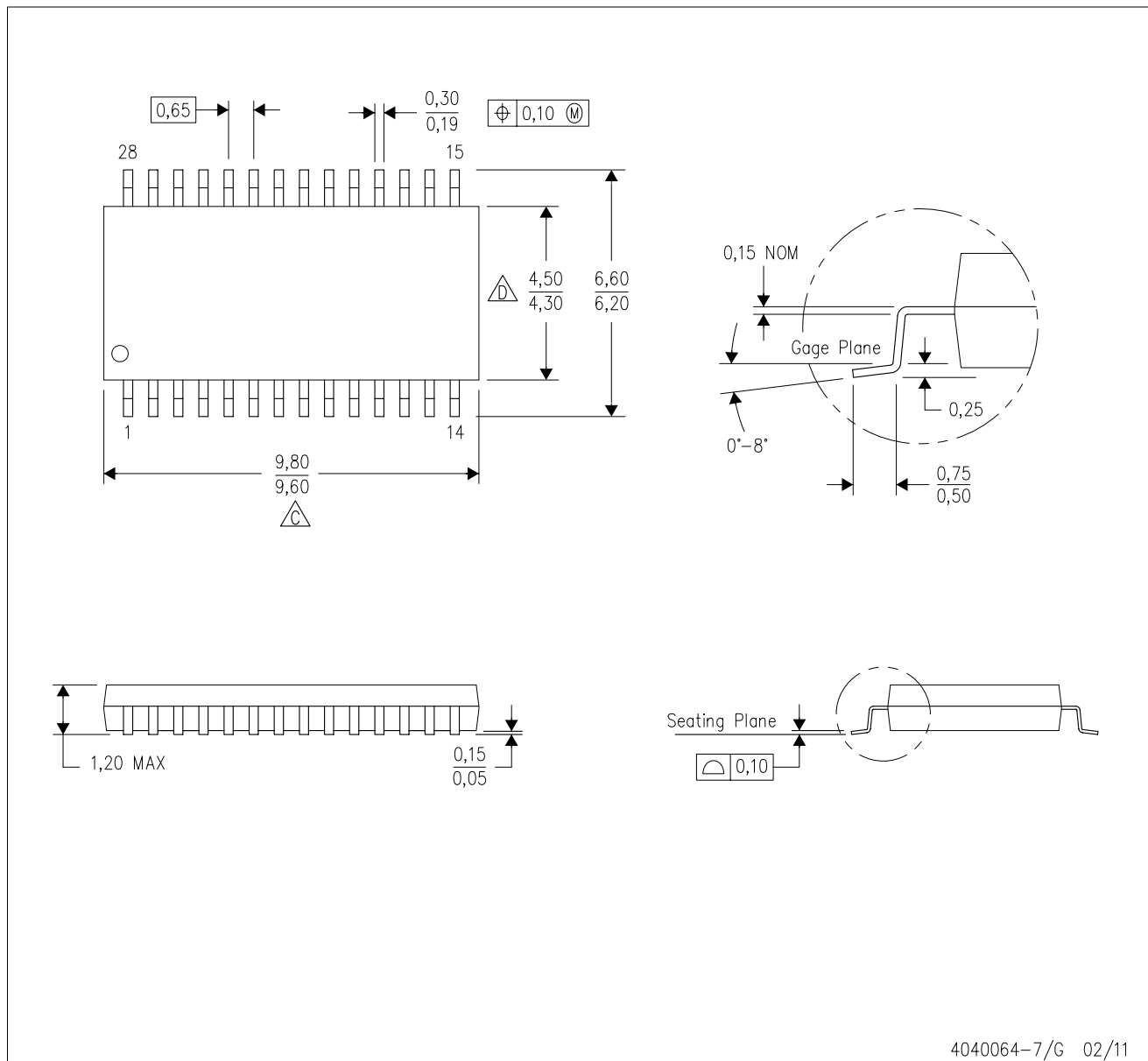


- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AE.

# MECHANICAL DATA

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate design.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated