TEXAS INSTRUMENTS

LMV651, LMV652, LMV654

SNOSAI7K – SEPTEMBER 2005 – REVISED MAY 2016

LMV65x 12-MHz, Low Voltage, Low Power Amplifiers

1 Features

- Typical 5-V Supply, Unless Otherwise Noted
- Specified 3-V and 5-V Performance
- Low Power Supply Current
  - LMV651: 116 µA
  - LMV652: 118 µA per Amplifier
  - LMV654: 122 µA per Amplifier
- High Unity-Gain Bandwidth: 12 MHz
- Maximum Input Offset Voltage: 1.5 mV
- CMRR: 100 dB
- PSRR: 95 dB
- Input Referred Voltage Noise: 17 nV/$\sqrt{\text{Hz}}$
- Output Swing With 2-kΩ Load, 120 mV from Rail
- Total Harmonic Distortion: 0.003% at 1 kHz, 2 kΩ
- Temperature Range: −40°C to 125°C

2 Applications

- Portable Equipment
- Automotive
- Battery-Powered Systems
- Sensors and Instrumentation

3 Description

TI's LMV65x devices are high-performance, low-power operational amplifier ICs implemented with TI's advanced VIP50 process. This family of parts features 12 MHz of bandwidth while consuming only 116 µA of current, which is an exceptional bandwidth to power ratio in this operational amplifier class. The LMV65x devices are unity-gain stable and provide an excellent solution for general-purpose amplification in low-voltage, low-power applications.

This family of low-voltage, low-power amplifiers provides superior performance and economy in terms of power and space usage. These operational amplifiers have a maximum input offset voltage of 1.5 mV, a rail-to-rail output stage, and an input common-mode voltage range that includes ground. The LMV65x provide a PSRR of 95 dB, a CMRR of 100 dB, and a total harmonic distortion (THD) of 0.003% at 1-kHz frequency and 2-kΩ load.

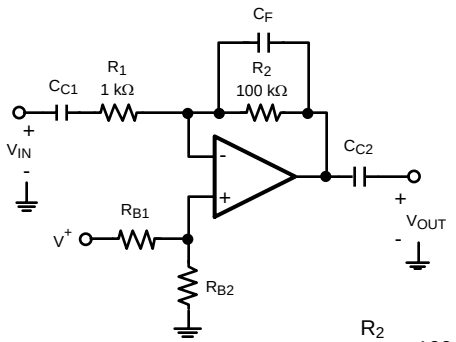
The operating supply voltage range for this family of parts is from 2.7 V and 5.5 V. These operational amplifiers can operate over a wide temperature range (−40°C to 125°C), making them ideal for automotive applications, sensor applications, and portable equipment applications. The LMV651 is offered in the ultra-tiny 5-pin SC70 and 5-pin SOT-23 package. The LMV652 is offered in an 8-pin VSSOP package. The LMV654 is offered in a 14-pin TSSOP package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV651	SOT-23 (5)	2.90 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm
LMV652	VSSOP (8)	3.00 mm × 3.00 mm
LMV654	TSSOP (14)	5.00 mm × 4.40 mm

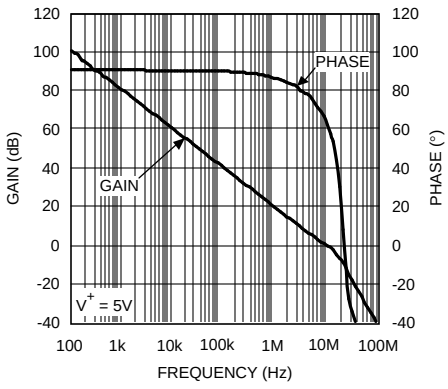
(1) For all available packages, see the orderable addendum at the end of the data sheet.

High Gain Wide Bandwidth Inverting Amplifier



$$A_V = -\frac{R_2}{R_1} = -100$$

Open-Loop Gain and Phase vs Frequency



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (March 2013) to Revision K **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision I (March 2012) to Revision J **Page**

- Changed layout of National Data Sheet to TI format ... 18

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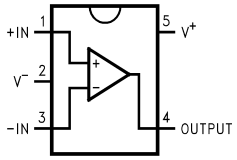
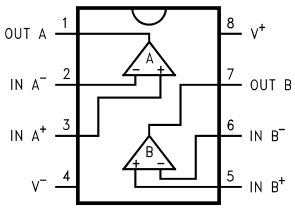
5 Pin Configuration and Functions

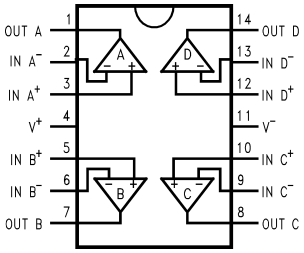
LMV651 DBV or DCK Package
5-Pin SC70 or SOT-23
Top View



LMV652 DGK Package
8-Pin VSSOP
Top View



LMV654 PW Package
14-Pin TSSOP
Top View



Pin Functions: LMV651

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN	3	I	Inverting Input
+IN	1	I	Noninverting Input
OUT	4	O	Output
V–	2	P	Negative supply input
V+	5	P	Positive Supply Input

Pin Functions: LMV652, LMV654

PIN			I/O	DESCRIPTION
NAME	VSSOP	TSSOP		
–IN A	2	2	I	Inverting input, channel A
+IN A	3	3	I	Noninverting input, channel A
–IN B	6	6	I	Inverting input, channel B
+IN B	5	5	I	Noninverting input, channel B
–IN C	—	9	I	Inverting input, channel C
+IN C	—	10	I	Noninverting input, channel C
–IN D	—	13	I	Inverting input, channel D
+IN D	—	12	I	Noninverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	—	8	O	Output, channel C
OUT D	—	14	O	Output, channel D
V–	4	11	P	Negative (lowest) power supply
V+	8	4	P	Positive (highest) power supply

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6 Specifications

6.1 Absolute Maximum Ratings[1][2]

		MIN	MAX	UNIT
Differential input V_{ID}			±0.3	
Supply voltage ($V_S = V^+ - V^-$)			6	
Input or output pin voltage		V^- − 0.3	V^+ + 0.3	V
Soldering information	Infrared or convection (20 sec)		235	°C
	Wave soldering lead temperature (10 sec)		260	
Junction temperature[3]			150	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)[1]	±2000	V
		Machine model[2]	±100	

(1) Human Body Model, applicable std. MIL-STD-883, Method 3015.7
(2) Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Temperature	−40	125	°C
Supply voltage	2.7	5.5	V

6.4 Thermal Information

THERMAL METRIC[1]		LMV651		LMV652	LMV653	UNIT
		DCK (SC70)	DBV (SOT-23)	DGK (VSSOP)	PW (TSSOP)	
		5 PINS	5 PINS	8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	303.5	214.2	200.3	134.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	135.5	173.3	89.1	60.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	81.1	72.5	120.9	77.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.4	56.7	21.7	11.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80.4	71.9	119.4	76.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 3-V DC Electrical Characteristics

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 3 V, V^- = 0 V, V_O = V_{CM} = V^+/2, and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input offset voltage				0.1	±1.5	mV
		Over specified temperature range				2.7	
TC V_{OS}	Input offset average drift				6.6		µV/°C
I_B	Input bias current(3)				80	120	nA
I_{OS}	Input offset current				2.2	15	nA
CMRR	Common-mode rejection ratio	0 ≤ V_{CM}≤ 2 V		87	100		dB
			Over specified temperature range	80			
PSRR	Power supply rejection ratio	3 ≤ V^+ ≤ 5 V, V_{CM} = 0.5		87	95		dB
			Over specified temperature range	81			
		2.7 ≤ V^+ ≤ 5.5 V, V_{CM} = 0.5		87	95		
			Over specified temperature range	81			
CMVR	Input common-mode voltage range	CMRR ≥ 75 dB		0		2.1	V
		CMRR ≥ 60 dB, over specified temperature range		0		2.1	
A_{VOL}	Large signal voltage gain	0.3 ≤ V_O ≤ 2.7, R_L = 2 kΩ to V^+/2		80	85		dB
		0.4 ≤ V_O ≤ 2.6, R_L = 2 kΩ to V^+/2, over specified temperature range		76			
		0.3 ≤ V_O ≤ 2.7, R_L = 10 kΩ to V^+/2		86	93		
		0.4 ≤ V_O ≤ 2.6, R_L = 10 kΩ to V^+/2, over specified temperature range		83			
V_O	Output swing high	R_L = 2 kΩ to V^+/2			80	95	mV from rail
			Over specified temperature range			120	
		R_L = 10 kΩ to V^+/2			45	50	
			Over specified temperature range			60	
	Output swing low	R_L = 2 kΩ to V^+/2			95	110	
			Over specified temperature range			125	
		R_L = 10 kΩ to V^+/2			60	65	
			Over specified temperature range			75	
I_{SC}	Maximum continuous output current	Sourcing(4)			17		mA
		Sinking(4)			25		
I_S	Supply current per amplifier	LMV651			115	140	µA
			Over specified temperature range			175	
		LMV652			118	140	
			Over specified temperature range			175	
		LMV654			122	140	
			Over specified temperature range			175	
SR	Slew rate	A_V = +1, 10% to 90%(5)			3.0		V/µs
GBW	Gain bandwidth product				12		MHz
e_n	Input-referred voltage noise	f = 100 kHz			17		nV/√Hz
		f = 1 kHz			17		
i_n	Input-referred current noise	f = 100 kHz			0.1		pA/√Hz
		f = 1 kHz			0.15		
THD	Total harmonic distortion	f = 1 kHz, A_V = 2, R_L = 2 kΩ			0.003%		

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) Positive current corresponds to current flowing into the device.
(4) Slew rate is the average of the rising and falling slew rates.
(5) The part is not short-circuit protected and is not recommended for operation with low resistive loads. Typical sourcing and sinking output current curves are provided in *Typical Characteristics* and should be consulted before designing for heavy loads.

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6.6 5-V DC Electrical Characteristics

Unless otherwise specified, all limits are specified for T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_O = V_{CM} = V^+/2, and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input offset voltage				0.1	±1.5	mV
		Over specified temperature range				2.7	
TC V_{OS}	Input offset average drift				6.6		µV/°C
I_B	Input bias current	See(3)			80	120	nA
I_{OS}	Input offset current				2.2	15	nA
CMRR	Common-mode rejection ratio	0 ≤ V_{CM}≤ 4 V		90	100		dB
			Over specified temperature range	83			
PSRR	Power supply rejection ratio	3 V ≤ V^+ ≤ 5 V, V_{CM} = 0.5 V		87	95		dB
			Over specified temperature range	81			
		2.7 V ≤ V^+ ≤ 5.5 V, V_{CM} = 0.5 V		87	95		
			Over specified temperature range	81			
CMVR	Input common-mode voltage range	CMRR ≥ 80 dB		0		4.1	V
		CMRR ≥ 68 dB, over specified temperature range		0		4.1	
A_{VOL}	Large signal voltage gain	0.3 ≤ V_O ≤ 4.7 V, R_L = 2 kΩ to V^+/2		79	84		dB
		0.4 ≤ V_O ≤ 4.6 V, R_L = 2 kΩ to V^+/2, over specified temperature range		76			
		0.3 ≤ V_O ≤ 4.7 V, R_L = 10 kΩ to V^+/2		87	94		
		0.4 ≤ V_O ≤ 4.6 V, R_L = 10 kΩ to V^+/2, over specified temperature range		84			
V_O	Output swing high	R_L = 2 kΩ to V^+/2			120	140	mV from rail
			Over specified temperature range			185	
		R_L = 10 kΩ to V^+/2			75	90	
			Over specified temperature range			120	
	Output swing low	R_L = 2 kΩ to V^+/2			110	130	
			Over specified temperature range			150	
		R_L = 10 kΩ to V^+/2			70	80	
			Over specified temperature range			95	
I_{SC}	Maximum continuous output current	Sourcing(4)			18.5		mA
		Sinking(4)			25		
I_S	Supply current per amplifier	LMV651			116	140	µA
			Over specified temperature range			175	
		LMV652			118	140	
			Over specified temperature range			175	
		LMV654			122	140	
			Over specified temperature range			175	
SR	Slew rate	A_V = +1, V_O = 1 V_{PP}, 10% to 90%(5)			3.0		V/µs
GBW	Gain bandwidth product				12		MHz
e_n	Input-referred voltage noise	f = 100 kHz			17		nV/√Hz
		f = 1 kHz			17		
i_n	Input-referred current noise	f = 100 kHz			0.1		pA/√Hz
		f = 1 kHz			0.15		
THD	Total harmonic distortion	f = 1 kHz, A_V = 2, R_L = 2 kΩ			0.003%		

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) Positive current corresponds to current flowing into the device.
(4) The part is not short-circuit protected and is not recommended for operation with low resistive loads. Typical sourcing and sinking output current curves are provided in *Typical Characteristics* and should be consulted before designing for heavy loads.
(5) Slew rate is the average of the rising and falling slew rates.

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6.7 Typical Characteristics

Unless otherwise specified, T_A= 25°C, V_S= 5 V, V^+= 5 V, V^-= 0 V, V_{CM}= V_S/2

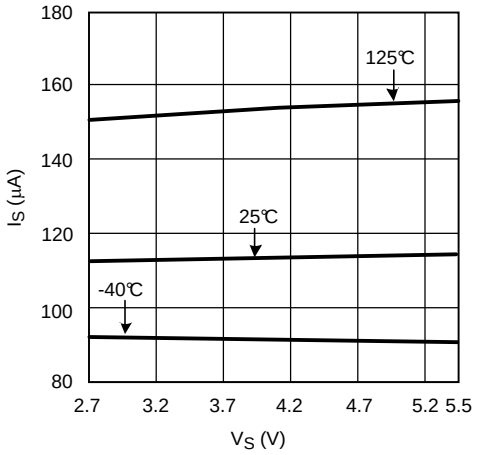

Figure 1. Supply Current vs Supply Voltage (LMV651)

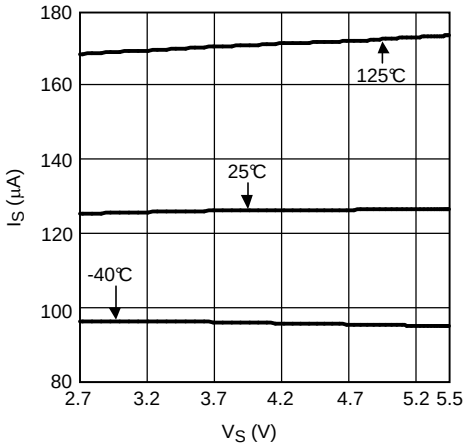

Figure 2. Supply Current per Channel vs Supply Voltage (LMV652)

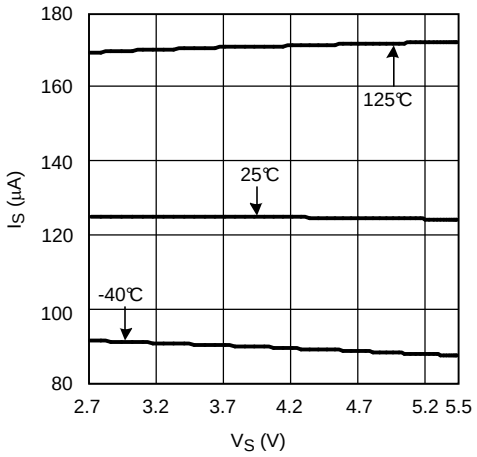

Figure 3. Supply Current per Channel vs Supply Voltage (LMV654)

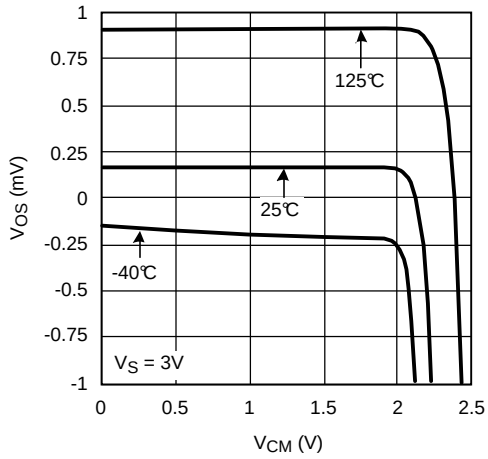

Figure 4. V_{OS} vs V_{CM}

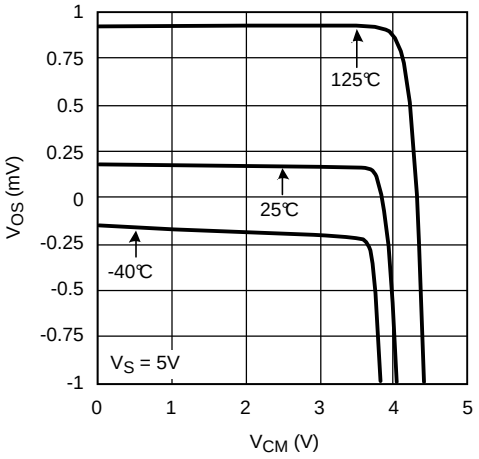

Figure 5. V_{OS} vs V_{CM}

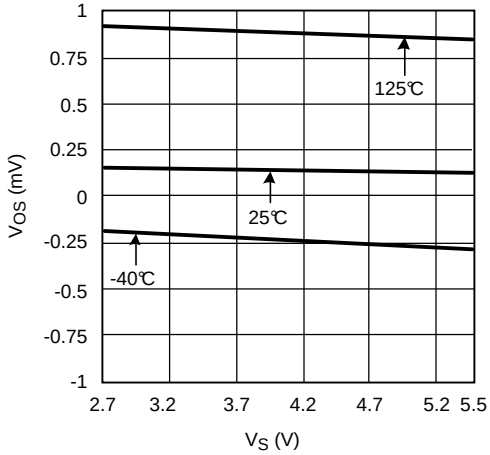

Figure 6. V_{OS} vs Supply Voltage

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Typical Characteristics (continued)

Unless otherwise specified, T_A= 25°C, V_S= 5 V, V^+= 5 V, V^-= 0 V, V_{CM}= V_S/2

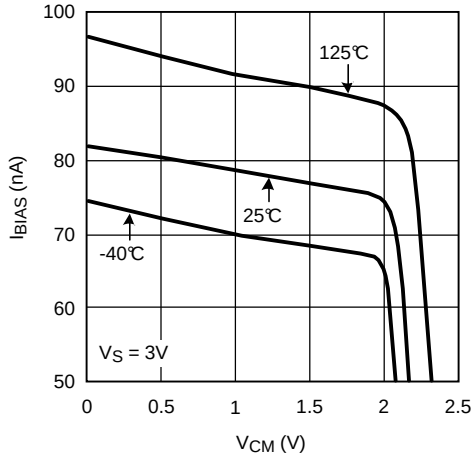

Figure 7. I_{BIAS} vs V_{CM}

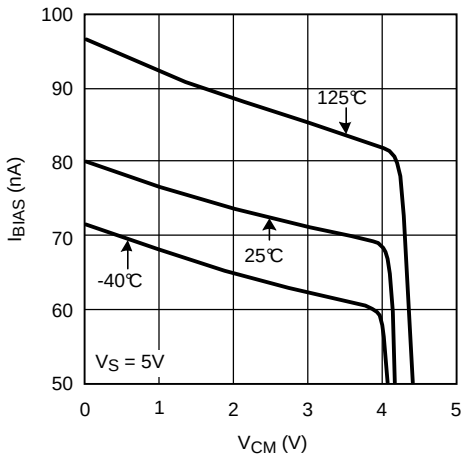

Figure 8. I_{BIAS} vs V_{CM}

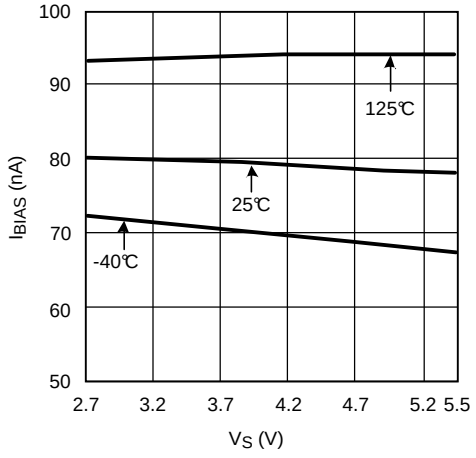

Figure 9. I_{BIAS} vs Supply Voltage

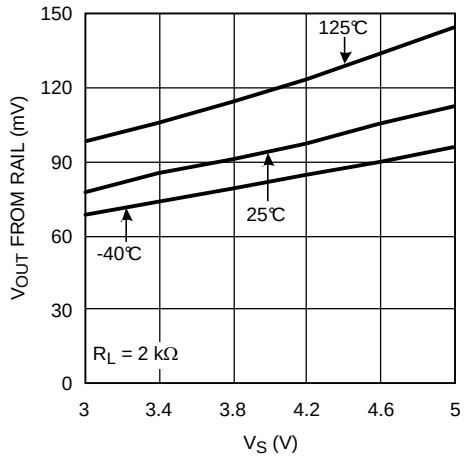

Figure 10. Positive Output Swing vs Supply Voltage

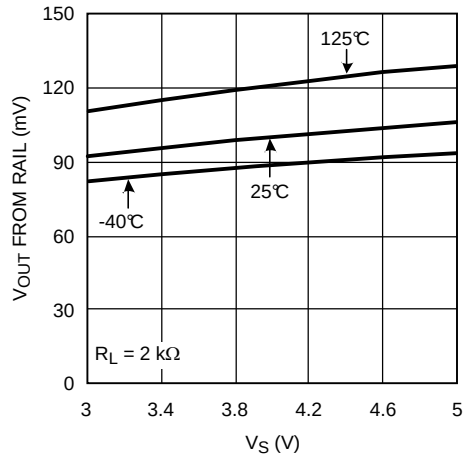

Figure 11. Negative Output Swing vs Supply Voltage

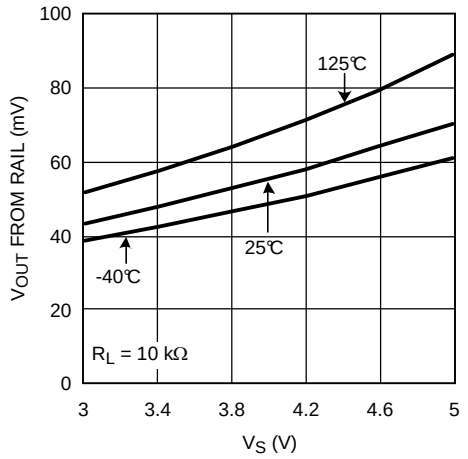

Figure 12. Positive Output Swing vs Supply Voltage

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Typical Characteristics (continued)

Unless otherwise specified, T_A= 25°C, V_S= 5 V, V^+= 5 V, V^-= 0 V, V_{CM}= V_S/2

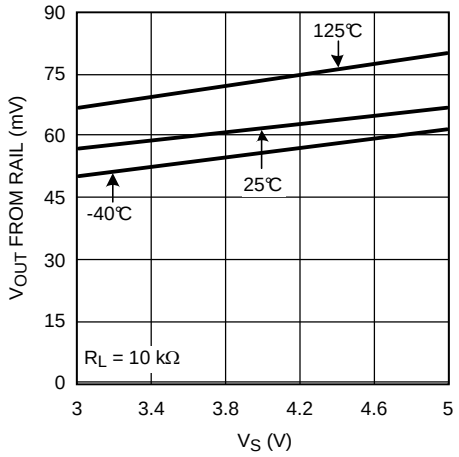

Figure 13. Negative Output Swing vs Supply Voltage

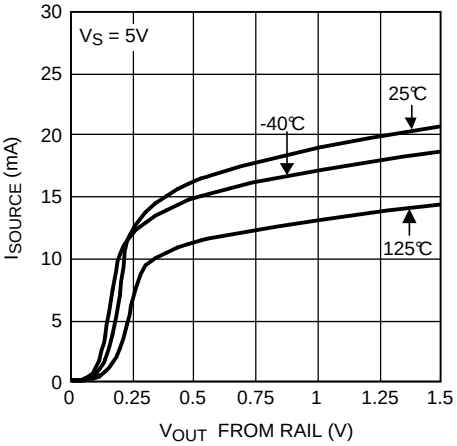

Figure 14. Sourcing Current vs Output Voltage

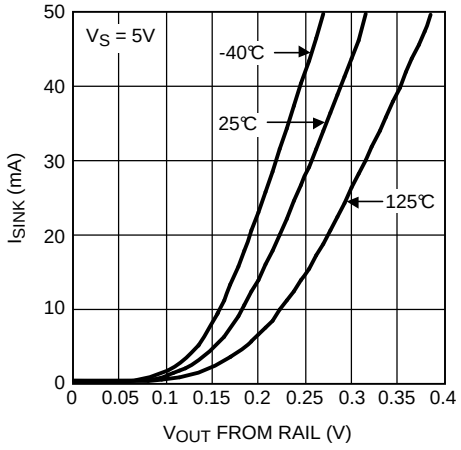

Figure 15. Sinking Current vs Output Voltage (LMV651)

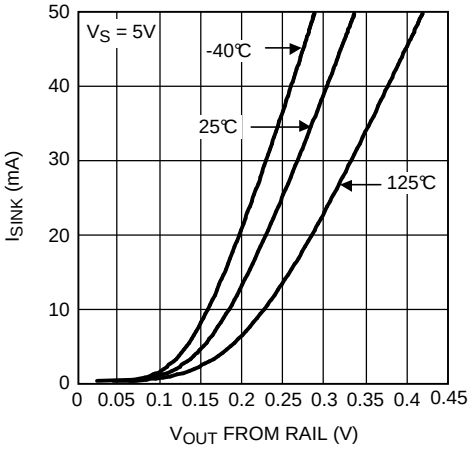

Figure 16. Sinking Current vs Output Voltage (LMV652)

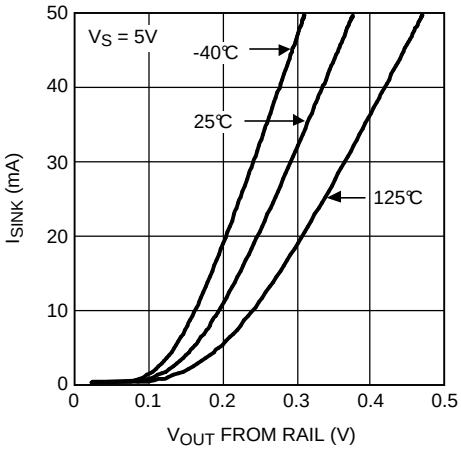

Figure 17. Sinking Current vs Output Voltage (LMV654)

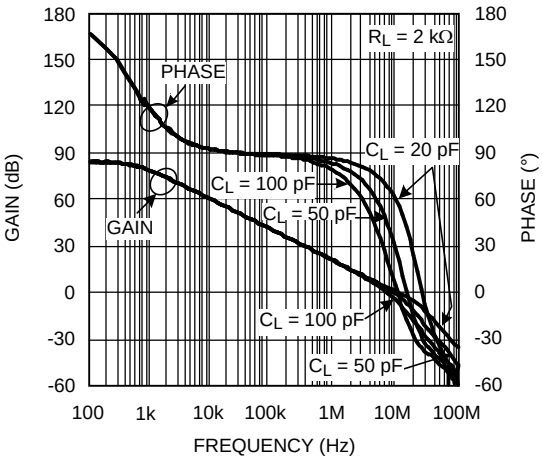

Figure 18. Open-Loop Gain and Phase With Capacitive Load

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Typical Characteristics (continued)

Unless otherwise specified, T_A= 25°C, V_S= 5 V, V^+= 5 V, V^-= 0 V, V_{CM}= V_S/2

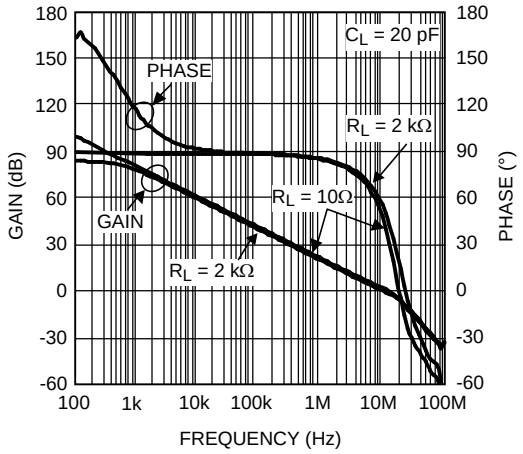

Figure 19. Open-Loop Gain and Phase With Resistive Load

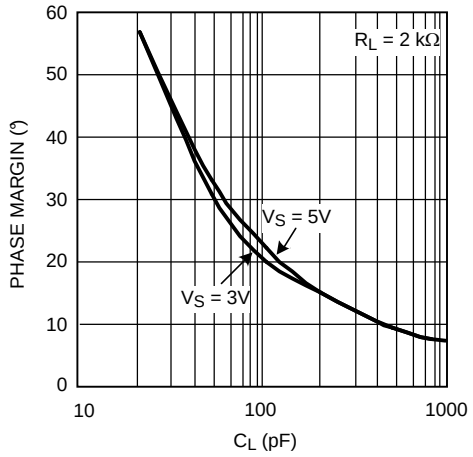

Figure 20. Phase Margin vs Capacitive Load (Stability)

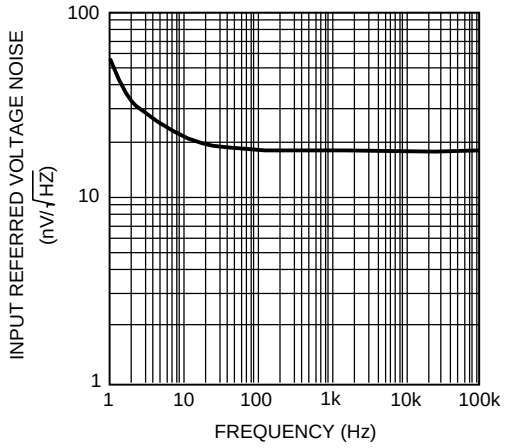

Figure 21. Input-Referred Voltage Noise vs Frequency

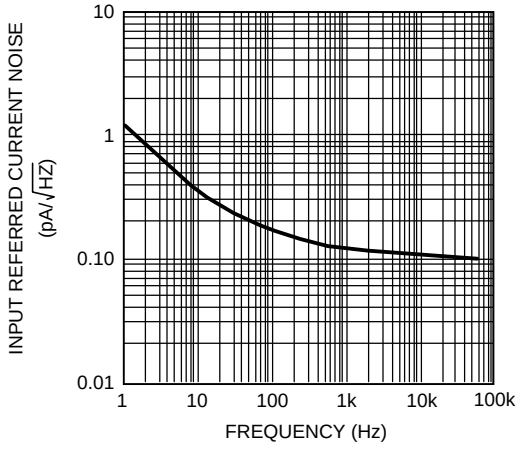

Figure 22. Input-Referred Current Noise vs Frequency

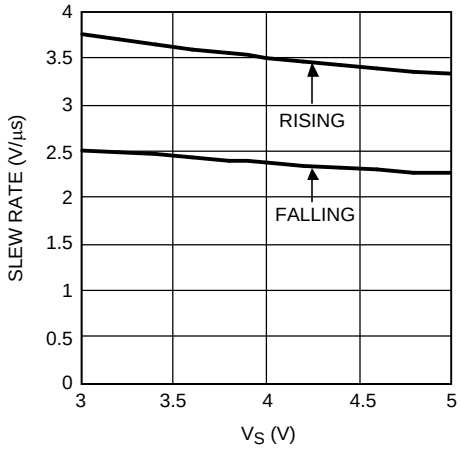

Figure 23. Slew Rate vs Supply Voltage

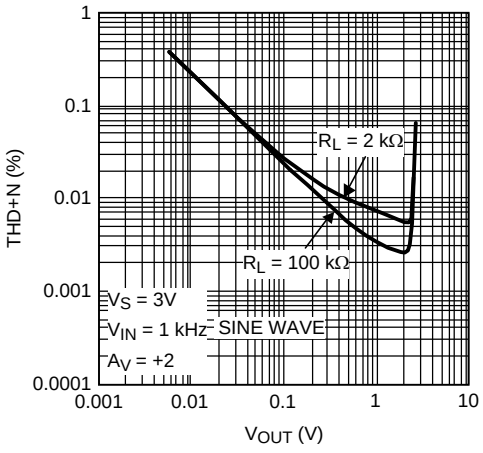

Figure 24. THD+N vs V_{OUT}

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Typical Characteristics (continued)

Unless otherwise specified, T_A= 25°C, V_S= 5 V, V^+= 5 V, V^-= 0 V, V_{CM}= V_S/2

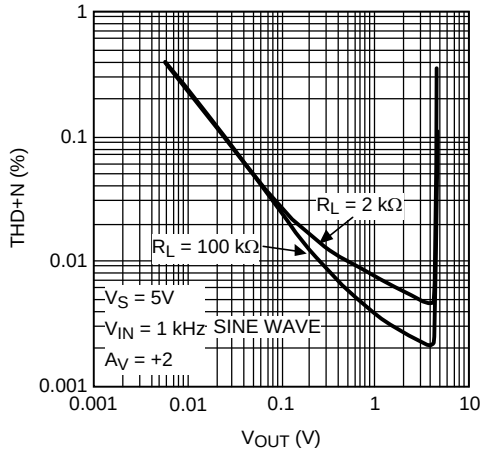

Figure 25. THD+N vs V_{OUT}

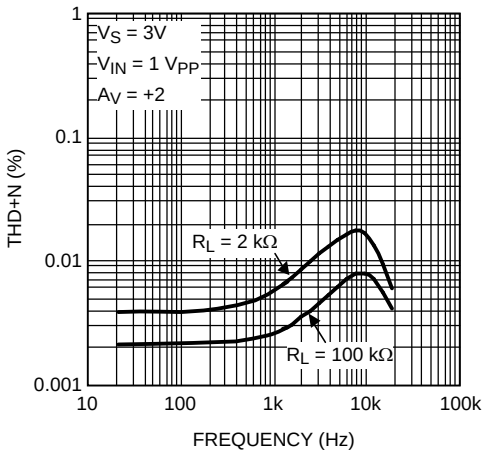

Figure 26. THD+N vs Frequency

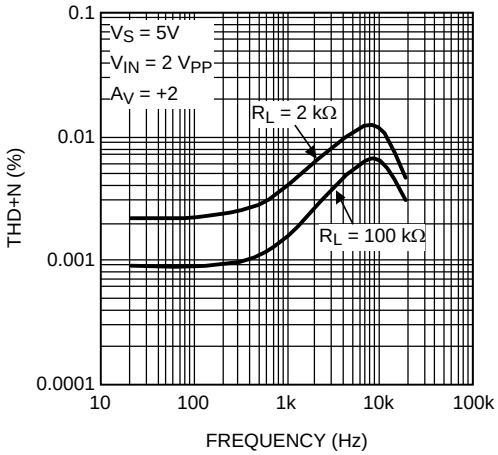

Figure 27. THD+N vs Frequency

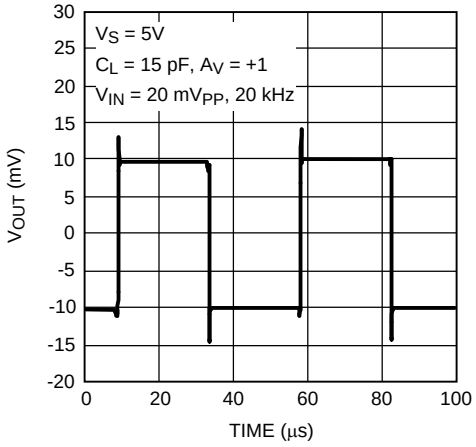

Figure 28. Small Signal Transient Response

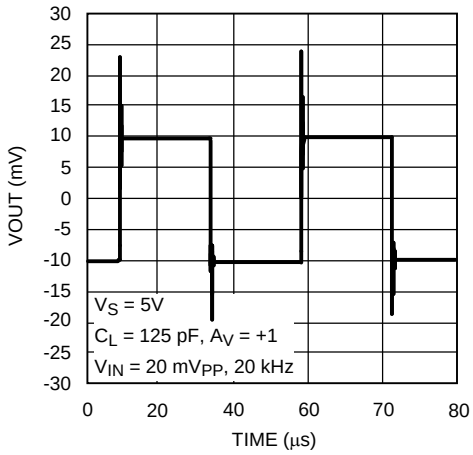

Figure 29. Small Signal Transient Response

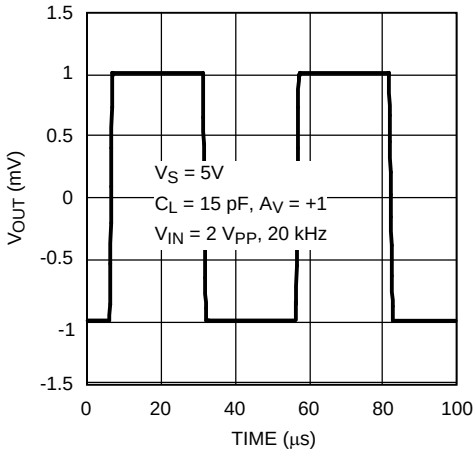

Figure 30. Large Signal Transient Response

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Typical Characteristics (continued)

Unless otherwise specified, T_A= 25°C, V_S= 5 V, V^+= 5 V, V^-= 0 V, V_{CM}= V_S/2

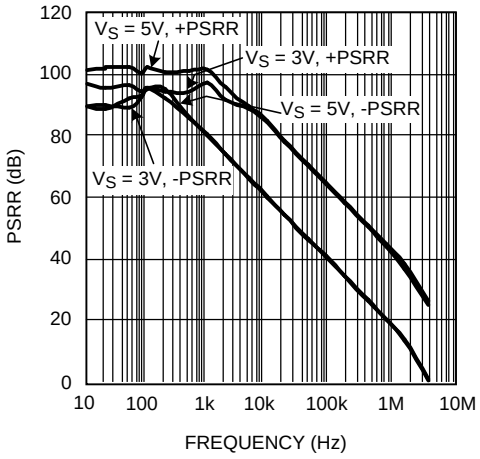

Figure 31. PSRR vs Frequency

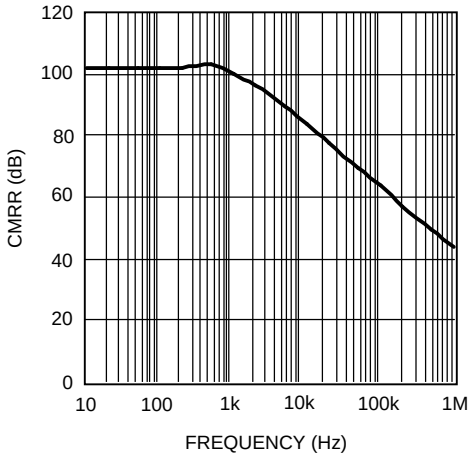

Figure 32. CMRR vs Frequency

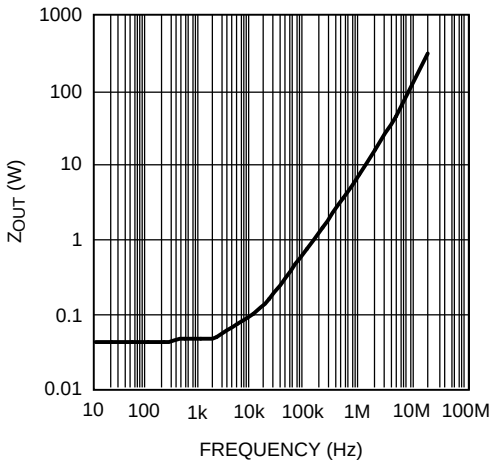

Figure 33. Closed-Loop Output Impedance vs Frequency

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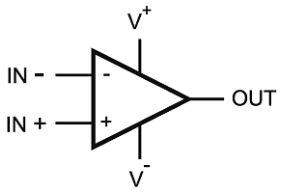
7 Detailed Description

7.1 Overview

TI's LMV65x devices have 12 MHz of bandwidth, are unity-gain stable, and consume only 116 µA of current. They also have a maximum input offset voltage of 1.5 mV, a rail-to-rail output stage, and an input common-mode voltage range that includes ground. Lastly, these operational amplifiers provide a PSRR of 95 dB, a CMRR of 100 dB, and a total harmonic distortion (THD) of 0.003% at 1-kHz frequency and 2-kΩ load.

7.2 Functional Block Diagram



(Each Amplifier)

7.3 Feature Description

7.3.1 Low Voltage and Low Power Operation

The LMV65x have performance specified at supply voltages of 3 V and 5 V. These parts are specified to be operational at all supply voltages between 2.7 V and 5.5 V. The LMV651 draws a low supply current of 116 µA, the LMV652 draws 118 µA/channel and the LMV654 draws 122 µA/channel. This family of operational amplifiers provides the low voltage and low power amplification that is essential for portable applications.

7.3.2 Wide Bandwidth

Despite drawing the very low supply current of 116 µA, the LMV65x manage to provide a wide unity-gain bandwidth of 12 MHz. This is easily one of the best bandwidth to power ratios ever achieved, and allows these operational amplifiers to provide wideband amplification while using the minimum amount of power. This makes this family of parts ideal for low-power signal processing applications such as portable media players and other accessories.

7.3.3 Low Input Referred Noise

The LMV65x provides a flatband input referred voltage noise density of 17 nV/$\sqrt{\text{Hz}}$, which is significantly better than the noise performance expected from a low-power operational amplifiers. These operational amplifiers also feature exceptionally low 1/f noise, with a very low 1/f noise corner frequency of 4 Hz. This makes these parts ideal for low power applications which require decent noise performance, such as PDAs and portable sensors.

7.3.4 Ground Sensing and Rail-to-Rail Output

The LMV65x each have a rail-to-rail output stage, which provides the maximum possible output dynamic range. This is especially important for applications requiring a large output swing. The input common-mode range of this family of devices includes the negative supply rail which allows direct sensing at ground in a single-supply operation.

7.3.5 Small Size

The small footprint of the packages for the LMV65x saves space on printed-circuit boards, and enables the design of smaller and more compact electronic products. Long traces between the signal source and the operational amplifier make the signal path susceptible to noise. By using a physically smaller package, these operational amplifiers can be placed closer to the signal source, reducing noise pickup and enhancing signal integrity.

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7.4 Device Functional Modes

7.4.1 Stability and Capacitive Loading

If the phase margin of the LMV65x is plotted with respect to the capacitive load (C_L) at its output, it is seen that the phase margin reduces significantly if C_L is increased beyond 100 pF. This is because the operational amplifier is designed to provide the maximum bandwidth possible for a low supply current. Stabilizing it for higher capacitive loads would have required either a drastic increase in supply current, or a large internal compensation capacitance, which would have reduced the bandwidth of the operational amplifier. Hence, if these devices are to be used for driving higher capacitive loads, they would have to be externally compensated.

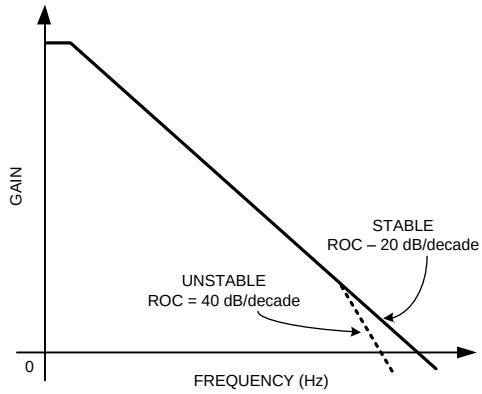

Figure 34. Gain vs Frequency for an Operational Amplifiers

An operational amplifier, ideally, has a dominant pole close to DC, which causes its gain to decay at the rate of 20 dB/decade with respect to frequency. If this rate of decay, also known as the rate of closure (ROC), remains the same until the unity-gain bandwidth of the operational amplifiers is stable. If, however, a large capacitance is added to the output of the operational amplifier, it combines with the output impedance of the operational amplifier to create another pole in its frequency response before its unity-gain frequency (see Figure 34). This increases the ROC to 40 dB/decade and causes instability.

In such a case a number of techniques can be used to restore stability to the circuit. The idea behind all these schemes is to modify the frequency response such that it can be restored to an ROC of 20 dB/decade, which ensures stability.

7.4.2 In The Loop Compensation

Figure 35 illustrates a compensation technique, known as *in-the-loop* compensation, that employs an RC feedback circuit within the feedback loop to stabilize a noninverting amplifier configuration. A small series resistance, R_S, is used to isolate the amplifier output from the load capacitance, C_L, and a small capacitance, C_F, is inserted across the feedback resistor to bypass C_L at higher frequencies.

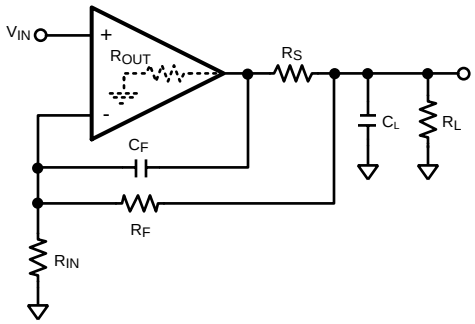

Figure 35. In-the-Loop Compensation

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Device Functional Modes (continued)

The values for R_S and C_F are decided by ensuring that the zero attributed to C_F lies at the same frequency as the pole attributed to C_L. This ensures that the effect of the second pole on the transfer function is compensated for by the presence of the zero, and that the ROC is maintained at 20 dB/decade. For the circuit shown in Figure 35 the values of R_S and C_F are given by Equation 1. Values of R_S and C_F required for maintaining stability for different values of C_L, as well as the phase margins obtained, are shown in Table 1. R_F and R_{IN} are taken to be 10 kΩ, R_L is 2 kΩ, while R_{OUT} is taken as 340 Ω.

$$R_S = \frac{R_{OUT}R_{IN}}{R_F}$$

$$C_F = \left(\frac{R_F + 2R_{IN}}{R_F^2}\right) C_L R_{OUT} \quad (1)$$

Table 1. Loop Compensation Values

C_L (pF)	R_S (Ω)	C_F (pF)	PHASE MARGIN (°)
150	340	15	39.4
200	340	20	34.6
250	340	25	31.1

Although this methodology provides circuit stability for any load capacitance, it does so at the price of bandwidth. The closed-loop bandwidth of the circuit is now limited by R_F and C_F.

7.4.3 Compensation By External Resistor

In some applications, it is essential to drive a capacitive load without sacrificing bandwidth. In such a case, in the loop compensation is not viable. A simpler scheme for compensation is shown in Figure 36. A resistor, R_{ISO}, is placed in series between the load capacitance and the output. This introduces a zero in the circuit transfer function, which counteracts the effect of the pole formed by the load capacitance, and ensures stability. The value of R_{ISO} to be used should be decided depending on the size of C_L and the level of performance desired. Values ranging from 5 Ω to 50 Ω are usually sufficient to ensure stability. A larger value of R_{ISO} results in a system with lesser ringing and overshoot, but it also limits the output swing and the short-circuit current of the circuit.

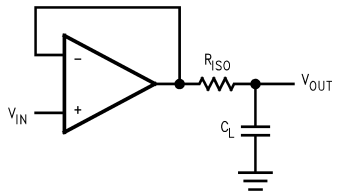

Figure 36. Compensation by Isolation Resistor

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

With a low supply current, low power operation, and low harmonic distortion, the LMV65x devices are ideal for wide-bandwidth, high gain amplification.

8.2 Typical Applications

8.2.1 High Gain, Low Power Inverting Amplifiers

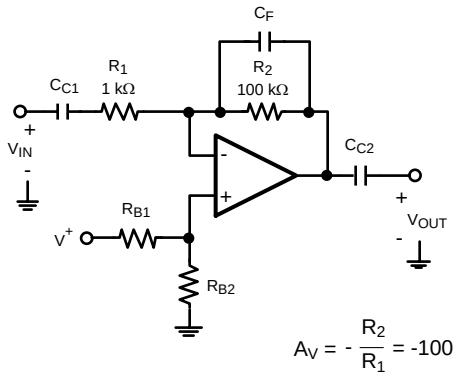

Figure 37. High Gain Inverting Amplifier

8.2.1.1 Design Requirements

The wide unity-gain bandwidth allows these parts to provide large gain over a wide frequency range, while driving loads as low as 2 kΩ with less than 0.003% distortion.

8.2.1.2 Detailed Design Procedure

Figure 37 is an inverting amplifier, with a 100-kΩ feedback resistor, R_2, and a 1-kΩ input resistor, R_1, and provides a gain of −100. With the LMV65x, these circuits can provide gain of −100 with a −3-dB bandwidth of 120 kHz, for a quiescent current as low as 116 µA. Coupling capacitors C_{C1} and C_{C2} can be added to isolate the circuit from DC voltages, while R_{B1} and R_{B2} provide DC biasing. A feedback capacitor C_F can also be added to improve compensation.

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Typical Applications (continued)

8.2.1.3 Application Curve

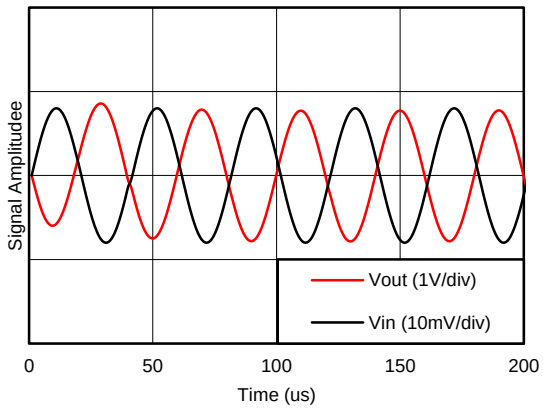

Figure 38. High Gain Inverting Amplifier Results

8.2.2 High Gain, Low Power Noninverting Amplifiers

With a low supply current, low power operation, and low harmonic distortion, the LMV65x devices are ideal for wide-bandwidth, high gain amplification. The wide unity-gain bandwidth allows these parts to provide large gain over a wide frequency range, while driving loads as low as 2 kΩ with less than 0.003% distortion. Figure 39 is a noninverting amplifier with a gain of 1001, can provide that gain with a −3-dB bandwidth of 12 kHz, for a similar low quiescent power dissipation. With the LMV65x, these circuits can provide gain of −100 with a −3-dB bandwidth of 120 kHz, for a quiescent current as low as 116 µA. Coupling capacitors C_{C1} and C_{C2} can be added to isolate the circuit from DC voltages, while R_{B1} and R_{B2} provide DC biasing. A feedback capacitor C_F can also be added to improve compensation.

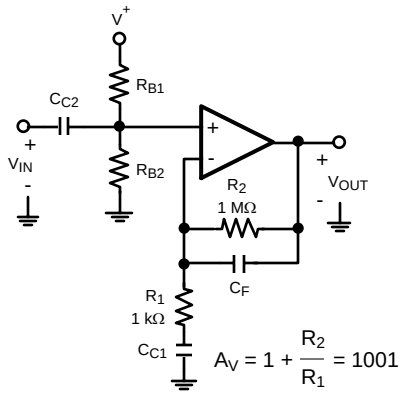

Figure 39. High Gain Noninverting Amplifier

8.2.3 Active Filters

With a wide unity-gain bandwidth of 12 MHz, low input-referred noise density, and a low power supply current, the LMV65x devices are well suited for low-power filtering applications. Active filter topologies, like the Sallen-Key low-pass filter shown in Figure 40, are very versatile, and can be used to design a wide variety of filters (Chebyshev, Butterworth, or Bessel). The Sallen-Key topology, in particular, can be used to attain a wide range of Q, by using positive feedback to reject the undesired frequency range.

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Typical Applications (continued)

In the circuit shown in Figure 40, the two capacitors appear as open circuits at lower frequencies and the signal is simply buffered to the output. At high frequencies the capacitors appear as short circuits and the signal is shunted to ground by one of the capacitors before it can be amplified. Near the cutoff frequency, where the impedance of the capacitances is on the same order as R_g and R_f, positive feedback through the other capacitor allows the circuit to attain the desired Q. The ratio of the two resistors, m^2, provides a knob to control the value of Q obtained.

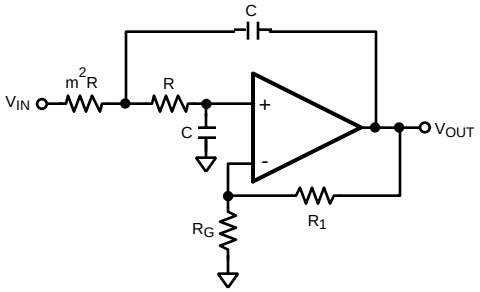

Figure 40. Sallen-Key Low-Pass Filter

8.3 Dos and Don'ts

Do properly bypass the power supplies.

Do add series resistence to the output when driving capacitive loads, particularly cables, Muxes, and ADC inputs.

Do add series current limiting resistors and external Schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1 mA or less (1 kΩ per volt).

9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, TI recommends that 10-nF capacitors be placed as close as possible to the operational amplifier power supply pins. For single supply, place a capacitor between V^+ and V^- supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between V^- and ground.

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10 Layout

10.1 Layout Guidelines

To properly bypass the power supply, several locations on a printed-circuit board need to be considered. A 6.8-µF or greater tantalum capacitor must be placed at the point where the power supply for the amplifier is introduced onto the board. Another 0.1-µF ceramic capacitor must be placed as close as possible to the power supply pin of the amplifier. If the amplifier is operated in a single power supply, only the V^+ pin needs to be bypassed with a 0.1-µF capacitor. If the amplifier is operated in a dual power supply, both V^+ and V^- pins must be bypassed.

It is good practice to use a ground plane on a printed-circuit board to provide all components with a low inductive ground connection.

Surface mount components in 0805 size or smaller are recommended in the LMV651-N application circuits. Designers can take advantage of the VSSOP miniature sizes to condense board layout in order to save space and reduce stray capacitance.

10.2 Layout Example

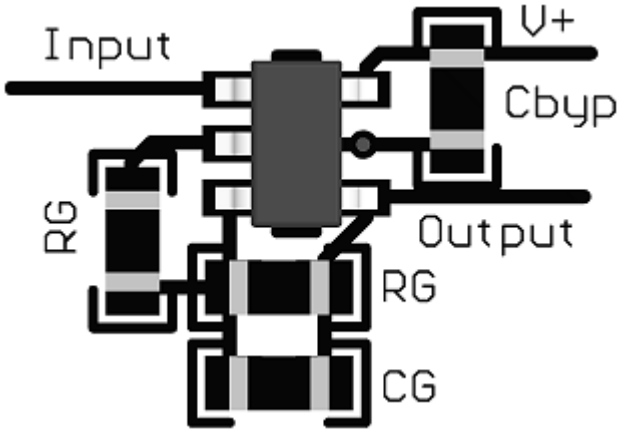

Figure 41. LMV65x Layout Example

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

LMV651 PSPICE Model http://www.ti.com/lit/zip/snom064

LMV652 PSPICE Model http://www.ti.com/lit/zip/snom065

LMV654 PSPICE Model http://www.ti.com/lit/zip/snom066

TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti

DIP Adapter Evaluation Module, http://www.ti.com/tool/dip-adapter-evm

TI Universal Operational Amplifier Evaluation Module, http://www.ti.com/tool/opampevm

TI Filterpro Software, http://www.ti.com/tool/filterpro

11.2 Documentation Support

11.2.1 Related Documentation

For additional applications, see the following:

AN-31 Op Amp Circuit Collection, SNLA140

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV651	Click here	Click here	Click here	Click here	Click here
LMV652	Click here	Click here	Click here	Click here	Click here
LMV654	Click here	Click here	Click here	Click here	Click here

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV651MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM		AY2A	Samples
LMV651MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM		AY2A	Samples
LMV651MG/NOPB	ACTIVE	SC70	DCK	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A93	Samples
LMV651MGX/NOPB	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A93	Samples
LMV652MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AB3A	Samples
LMV652MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AB3A	Samples
LMV654MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV65 4MT	Samples
LMV654MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV65 4MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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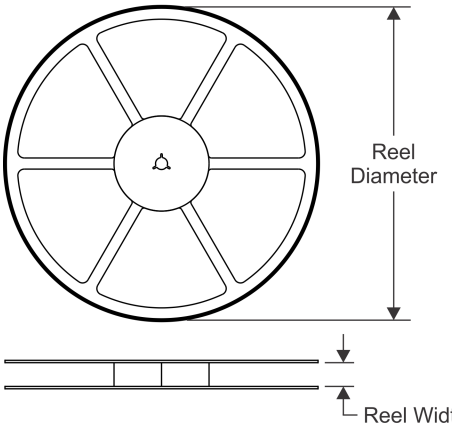
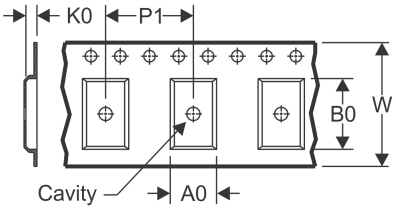
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

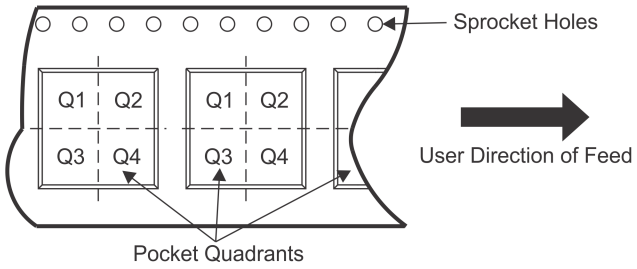


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

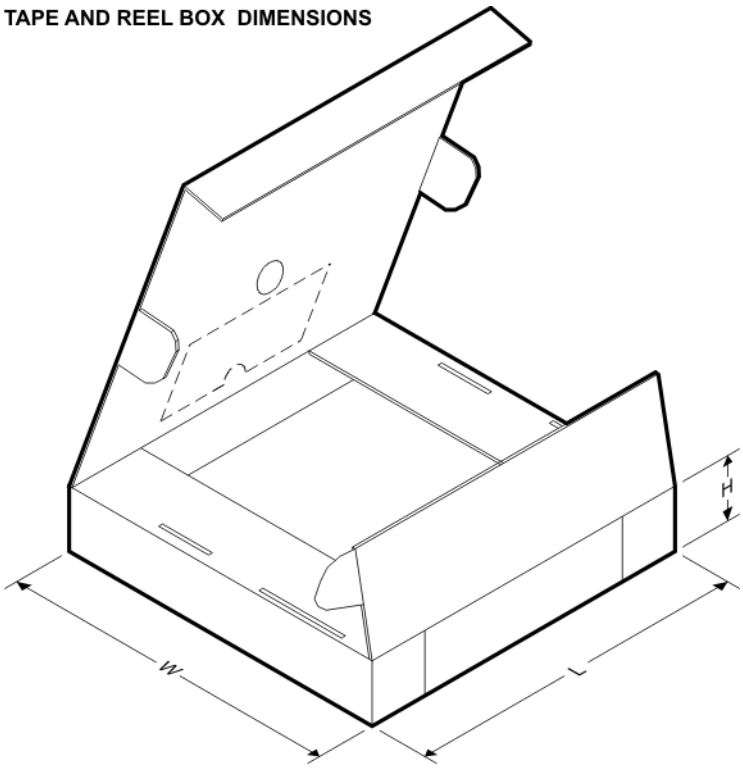
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV651MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV651MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV651MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV651MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV652MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV652MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV654MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

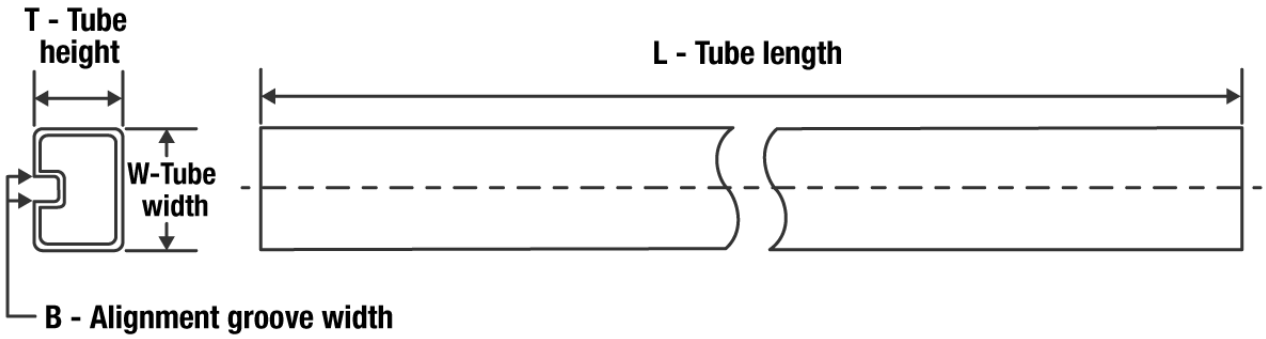
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV651MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV651MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV651MG/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LMV651MGX/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0
LMV652MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV652MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV654MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

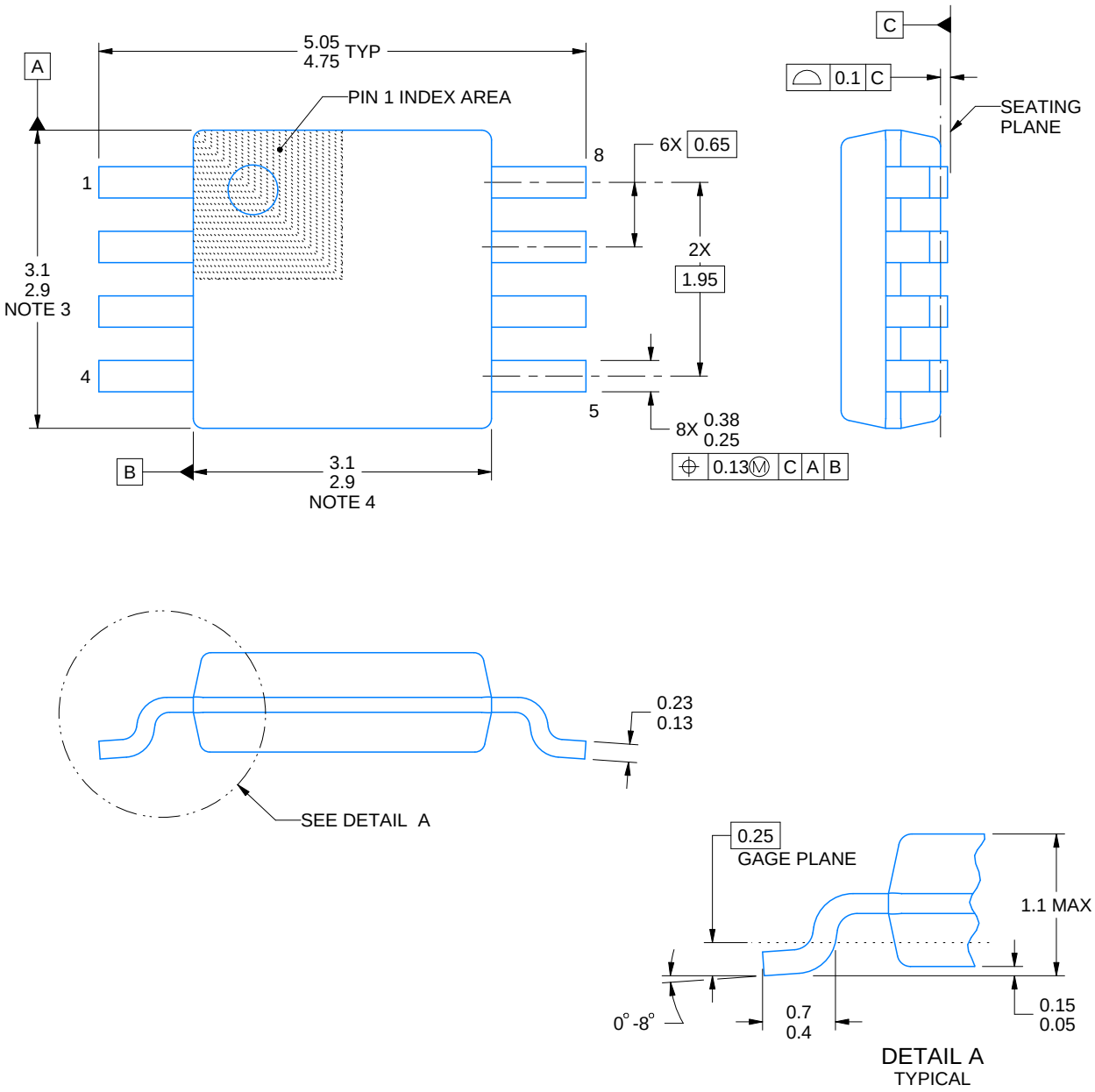
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMV654MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

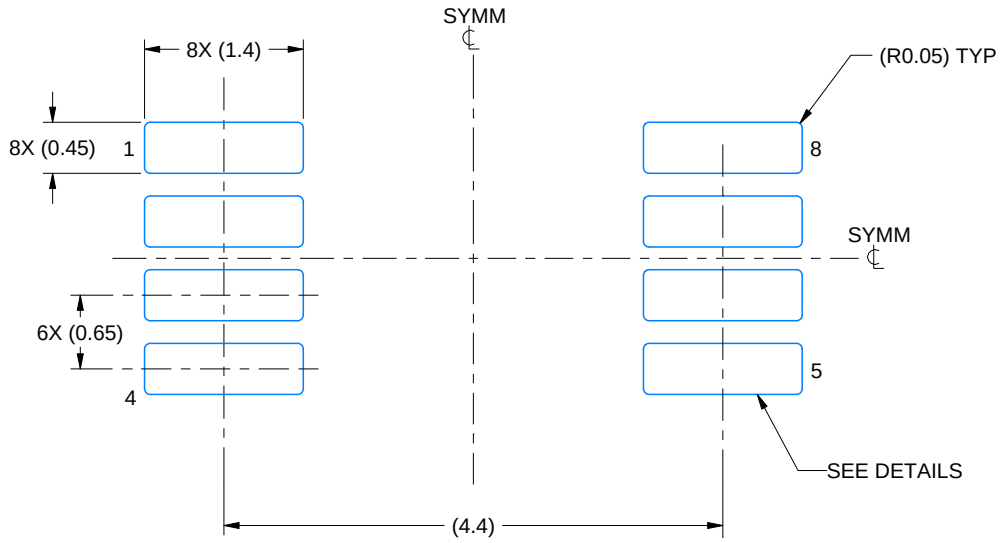
SMALL OUTLINE PACKAGE



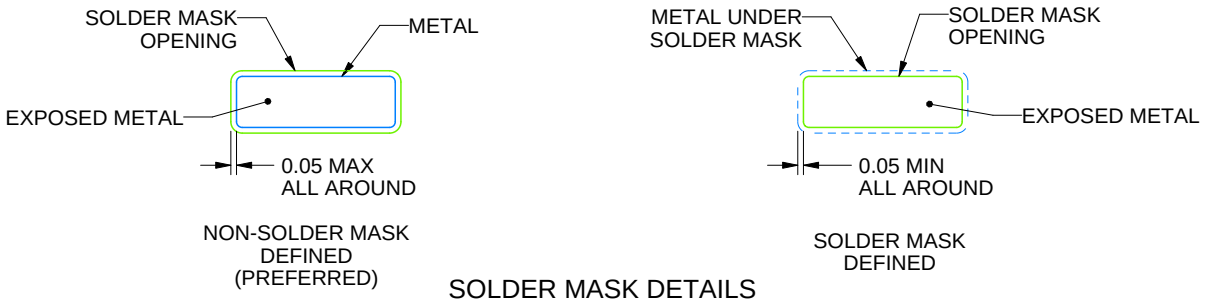
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

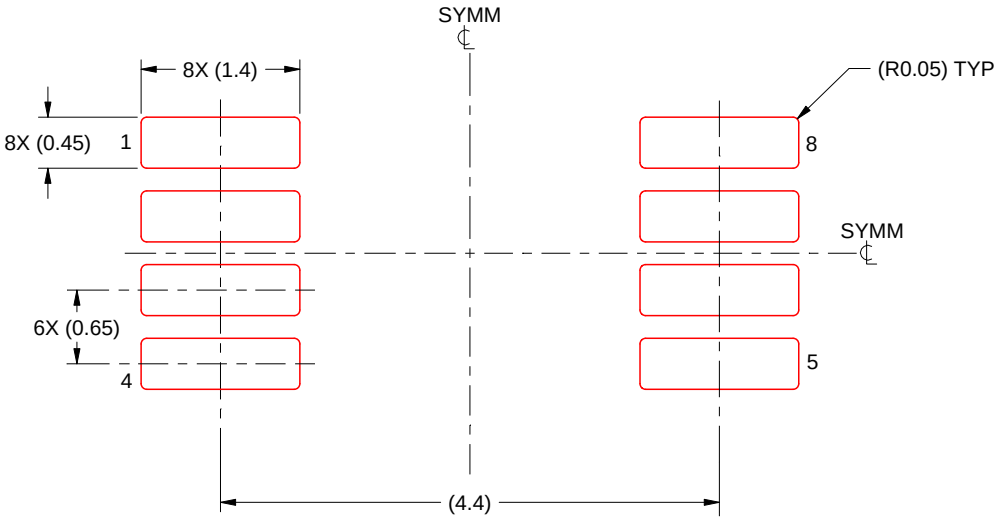


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

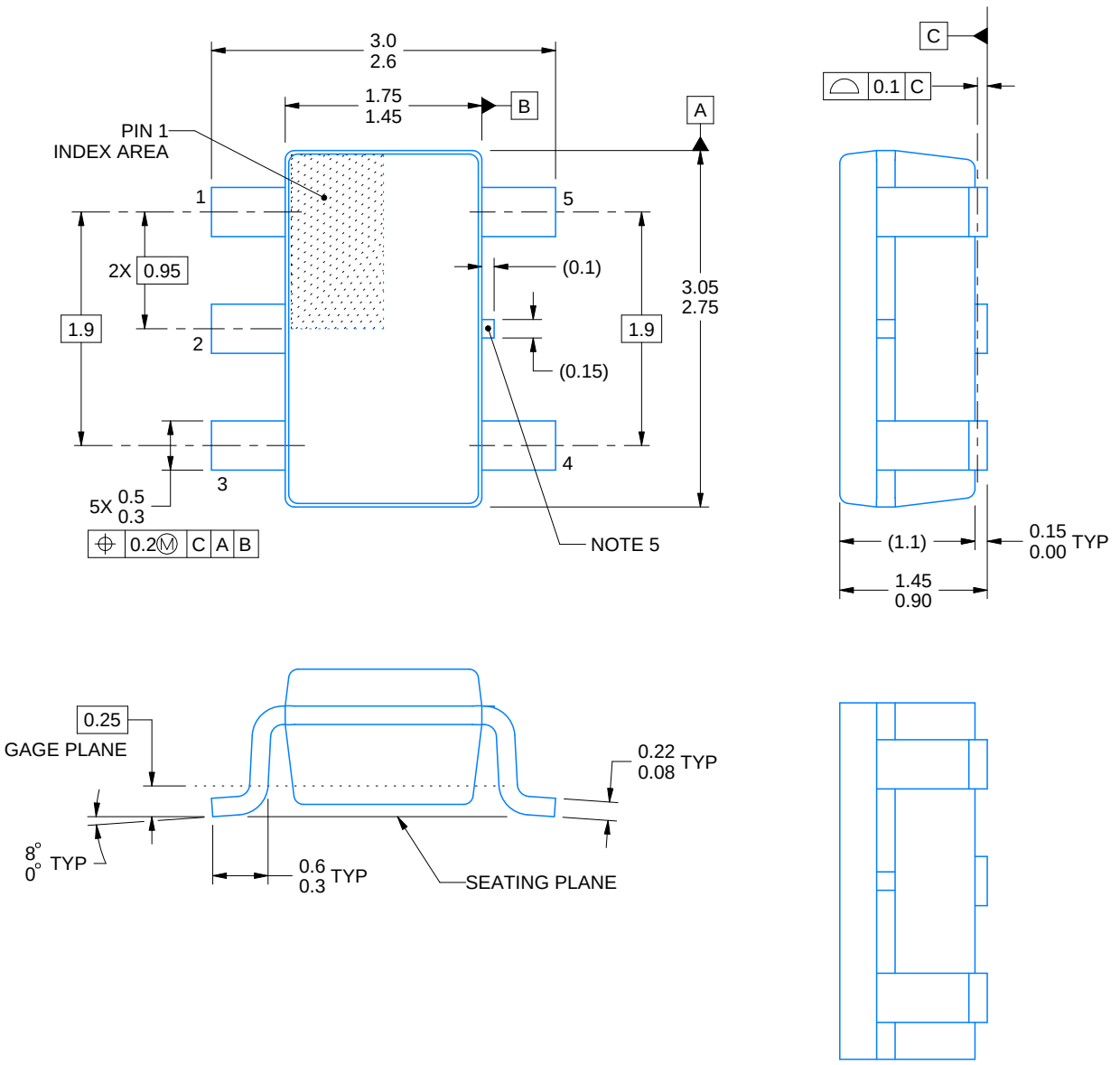
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

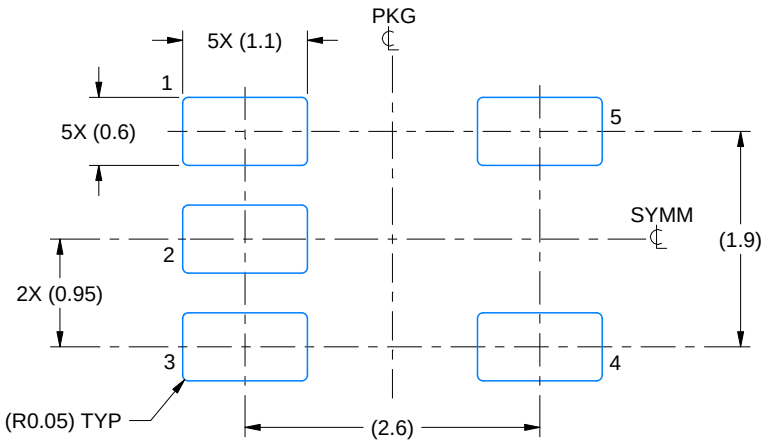


ALTERNATIVE PACKAGE SINGULATION VIEW

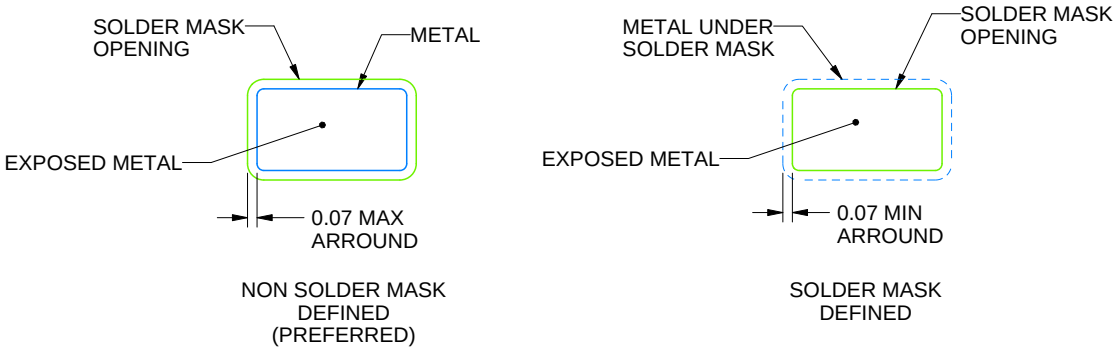
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

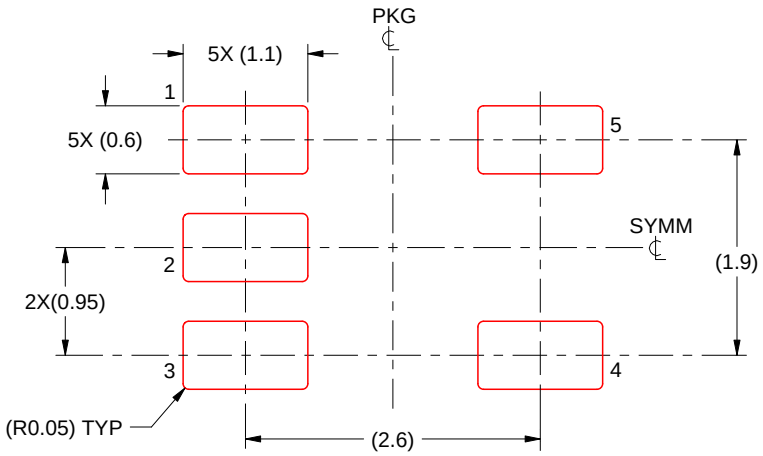


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

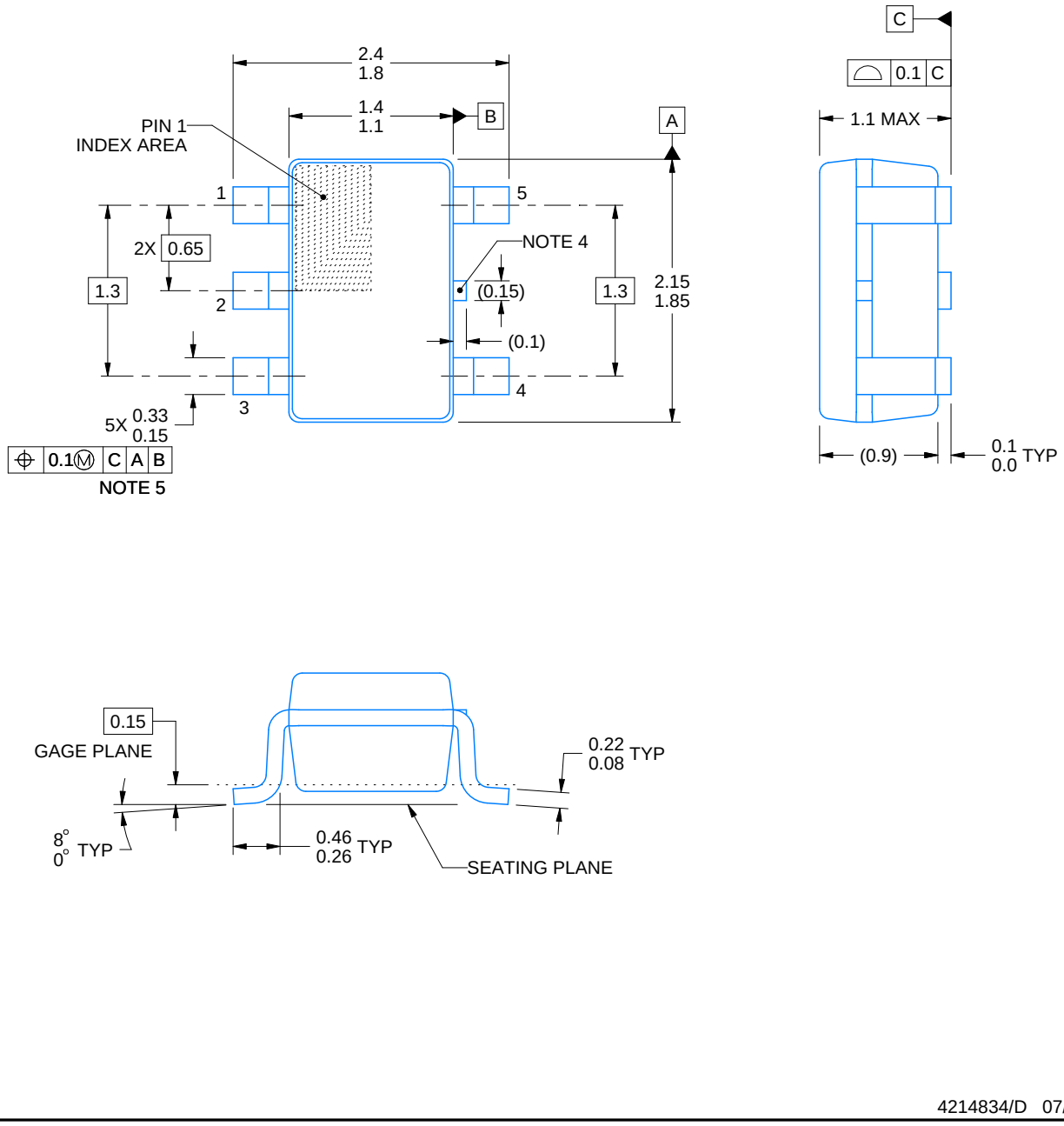
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

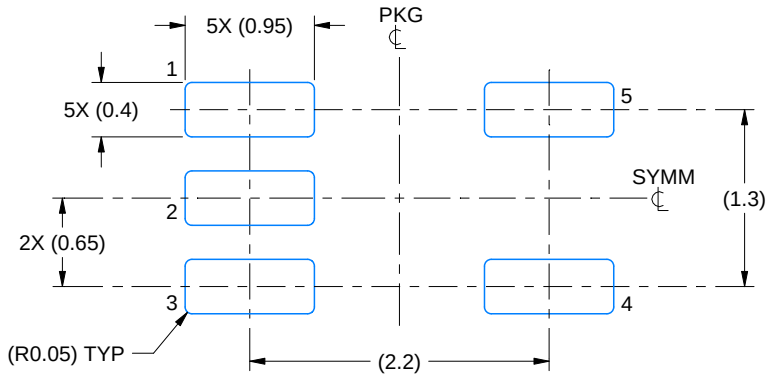
SMALL OUTLINE TRANSISTOR



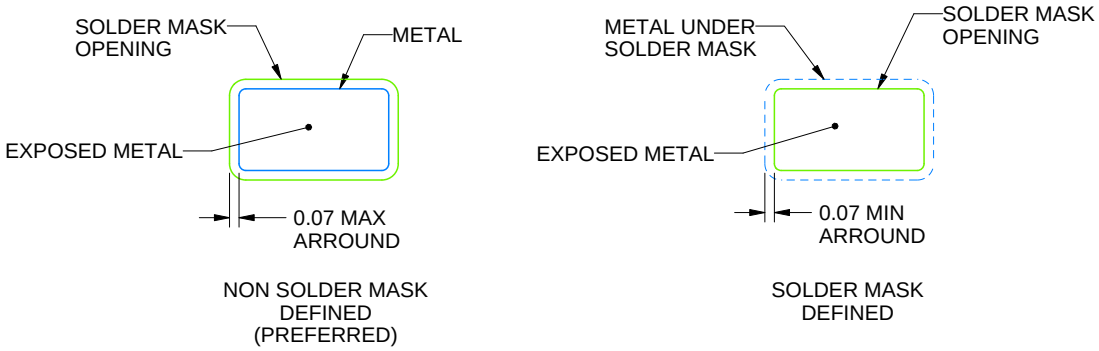
4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

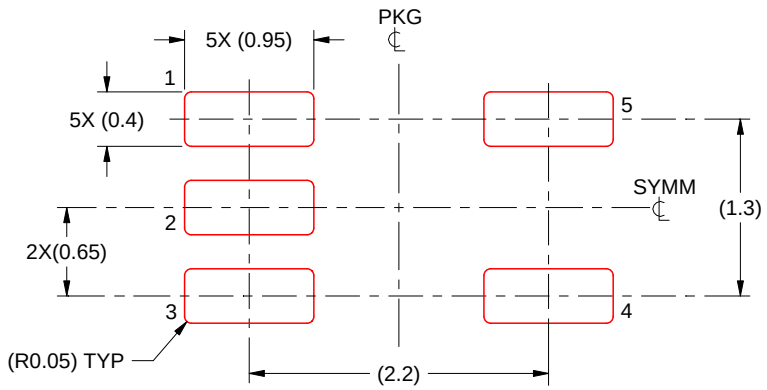


SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



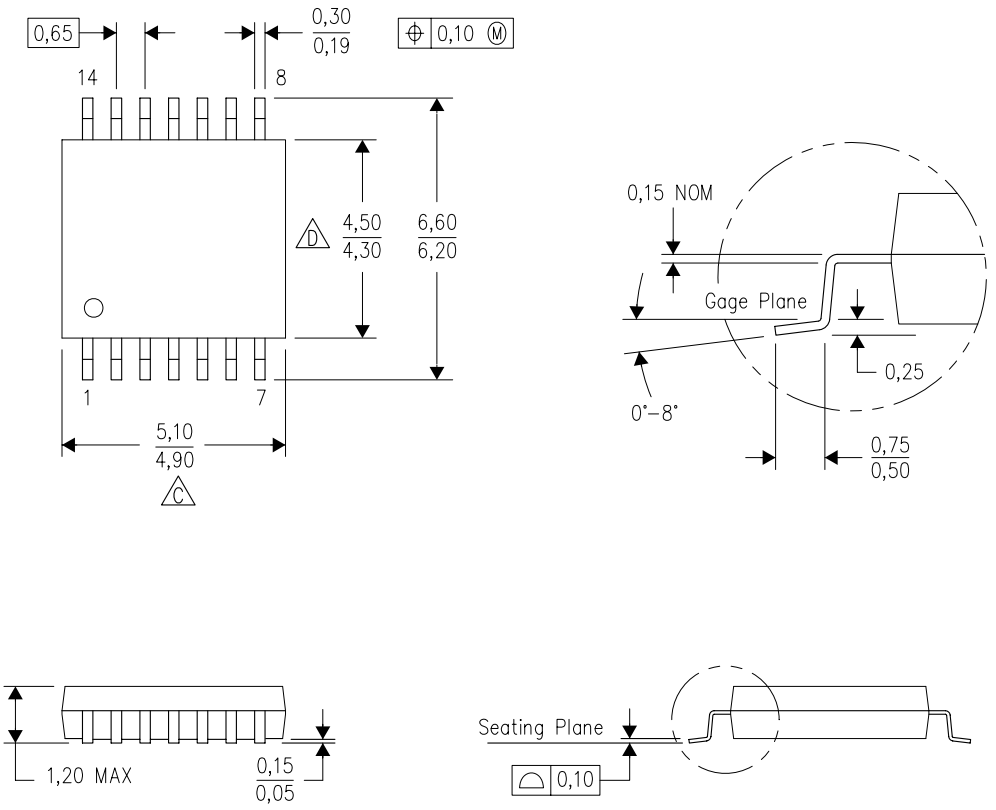
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

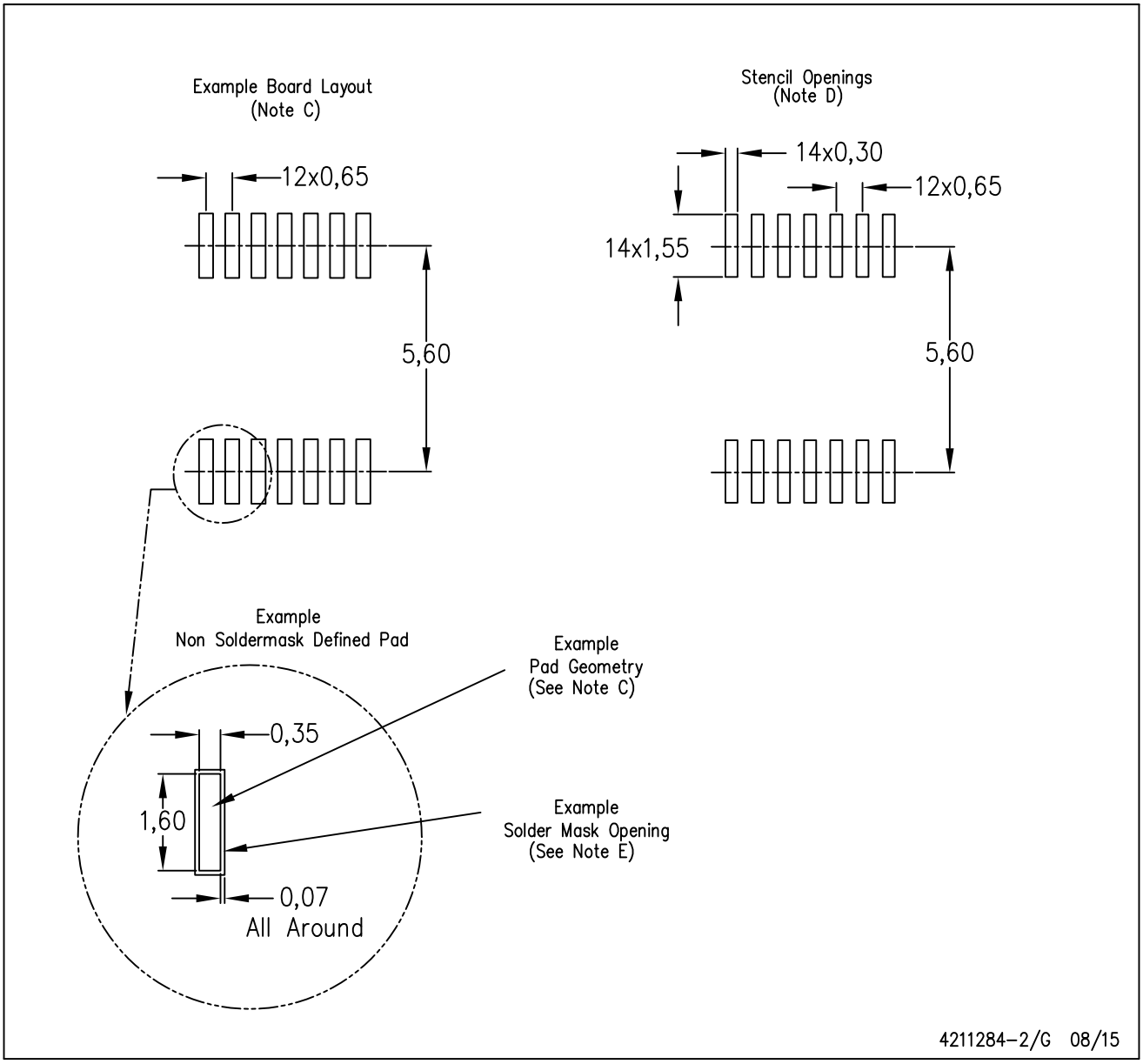
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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