

# SN74AC595-Q1 Automotive 8-Bit Shift Register With 3-State Output Registers

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Wide operating range of 1.5V to 6V
- Inputs accept voltages up to 6V
- Continuous  $\pm 24\text{mA}$  output drive at 5V
- Supports up to  $\pm 75\text{mA}$  output drive at 5V in short bursts
- Drives 50 $\Omega$  transmission lines
- Maximum  $t_{pd}$  of 12ns at 5V, 50pF load

## 2 Applications

- [Output expansion](#)
- [LED matrix control](#)
- [7-segment display control](#)

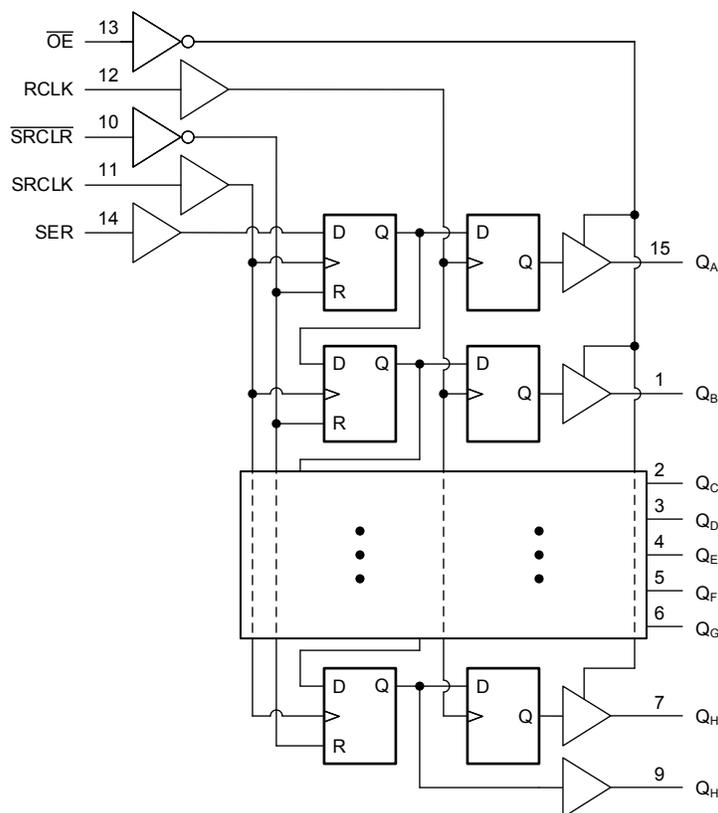
## 3 Description

The SN74AC595-Q1 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. This configuration allows data to be loaded into the shift register while the outputs remain static. The device includes 3-state outputs to allow for disabling the outputs. The device has a separate shift register output ( $Q_H$ ) for connecting shift registers in series.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE <sup>(3)</sup>
SN74AC595-Q1	PW (TSSOP, 16)	5mm × 6.4mm	5mm × 4.4mm
	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm

- (1) For more information, see [Section 11](#).
- (2) The package size (length x width) is a nominal value and includes pins, where applicable.
- (3) The body size (length x width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



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## 4 Pin Configuration and Functions

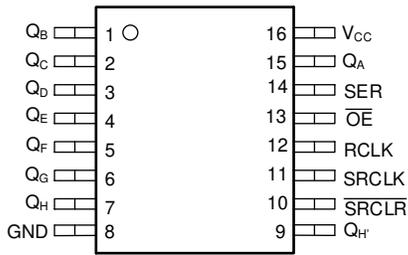


Figure 4-1. PW Package, 16-PIN TSSOP (Top View)

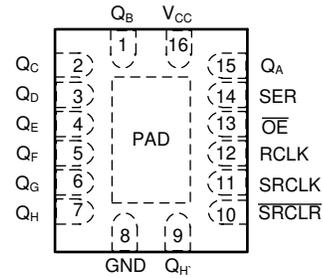


Figure 4-2. BQB Package, 16-Pin WQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
Q <sub>B</sub>	1	O	Storage register B output
Q <sub>C</sub>	2	O	Storage register C output
Q <sub>D</sub>	3	O	Storage register D output
Q <sub>E</sub>	4	O	Storage register E output
Q <sub>F</sub>	5	O	Storage register F output
Q <sub>G</sub>	6	O	Storage register G output
Q <sub>H</sub>	7	O	Storage register H output
GND	8	G	Ground
Q <sub>H'</sub>	9	O	Shift register H output
SRCLR	10	I	Shift register clear input, active low
SRCLK	11	I	Shift register clock input
RCLK	12	I	Output register clock input
OE	13	I	Output enable for Q <sub>A</sub> — Q <sub>H</sub> outputs, active low
SER	14	I	Shift register serial data input
Q <sub>A</sub>	15	O	Storage register A output
V <sub>CC</sub>	16	P	Positive supply
Thermal pad <sup>(2)</sup>		—	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.

(1) I = Input, O = Output, G = Ground, P = Power

(2) BQB package only

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>		-0.5	V <sub>CC</sub> + 0.5 V	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>		-0.5	V <sub>CC</sub> + 0.5 V	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V		±20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V		±50	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±50	mA
	Continuous output current through V <sub>CC</sub> or GND			±200	mA
T <sub>J</sub>	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Spec	Description	Condition	MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Supply voltage	1.5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.5 V	1.2		V
		V <sub>CC</sub> = 1.8 V	1.26		V
		V <sub>CC</sub> = 2.5 V	1.75		V
		V <sub>CC</sub> = 3 V	2.1		V
		V <sub>CC</sub> = 4.5 V	3.15		V
		V <sub>CC</sub> = 5.5 V	3.85		V
V <sub>IL</sub>	Low-Level input voltage	V <sub>CC</sub> = 1.5 V		0.3	V
		V <sub>CC</sub> = 1.8 V		0.54	V
		V <sub>CC</sub> = 2.5 V		0.75	V
		V <sub>CC</sub> = 3 V		0.9	V
		V <sub>CC</sub> = 4.5 V		1.35	V
		V <sub>CC</sub> = 5.5 V		1.65	V
V <sub>I</sub>	Input Voltage	Input Voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output Voltage	Output Voltage	0	V <sub>CC</sub>	V

### 5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

Spec	Description	Condition	MIN	MAX	UNIT
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.8 V		-1	mA
		V <sub>CC</sub> = 2.5 V		-2	mA
		V <sub>CC</sub> = 3 V		-12	mA
		V <sub>CC</sub> = 4.5 V to 5.5 V		-24	mA
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.8 V		1	mA
		V <sub>CC</sub> = 2.5 V		2	mA
		V <sub>CC</sub> = 3 V		12	mA
		V <sub>CC</sub> = 4.5 V to 5.5 V		24	mA
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.5 V to 3 V		50	ns/V
		V <sub>CC</sub> = 3.6 V to 5.5 V		20	ns/V
T <sub>A</sub>	Operating free-air temperature	Operating free-air temperature	-40	125	°C

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		BQB (WQFN)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	83.9	126.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	80.6	60.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	53.6	84.2	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	8.6	7.5	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	53.5	83.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	31.3	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	1.5 V	1.4	1.49	1.4	1.4	1.4	1.4	1.4	1.4	V	
		1.8 V	1.7	1.79	1.7	1.7	1.7	1.7	1.7	1.7		
		2.5 V	2.4	2.49	2.4	2.4	2.4	2.4	2.4	2.4		
		3 V	2.9	2.99	2.9	2.9	2.9	2.9	2.9	2.9		
		4.5 V	4.4	4.49	4.4	4.4	4.4	4.4	4.4	4.4		
		5.5 V	5.4	5.49	5.4	5.4	5.4	5.4	5.4	5.4		
	I <sub>OH</sub> = -1 mA	1.8 V	1.53		1.5		1.44					
	I <sub>OH</sub> = -2 mA	2.5 V	2.13		2.1		2					
	I <sub>OH</sub> = -4 mA	3 V	2.58		2.48		2.4					
	I <sub>OH</sub> = -12 mA	3 V	2.58		2.48		2.4					
	I <sub>OH</sub> = -24 mA	4.5 V	3.94		3.8		3.7					
	I <sub>OH</sub> = -24 mA	5.5 V	4.94		4.8		4.7					
	I <sub>OH</sub> = -50 mA <sup>(1)</sup>	5.5 V			3.85							
I <sub>OH</sub> = -75 mA <sup>(1)</sup>	5.5 V					3.85						

## 5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	1.5 V	0.01	0.1		0.1		0.1			V	
		1.8 V	0.01	0.1		0.1		0.1				
		2.5 V	0.01	0.1		0.1		0.1				
		3 V	0.01	0.1		0.1		0.1				
		4.5 V	0.01	0.1		0.1		0.1				
		5.5 V	0.01	0.1		0.1		0.1				
	I <sub>OL</sub> = 1 mA	1.8 V			0.2		0.3		0.36			
	I <sub>OL</sub> = 2 mA	2.5 V			0.36		0.44		0.5			
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44		0.5			
	I <sub>OL</sub> = 12 mA	3 V			0.36		0.44		0.5			
	I <sub>OL</sub> = 24 mA	4.5 V			0.36		0.44		0.5			
	I <sub>OL</sub> = 24 mA	5.5 V			0.36		0.44		0.5			
	I <sub>OL</sub> = 50 mA <sup>(1)</sup>	5.5 V					1.65					
I <sub>OL</sub> = 75 mA <sup>(1)</sup>	5.5 V							1.65				
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V		±0.1		±1		±1		μA		
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V		±0.25		±2.5		±5		μA		
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		2		20		20		μA		
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		9		9		9		pF		
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		15		15		15		pF		
C <sub>PD</sub>	C <sub>L</sub> = 50 pF, F = 1 MHz	5 V		60		60		60		pF		

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

## 5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

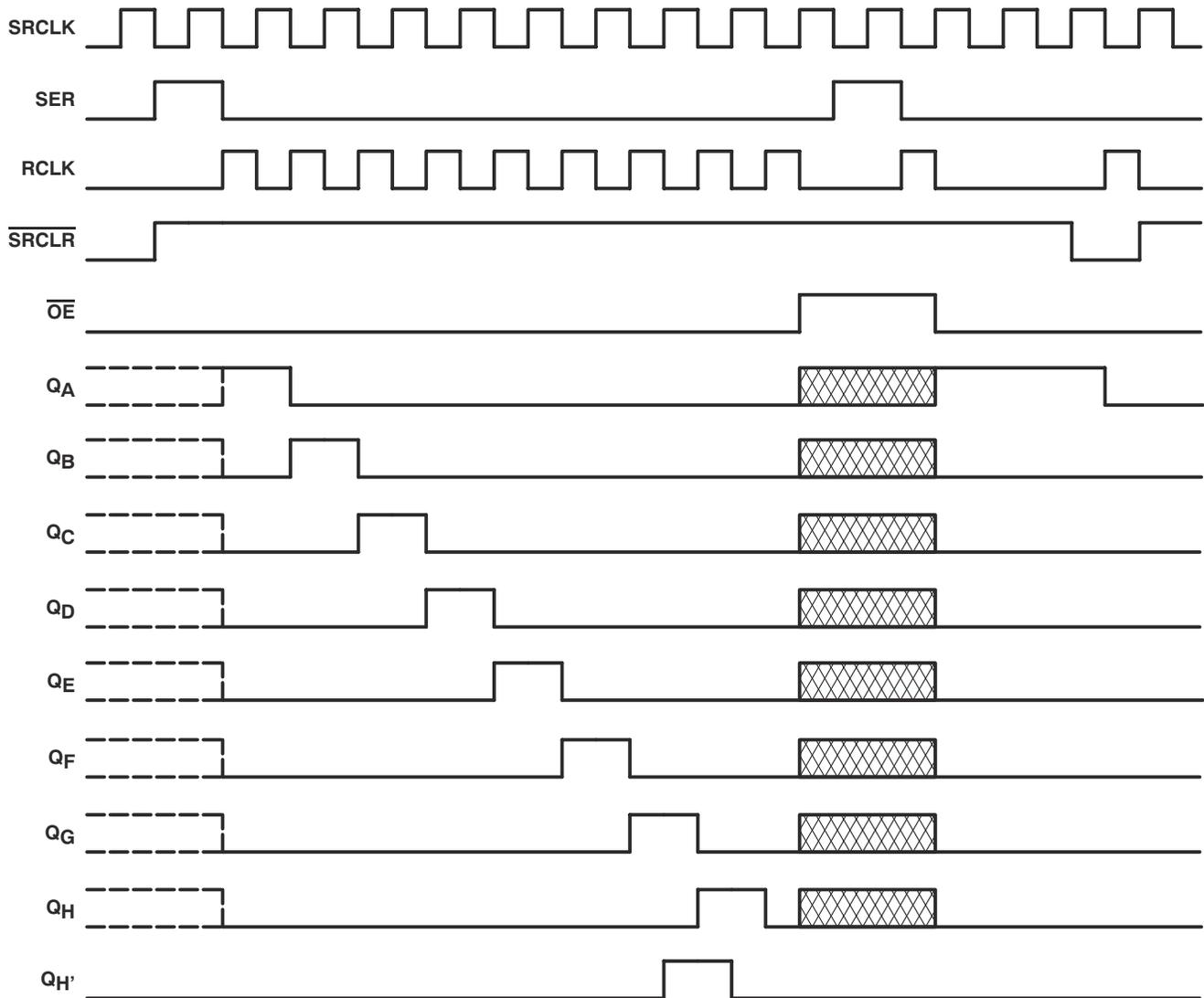
PARAMETER	DESCRIPTION	CONDITION	V <sub>CC</sub>	T <sub>A</sub> = 25°C		-40°C to 85°C		-40°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>CLOCK</sub>	Clock frequency		1.5 V					20	MHz	
			1.8 V					25	MHz	
			2.5 V					50	MHz	
			3.3 V					55	MHz	
			5 V					90	MHz	

## 5.6 Timing Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V <sub>CC</sub>	T <sub>A</sub> = 25°C		-40°C to 85°C		-40°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	RCLK or SRCLK high or low	1.5 V					13		ns
			1.8 V					8		ns
			2.5 V					6		ns
			3.3 V					4		ns
			5 V					2		ns
		SRCLR low	1.5 V					7		ns
			1.8 V					6		ns
			2.5 V					4		ns
			3.3 V					3		ns
			5 V					2		ns
t <sub>su</sub>	Setup time	SER before SRCLK↑	1.5 V					8		ns
			1.8 V					5		ns
			2.5 V					3		ns
			3.3 V					2		ns
			5 V					1		ns
		SRCLK↑ before RCLK↑	1.5 V					25		ns
			1.8 V					15		ns
			2.5 V					9		ns
			3.3 V					6		ns
			5 V					4		ns
		SRCLR low before RCLK↑	1.5 V					17		ns
			1.8 V					11		ns
			2.5 V					7		ns
			3.3 V					5		ns
			5 V					3		ns
		SRCLR high (inactive) before SRCLK↑	1.5 V					2		ns
			1.8 V					1		ns
			2.5 V					1		ns
			3.3 V					1		ns
			5 V					1		ns
t <sub>H</sub>	Hold time	SER after SRCLK↑	1.5 V					7		ns
			1.8 V					4		ns
			2.5 V					3		ns
			3.3 V					2		ns
			5 V					2		ns

### 5.7 Timing Diagrams



NOTE:  implies that the output is in 3-State mode.

### 5.8 Switching Characteristics

$C_L = 50$  pF; over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$			$-40^\circ\text{C to } 125^\circ\text{C}$			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PZL}$	$\overline{OE}$	Q	1.5 V								58	ns	
$t_{PZH}$	$\overline{OE}$	Q	1.5 V								54	ns	
$t_{PLZ}$	$\overline{OE}$	Q	1.5 V								42	ns	
$t_{PHZ}$	$\overline{OE}$	Q	1.5 V								50	ns	
$t_{PLH}$	RCLK	$Q_A-Q_H$	1.5 V								60	ns	
$t_{PHL}$	RCLK	$Q_A-Q_H$	1.5 V								60	ns	
$t_{PLH}$	SRCLK	$Q_{H'}$	1.5 V								64	ns	
$t_{PHL}$	SRCLK	$Q_{H'}$	1.5 V								63	ns	
$t_{PHL}$	$\overline{SRCLR}$	$Q_{H'}$	1.5 V								51	ns	
$t_{PZL}$	$\overline{OE}$	Q	1.8 V								38	ns	

## 5.8 Switching Characteristics (continued)

$C_L = 50$  pF; over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$			$-40^\circ\text{C to } 125^\circ\text{C}$			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PZH}$	$\overline{OE}$	Q	1.8 V								35	ns	
$t_{PLZ}$	$\overline{OE}$	Q	1.8 V								27	ns	
$t_{PHZ}$	$\overline{OE}$	Q	1.8 V								32	ns	
$t_{PLH}$	RCLK	$Q_A$ - $Q_H$	1.8 V								37	ns	
$t_{PHL}$	RCLK	$Q_A$ - $Q_H$	1.8 V								38	ns	
$t_{PLH}$	SRCLK	$Q_H$ '	1.8 V								39	ns	
$t_{PHL}$	SRCLK	$Q_H$ '	1.8 V								39	ns	
$t_{PHL}$	$\overline{SRCLR}$	$Q_H$ '	1.8 V								34	ns	
$t_{PZL}$	$\overline{OE}$	Q	2.5 V								24	ns	
$t_{PZH}$	$\overline{OE}$	Q	2.5 V								22	ns	
$t_{PLZ}$	$\overline{OE}$	Q	2.5 V								13	ns	
$t_{PHZ}$	$\overline{OE}$	Q	2.5 V								16	ns	
$t_{PLH}$	RCLK	$Q_A$ - $Q_H$	2.5 V								21	ns	
$t_{PHL}$	RCLK	$Q_A$ - $Q_H$	2.5 V								21	ns	
$t_{PLH}$	SRCLK	$Q_H$ '	2.5 V								22	ns	
$t_{PHL}$	SRCLK	$Q_H$ '	2.5 V								22	ns	
$t_{PHL}$	$\overline{SRCLR}$	$Q_H$ '	2.5 V								20	ns	
$t_{PZL}$	$\overline{OE}$	Q	3.3 V								19	ns	
$t_{PZH}$	$\overline{OE}$	Q	3.3 V								17	ns	
$t_{PLZ}$	$\overline{OE}$	Q	3.3 V								10	ns	
$t_{PHZ}$	$\overline{OE}$	Q	3.3 V								12	ns	
$t_{PLH}$	RCLK	$Q_A$ - $Q_H$	3.3 V								17	ns	
$t_{PHL}$	RCLK	$Q_A$ - $Q_H$	3.3 V								17	ns	
$t_{PLH}$	SRCLK	$Q_H$ '	3.3 V								18	ns	
$t_{PHL}$	SRCLK	$Q_H$ '	3.3 V								18	ns	
$t_{PHL}$	$\overline{SRCLR}$	$Q_H$ '	3.3 V								16	ns	
$t_{PZL}$	$\overline{OE}$	Q	5 V								13	ns	
$t_{PZH}$	$\overline{OE}$	Q	5 V								12	ns	
$t_{PLZ}$	$\overline{OE}$	Q	5 V								6	ns	
$t_{PHZ}$	$\overline{OE}$	Q	5 V								8	ns	
$t_{PLH}$	RCLK	$Q_A$ - $Q_H$	5 V								12	ns	
$t_{PHL}$	RCLK	$Q_A$ - $Q_H$	5 V								11	ns	
$t_{PLH}$	SRCLK	$Q_H$ '	5 V								12	ns	
$t_{PHL}$	SRCLK	$Q_H$ '	5 V								12	ns	
$t_{PHL}$	$\overline{SRCLR}$	$Q_H$ '	5 V								11	ns	

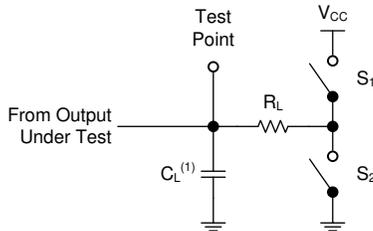
## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{MHz}$ ,  $Z_O = 50\Omega$ ,  $t_f < 2.5\text{ns}$ .

For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.

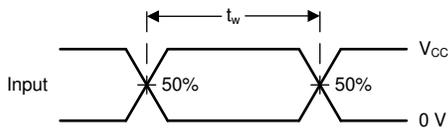
The outputs are measured individually with one input transition per measurement.

TEST	S1	S2	R <sub>L</sub>	C <sub>L</sub>	ΔV	V <sub>CC</sub>
t <sub>PLH</sub> , t <sub>PHL</sub>	OPEN	OPEN	—	2.5ns	—	ALL
t <sub>PLZ</sub> , t <sub>PZL</sub>	CLOSED	OPEN	500Ω	2.5ns	0.15V	≤ 2.5V
t <sub>PHZ</sub> , t <sub>PZH</sub>	OPEN	CLOSED	500Ω	2.5ns	0.15V	≤ 2.5V
t <sub>PLZ</sub> , t <sub>PZL</sub>	CLOSED	OPEN	500Ω	2.5ns	0.3V	> 2.5V
t <sub>PHZ</sub> , t <sub>PZH</sub>	OPEN	CLOSED	500Ω	2.5ns	0.3V	> 2.5V

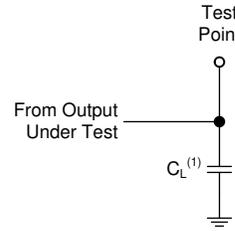


(1) C<sub>L</sub> includes probe and test-fixture capacitance.

**Figure 6-1. Load Circuit for 3-State Outputs**

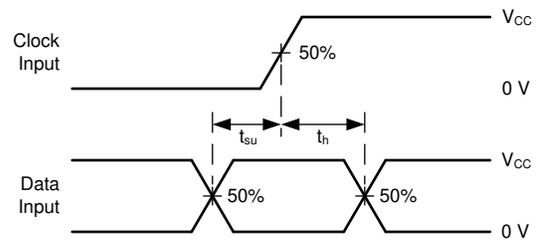


**Figure 6-3. Voltage Waveforms, Pulse Duration**

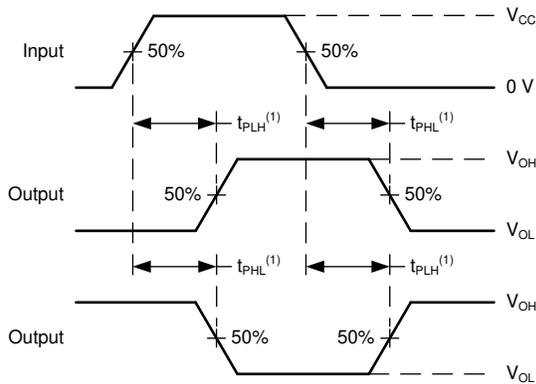


(1) C<sub>L</sub> includes probe and test-fixture capacitance.

**Figure 6-2. Load Circuit for Push-Pull Outputs**

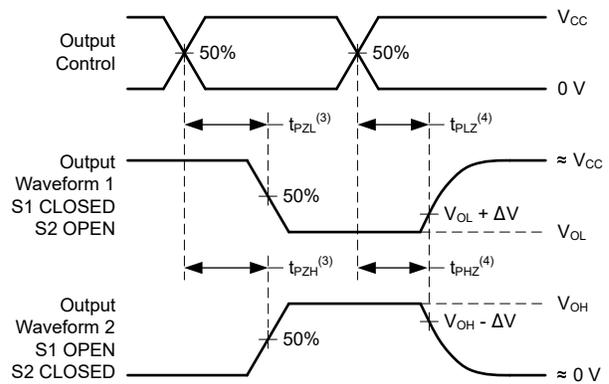


**Figure 6-4. Voltage Waveforms, Setup and Hold Times**



(1) The greater between t<sub>PLH</sub> and t<sub>PHL</sub> is the same as t<sub>pd</sub>.

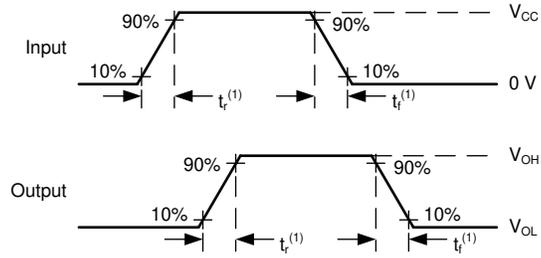
**Figure 6-5. Voltage Waveforms Propagation Delays**



(3) The greater between t<sub>PZL</sub> and t<sub>PZH</sub> is the same as t<sub>en</sub>.

(4) The greater between t<sub>PLZ</sub> and t<sub>PHZ</sub> is the same as t<sub>dis</sub>.

**Figure 6-6. Voltage Waveforms Propagation Delays**



(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .

**Figure 6-7. Voltage Waveforms, Input and Output Transition Times**

## 7 Detailed Description

### 7.1 Overview

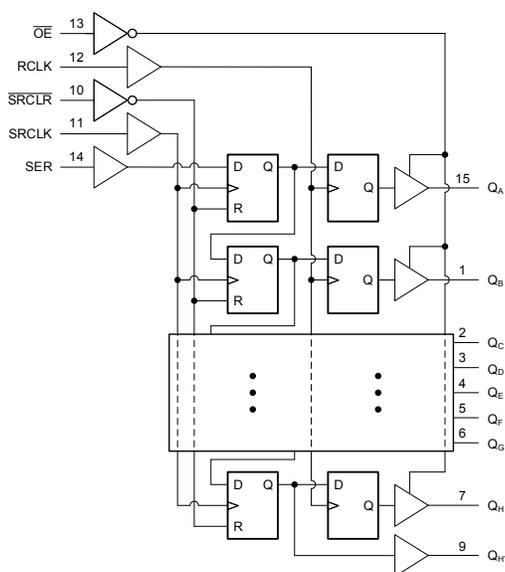
The SN74AC595-Q1 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 parallel 3-state outputs. Separate clocks are provided for both the shift (SRCLK) and storage (RCLK) registers.

The shift register has a direct overriding clear ( $\overline{\text{SRCLR}}$ ) input, serial (SER) input, and a serial output ( $Q_H$ ) for cascading. When the output-enable ( $\overline{\text{OE}}$ ) input is high, all outputs, except  $Q_H$ , are in the high-impedance state.

Both the shift-register clock (SRCLK) and storage-register clock (RCLK) are positive-edge triggered.

If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register. In this configuration, it takes 8 clock pulses to load data into all 8 registers, and 9 clock pulses for the outputs to display that data.

### 7.2 Functional Block Diagram



**Figure 7-1. Logic Diagram (Positive Logic)**

### 7.3 Device Functional Modes

**Table 7-1. Function Table**

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	OE	
X	L, H, ↓	H	X	X	Shift register data remains constant.
X	X	X	L, H, ↓	X	Storage register data remains constant.
X	X	X	X	H	Outputs Q <sub>A</sub> –Q <sub>H</sub> are disabled.
X	X	X	X	L	Outputs Q <sub>A</sub> –Q <sub>H</sub> are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Each subsequent stage stores the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Each subsequent stage stores the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored into the storage register.

## 8 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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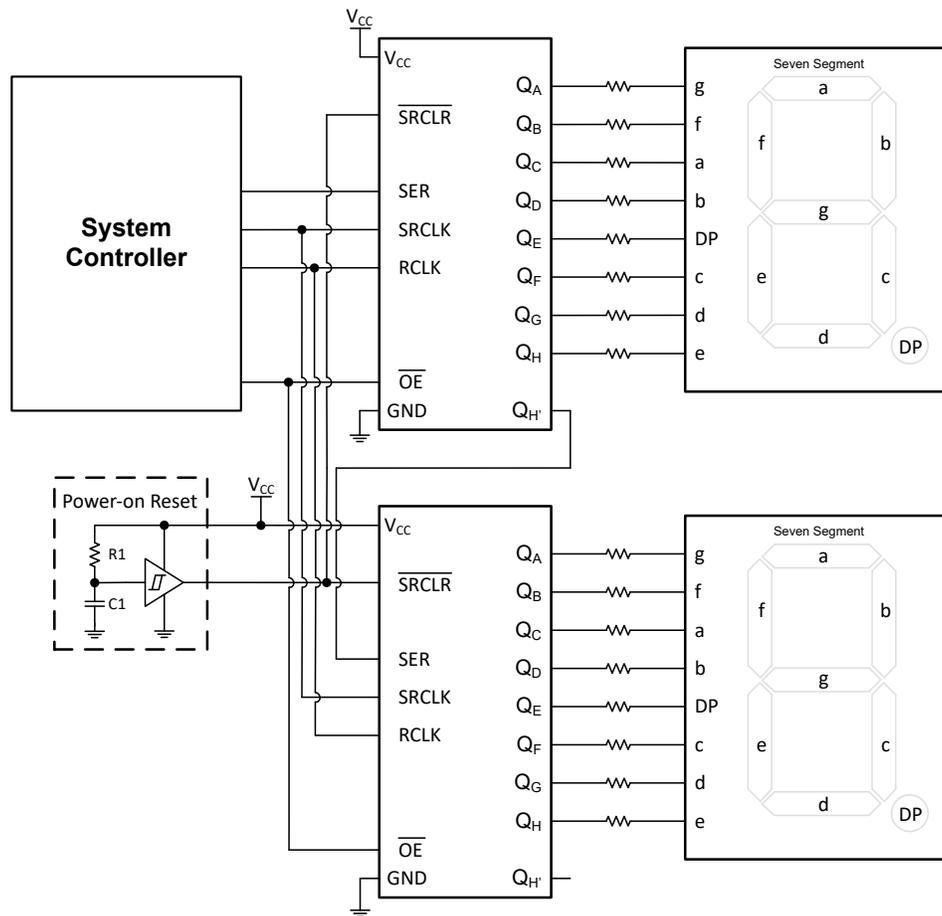
### 8.1 Application Information

In this application, the SN74AC595-Q1 is used to control seven-segment displays. Utilizing the serial output and combining a few of the input signals, this implementation reduces the number of I/O pins required to control the displays from sixteen to four. Unlike other I/O expanders, the SN74AC595-Q1 does not need a communication interface for control. It can be easily operated with simple GPIO pins.

The OE pin is used to easily disable the outputs when the displays need to be turned off or connected to a PWM signal to control brightness. However, this pin can be tied low and the outputs of the SN74AC595-Q1 can be controlled accordingly to turn off all the outputs reducing the I/O needed to three. There is no practical limitation to how many SN74AC595-Q1 devices can be cascaded. To add more, the serial output will need to be connected to the following serial input and the clocks will need to be connected accordingly. With separate control for the shift registers and output registers, the desired digit can be displayed while the data for the next digit is loaded into the shift register.

At power-up, the initial state of the shift registers and output registers are unknown. To give them a defined state, the shift register needs to be cleared and then clocked into the output register. An RC circuit can be connected to the  $\overline{\text{SRCLR}}$  pin as shown in the [Figure 8-1](#) to initialize the shift register to all zeros. With the  $\overline{\text{OE}}$  pin pulled up with a resistor, this process can be performed while the outputs are in a high impedance state eliminating any erroneous data causing issues with the displays.

## 8.2 Typical Application



**Figure 8-1. Typical Application Block Diagram**

### 8.2.1 Design Requirements

#### 8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AC595-Q1 plus the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AC595-Q1 plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74AC595-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74AC595-Q1 can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

#### CAUTION

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 8.2.1.2 Input Considerations

Input signals must cross  $V_{IL(max)}$  to be considered a logic LOW, and  $V_{IH(min)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AC595-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10k $\Omega$  resistor value is often used due to these factors.

The SN74AC595-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

### 8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### 8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is  $\leq 50\text{pF}$ . This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74AC595-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(\text{max})})\Omega$ . Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in  $\text{M}\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

### 8.3 Application Curves

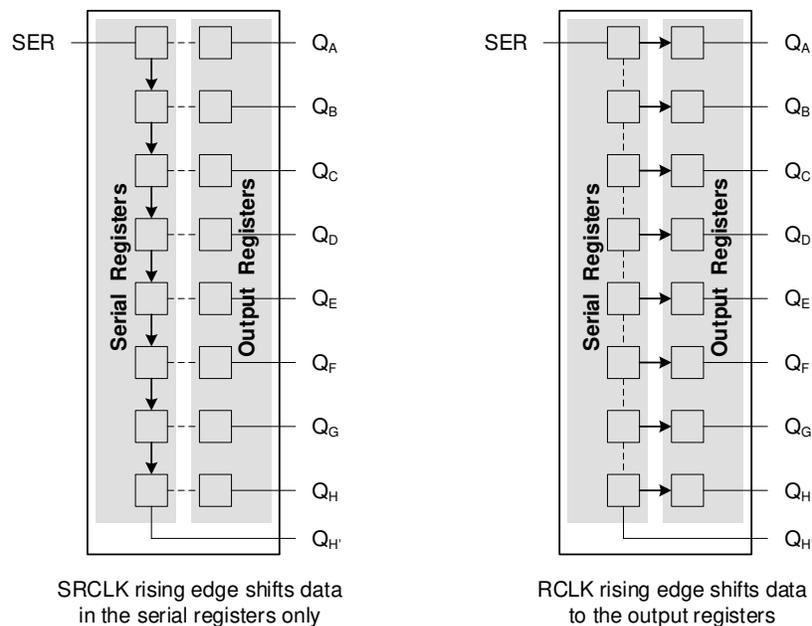


Figure 8-2. Simplified Functional Diagram Showing Clock Operation

### 8.4 Power Supply Recommendations

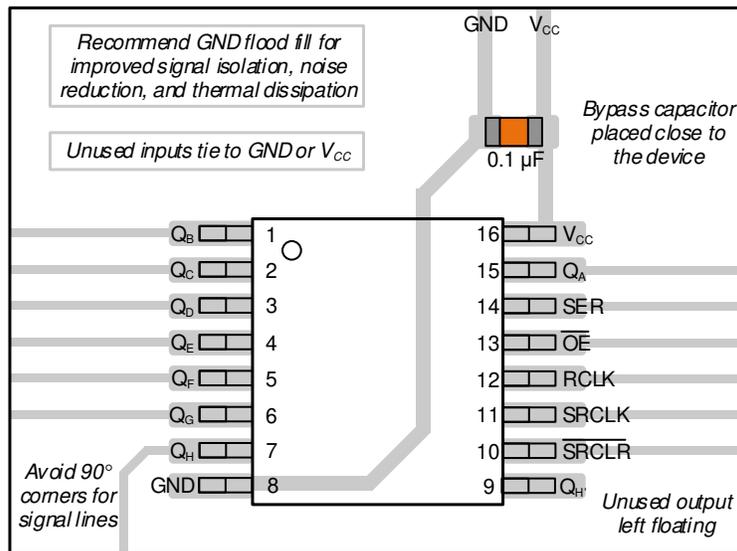
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A  $0.1\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The  $0.1\mu\text{F}$  and  $1\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

## 8.5 Layout

### 8.5.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 8.5.2 Layout Example



**Figure 8-3. Example Layout for the SN74AC595-Q1**

## 9 Device and Documentation Support

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

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### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2024) to Revision A (April 2024)	Page
• Changed the status from: <i>Advanced Information</i> to: <i>Production Data</i> .....	1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PSN74AC595PWRQ1	ACTIVE	TSSOP	PW	16	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

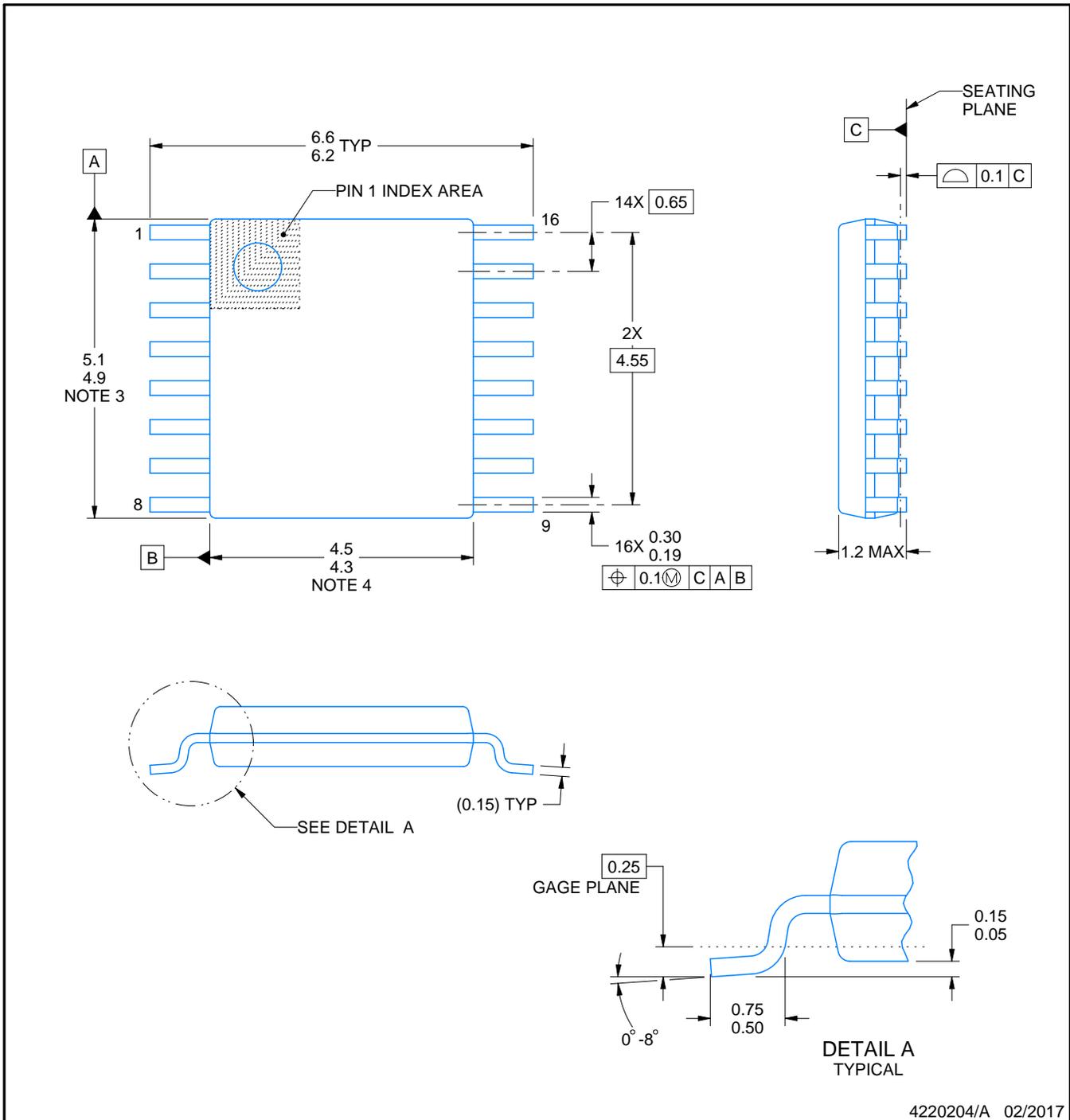
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:

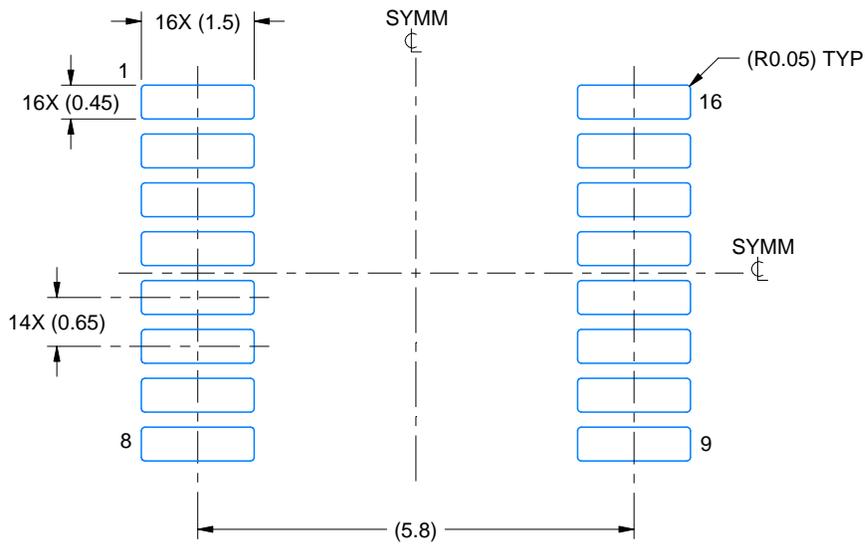
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

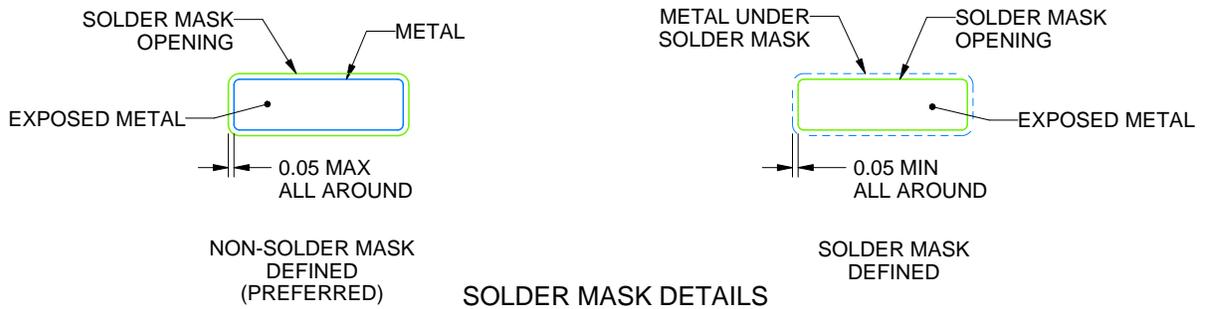
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

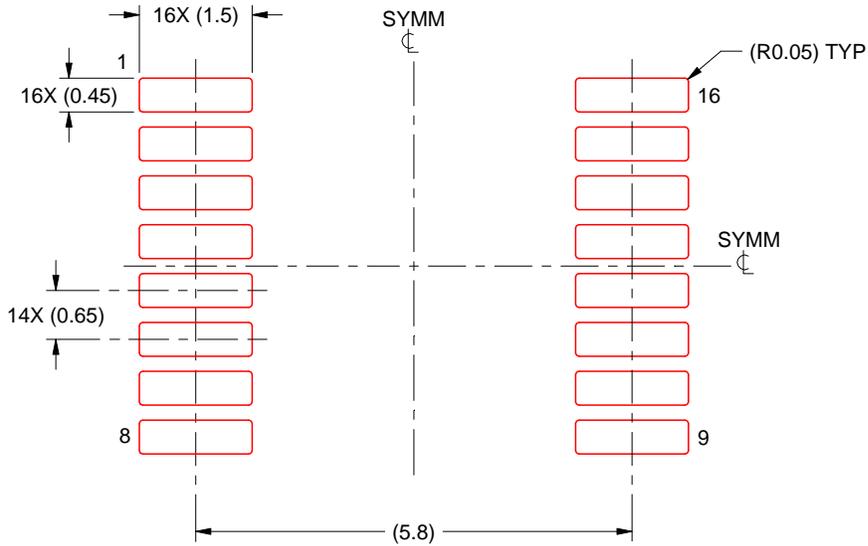
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

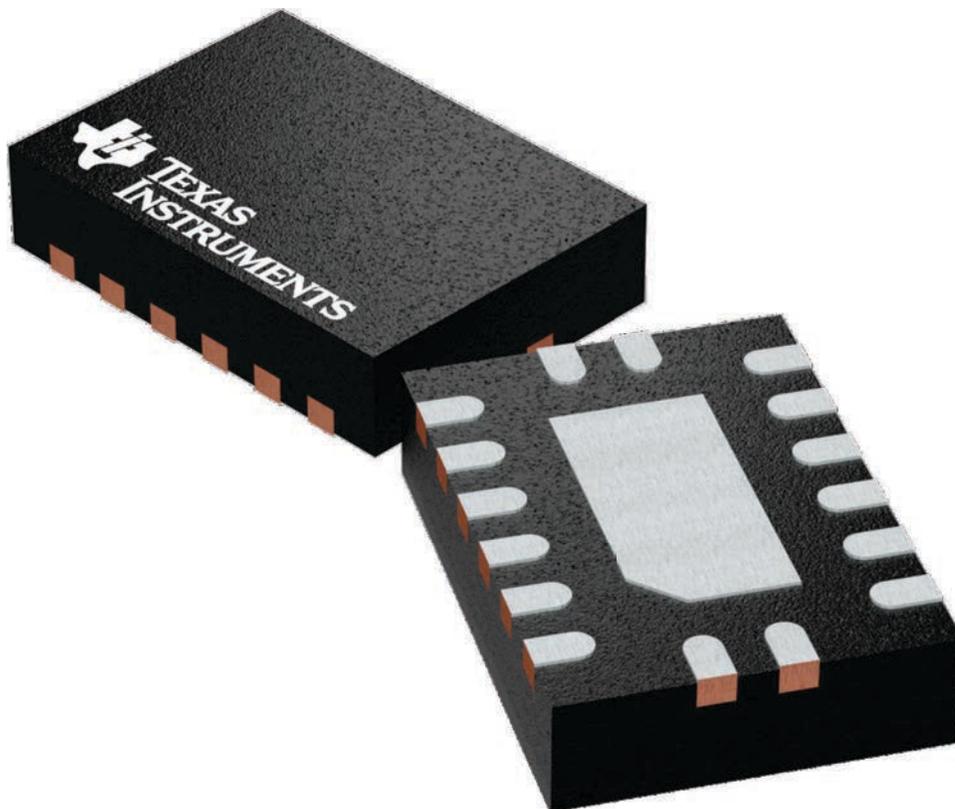
**BQB 16**

**WQFN - 0.8 mm max height**

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226161/A

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