Design Considerations for Active Clamp and Reset Technique

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Abstract

Performance of the single-ended forward and flyback converters can be significantly enhanced by use of the active clamp/reset technique. The benefits of this technique include higher efficiency at high switching frequencies, lower EMI/RFI and lower component stresses. Previous Unitrode Seminar (SEM-1000) and other publications have provided a qualitative overview of this technique by highlighting various modes of operation. This paper addresses the design considerations required for designing single-ended active clamp forward and flyback converters. Major performance trade-offs are identified and quantified. A design procedure with relevant equations is provided. This procedure is used to design an off-line forward converter with active clamping. Operating results of this converter are presented with effects of certain design choices highlighted.

1. Introduction

Single-ended active clamp converters, stemming from designs first documented by Bruce Carsten in 1978[1], have more recently gained widespread acceptance for many medium power off-line and DC/DC converter applications. This topology adds an active clamp network - consisting of a small auxilliary switch in series with a capacitor plus the associated drive circuitry - to traditional transformer-isolated forward and flyback converters resulting in significant performance enhancements. Theory and operation of these converters have been reported in many recent publications [2-7]. Typically, the clamp switch is kept on during the off-time of the main switch. As a result, the clamp capacitor absorbs and returns parasitic energy during every cycle with minimal losses. A large value of the clamp capacitance keeps the associated voltage ripple to a minimum.

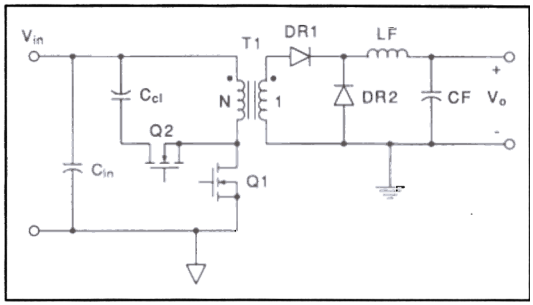

Figure 1(a). Active clamp forward converter with flyback-type clamp

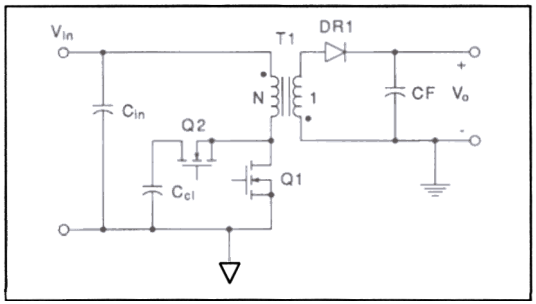

Figure 1(b). Active clamp flyback converter with boost type clamp

Fig. 1 depicts the active clamp approach applied to forward and flyback converters. As shown in the figure, two distinct types of clamping are possible depending on how the active clamp network is placed in the converter. In Fig. 1(a), the clamp circuit, known as flyback type clamp, is applied across the primary winding. The clamp circuit in Fig. 1(b), known as boost type clamp, is applied across the switch. Both types of clamps are very similar in nature and applicable to either forward or flyback converters. The major difference

is the steady state voltage across the clamp capacitance. Equations 1(a) and (b) give the clamp voltage values as functions of input voltage and main switch duty cycle. These equations closely resemble the transfer functions of flyback and boost converters respectively, hence the nomenclature of clamp circuits. It is seen that the voltage stress on the capacitor is higher by a value of V_{in} for the boost type clamp compared to the flyback type clamp, making the flyback clamp more practical. The boost clamp configuration also forces a higher AC current through the input filter capacitor during clamp mode. One possible advantage of using the boost clamp is that the clamp switch can be made p-channel and driven directly (by swapping the clamp switch and the capacitor in Fig. 1(b)) in some applications. In all other respects (such as steady state behavior, voltage stress on switches, reset mechanism etc.), both clamp approaches are similar. For the rest of this paper, only the flyback type clamp is considered due to its obvious advantages.

For flyback type clamp:

$$V_{cl} = V_{in} \frac{D}{(1-D)} \qquad 1(a)$$

For boost type clamp:

$$V_{cl} = V_{in} \frac{1}{(1-D)} = \frac{V_{in} \bullet D}{(1-D)} + V_{in} \qquad 1(b)$$

1.1 Active Clamp Technique Benefits

The benefits of active clamp/reset techniques can be summarized as below -

- No additional reset winding or dissipative clamps are required for transformer reset.
- Higher maximum duty cycle allows wider input voltage range or higher turns ratio.
- With higher turns ratio, current stresses on the primary side and voltage stresses on the secondary side can be reduced significantly.
- The energy stored in parasitic elements is transferred to tank elements and recycled, resulting in higher efficiency and lower noise.
- Switch voltage is clamped to a controlled level resulting in smaller (lower stress) switching devices.
- In forward converters, transformer core reset is provided.
- Zero Voltage Switching (ZVS) of the switches is possible, leading to higher efficiency and possible high frequency operation.
- The voltage stress across the switches is relatively constant (or concave shaped) over the full range of input voltage. This feature offers certain design trade-offs which are not available in other single-ended implementations due to the switch voltage stress being proportional to the input voltage.
- Another unique feature of this approach is that its transformer waveforms allow easy implementation of the synchronous switching technique on the secondary side.

1.2 Analysis of Operation - Forward and Flyback Active Clamp Converters

The active clamp technique is applicable to both types of isolated single-ended converter topologies - forward and flyback. Fig. 2 shows a generalized primary circuit of an active clamp converter (forward or flyback) with parasitic elements. The primary winding has magnetizing inductance L_m and lumped leakage inductance L_l in addition to the idealized transformer winding. The lumped leakage inductance (L_l) may also include an additional external series inductor placed to achieve

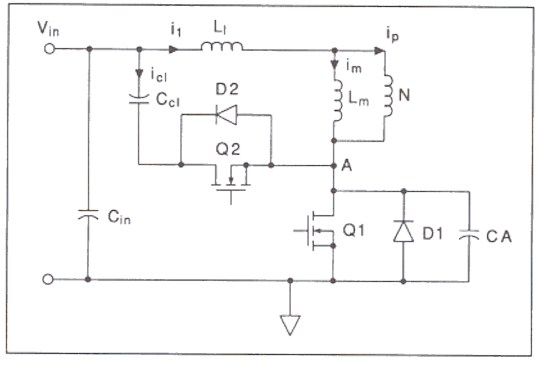

Figure 2. Primary side active clamp circuit with parasitic elements

soft switching transition. For the remainder of this paper, the terms series inductance and leakage inductance are used interchangeably and are meant to represent the effective series inductance reflected to the primary. D1 and D2 are parasitic anti-parallel diodes of switches Q1 and Q2 respectively. The parasitic junction capacitances of Q1 and Q2 are lumped together along with transformer intra-winding capacitance into a single capacitance CA representing equivalent capacitance at node A. In order to analyze the circuit behavior, its operation can be broken down into 4 major operating modes during a switching cycle. Within each mode, there are variations depending on converter type, operating conditions, circuit parasitics etc. which are briefly alluded to in this section. More detailed analyses of the individual converters is available in references[5,6]. Figs. 3 and 4 show corresponding timing diagrams for active clamp forward and flyback converters respectively.

Mode 1: Main Switch Conduction [t_0-t_1]

During this mode, the main switch (Q1) of the converter is on. The clamp capacitor (charged to V_{cl}) is disconnected from the rest of the circuit by virtue of the clamp switch and diode (Q2/D2) being off. The input voltage appears across the (non-ideal) primary winding. For a forward converter, the output rectifier is on and power transfer to output is taking place during this mode. Magnetizing current is linearly increasing. For a flyback converter, the

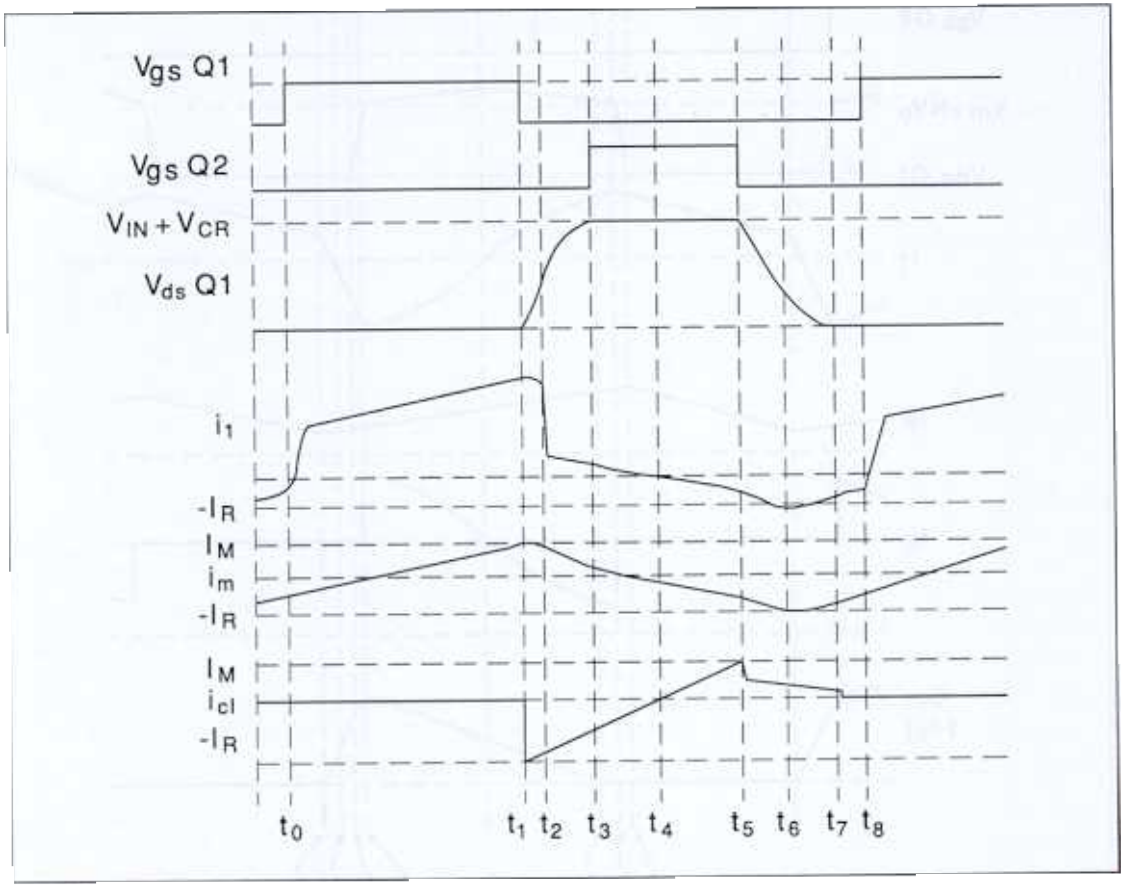

Figure 3. Steady-state waveforms of active clamp forward converter

output diode is reverse-biased in this mode, while the energy storage is taking place in the primary winding (both leakage and magnetizing inductances).

Mode 2: Turn-off Transition[t_1-t_3]

When Q1 is turned off, CA charges up to a voltage high enough to forward bias D2 (V_{in} + V_{cl}). Q2 should be turned on only after D2 has turned on to achieve zero voltage transition. For the forward converter, part of the charging is linear as reflected load current charges CA up to V_{in}. Beyond this point, output rectifier is off and stored leakage energy and magnetizing energy are sequentially used to charge CA up to V_{in} + V_{cl}. In a flyback converter, portions of the magnetizing and leakage inductance energy are utilized to accomplish the complete charging of CA. The output rectifier turns on during this transition and its current starts rising slowly due to the presence of leakage inductance.

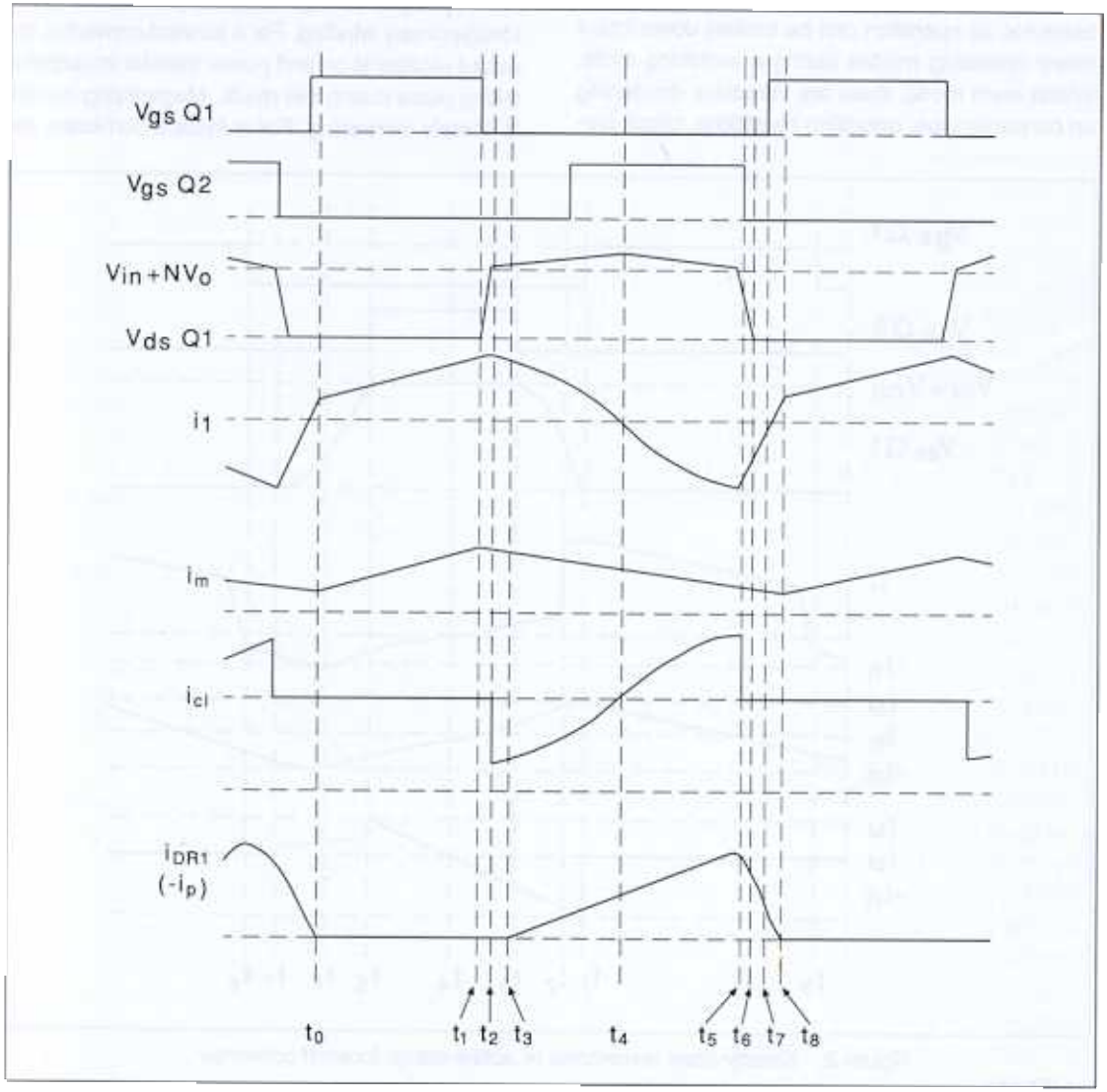

Figure 4. Steady-state waveforms of active clamp flyback converter

Mode 3: Clamp Circuit Operation [t_3-t_5]

During this mode, the clamp circuit (D2/Q2/C_{cl}) provides a low impedance path for most of the leakage inductance energy without allowing excessive ringing or power dissipation. When D2 conducts, the clamp capacitor is charged while negative voltage appears across the primary. At the same time, the clamp circuit current is decreasing in a resonant manner. The resonant frequency is determined by the clamp capacitance and some combination of magnetizing and leakage inductances depending on the converter topology. Once the clamp circuit current reaches zero, it is allowed to reverse if Q2 has been turned on. For the duration of Q2 conduction, energy is transferred back to the magnetizing and/or leakage inductances and the clamp capacitor is discharged back to its steady-state value. For a forward converter, the output is disconnected from the primary during this mode. Hence, L_m and L_l appear in series and L_m (due to its higher value) plays dominant role in energy transfer phenomenon. For a flyback converter, the magnetizing inductance is clamped to reflected output voltage and most of the magnetizing energy is being transferred to the output during this mode. Energy transfer takes place between clamp capacitance and leakage inductance. Some of the clamp circuit energy is also transferred to the load.

Mode 4: Turn-on Transition [t_5-t_8]

When Q2 is turned off, the reverse current flowing in leakage and/or magnetizing inductances begins to discharge CA. To achieve ZVT turn-on of Q1, CA has to be completely discharged before Q1 can be turned on. For a forward converter, energy in magnetizing and leakage inductances is available up to the point when CA is discharged to V_{in}. Beyond this point, the output diode gets forward biased and diverts the magnetizing energy to output. Higher level of leakage inductance can delay this diversion sufficiently to allow complete discharge of CA. In addition, primary leakage inductance energy (which can be augmented by adding an external series inductance) still contributes completely to the transition process. It should be noted that the series and leakage inductances have a detrimental effect of reducing effective duty cycle. For a flyback converter, only the energy stored in primary leakage inductance is available for discharge of CA.

It is clear that certain distinctions must be made when applying the active clamp technique to forward or flyback converters. One such distinction is that during the transitions from main switch conduction to the clamp circuit operation, the equivalent circuit conditions are not the same. Also, in the forward converter, the transformer magnetizing energy is not supplied to the output. In the forward converter, the transformer reset should be ensured under all operating conditions, which restricts the inductance that can be added in series with the primary winding. In the flyback converter, the active clamp circuit alters the operating waveforms significantly. As shown in the last waveform of Fig. 4, the output diode current (i_{DR1}) has an inverted slope and higher peak compared to the conventional flyback converters. The active clamp circuit provides immediate path for the current i_1 to be diverted at instant t_3 while the output current (reflected as i_p) rises slowly. In Fig. 4, i_{DR1} (=-i_p) is the difference between i_m and i_1 and all currents are drawn to the same scale. The current i_m is dictated by the voltage across L_m and the current i_1 is dictated by the resonance effect during mode 3.

2. Power Stage Design Procedure

In order to understand the practical issues and trade-offs involved in the design of active clamp circuits, a detailed step-by-step power stage design procedure is presented in this section. Where appropriate, application of this procedure is illustrated for design examples of active clamp forward and flyback converters with universal AC input voltage and 15V, 100W output.

Input Voltage Range Considerations

The required input voltage range of any power supply impacts its cost, size and performance significantly. Wider input voltage range imposes higher component stresses, wider duty cycle operation and potentially lower efficiency on a given design. However, in the global marketplace, universal voltage range operation presents a significant marketing advantage. In addition, hold-up time

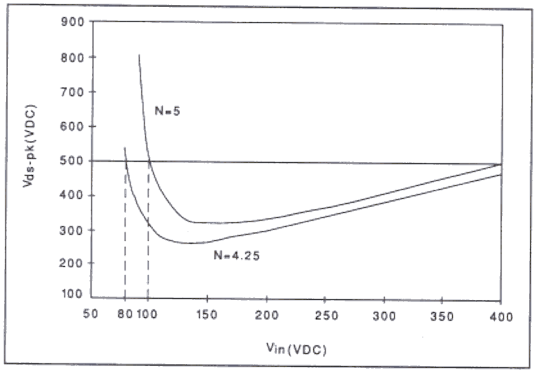

Figure 5. Effects of input voltage range and turns ratio on switch voltage stress

requirements in some systems force wider input voltage range as a compromise against increasing hold-up capacitor values to a very high level.

As mentioned earlier, active clamp circuits offer wider input voltage range operation by allowing maximum duty cycle to go above 50% and allowing wider duty cycle range. The drawback of going to wider input voltage range is that it can force a lower turns ratio or higher voltage stresses on switching devices. This fact is illustrated by the curves of peak voltage stress vs. input voltage in Fig. 5. The plots shown in Fig. 5 are for an off-line 100W active clamp forward converter with 15V output. For a 100-400V input range, N=5 can be used with peak voltage stress of 500V. To reduce the capacitance required at the input, some designs may require lower minimum input voltage. In this case, a turns ratio of 5 can result in prohibitive voltage stresses at low lines as shown. The only recourse in such instance is to settle for a lower turns-ratio (e.g. N=4.25) which allows the peak stress to be about the same (500V) for input voltage range of 80-400V. The lower turns ratio does result in higher current stress on the primary side and higher voltage stress on secondary rectifiers.

Step 1: Select input voltage range

In the present case, an input voltage range of 85-400 VDC is considered. For a universal input voltage range of 85-260 VAC, the rectified peak DC voltage range is 120-375 V. To allow for voltage droop at full load with a reasonable size input filter capacitor, $V_{in}(min)$ is selected to be 85V. $V_{in}(max)$ of 400V allows for a direct interface to a PFC front-end with a regulated output DC voltage of 380V ±5%.

Step 2: For a given output voltage V_o, determine the required min. secondary voltage (V_{sec}) using eqn. 2.

$$V_{sec} = V_o + V_F + I_o r_s \quad (2)$$

where V_F is the output diode forward drop, r_s is the secondary path resistance and I_o is the output current. V_{sec} = 15 + 1 = 16V in the present example.

Step 3A: Select turns ratio (Forward Converter)

From Fig. 5, it can be seen that the voltage stress (V_{ds}-peak) on the switching devices tends to have a concave shape over the input voltage range. In order to minimize the stress over the input voltage range, the design goal should be to ensure that the stress at minimum and maximum input voltages is equal. By doing that, proper design optimization (maximum N) can be achieved without generating excessive voltage stresses. The design procedure for this step is derived as follows.

Design Goal: $V_{ds}@V_{in}(min) = V_{ds}@V_{in}(max)$

$$\text{From eqn.1(a), } V_{ds} = V_{in} + V_{cl} = \frac{V_{in}}{(1\text{-}D)} \quad (3)$$

$$\frac{V_{in}(min)}{1\text{-}D_{max}} = \frac{V_{in}(max)}{1\text{-}D_{min}} \quad (4)$$

$$D_{max} = \frac{N(V_{sec} + V_{ll})}{\quad} \quad (5)$$

$$D_{min} = \frac{N(V_{sec} + V_{ll})}{V_{in}(max)} \quad (6)$$

where V_{ll} is the equivalent drop in the leakage inductance(L_l) approximated by:

$$V_{ll} = L_l I_o f_s \quad (7)$$

Combining equations (4-6), results in:

$$N(V_{sec} + V_{ll}) = \frac{V_{in}(max)V_{in}(min)}{V_{in}(max) + V_{in}(min)} \qquad (8)$$

From equation 8, the value of N can be determined. Initially, V_{ll} can be ignored and the value of N can be revisited once the final value of L_l is known. For the example circuit under consideration -

16N = 400 • 85/(400+85) => N = 4.38.

In many cases, the calculated value of N can be a value which is not practically achievable. N is then selected to be the closest practical value below the calculated value. The resulting value of V_{ds} at $V_{in}(max)$ will be higher than V_{ds} at $V_{in}(min)$. Selecting N above the calculated value from eqn. (8) is not recommended as it can lead to a high maximum duty cycle. Once N is selected, maximum duty cycle and maximum voltage stress on the devices can be determined using equations (5) and (9) respectively.

$$V_{ds}(max) = \frac{V_{in}(max)^2}{V_{in}(max) - N(V_{sec} + V_{ll})} \qquad (9)$$

In the present example, N = 4.28 is used based on practically achievable turns ratio of 30:7, D_{max} = 4.28 • 16/85 = 0.81 and $V_{ds}(max) = (400)^2/(400-69)$ = 483V.

If the D_{max} resulting from eqn. (5) is too high, N can be recalculated based on a more practical value of D_{max}. It should be realized that for the active clamp converters, D_{max} must be tightly regulated. The above equations should account for any variations in D_{max} . From eqn. 1(a) and Fig. 5, it is clear that at low input voltages, the clamp voltage tends to rise at a high rate. By controlling the maximum duty cycle, this rise is prevented.

Step 3B: Select Turns Ratio (Flyback Converter)

For a CCM flyback converter, the turns ratio is not determined by max. duty cycle and secondary voltage. Reflected output voltage can be higher than input voltage for D>0.5. As a result, higher turns ratio is possible to reduce the secondary voltage stress. However, going to a very high turns ratio can be detrimental to the circuit performance. High N will increase the maximum duty cycle at low input voltages. It will also increase the voltage stress on the main switch that is approximately given by V_{in} +NV_o. High value of N also results in a very high primary inductance that can shift the RHP zero of the converter to a lower frequency forcing a low bandwidth system. For the flyback converter under consideration, a turns ratio of N=6 is chosen. This choice results in Dmax of 0.53 and V_{ds}(max) of ~500V.

Step 4: Switching Frequency Selection

The switching frequency determines many of the converter performance metrics. In general, higher switching frequency leads to smaller magnetics and faster loop response of the converters. Choice of switching frequency is often dictated by the particular application and its size, cost and schedule/risk constraints. The ZVS characteristics of active clamp circuits can be exploited to push the switching frequency higher without corresponding increase in switching losses. While successful power supply designs operating at switching frequencies up to 1 MHz have been developed with these techniques, not all switching losses are eliminated in the active clamp circuits. For example, the switch turn-off losses, gate drive losses and output rectifier switching losses are proportional to switching frequency. In addition, possible magnetics size reduction at higher switching frequency requires careful evaluation. It should also be remembered that the circuit parasitics at higher switching frequency are less predictable and have a larger impact on the converter performance. For the purpose of the prototype circuit, a switching frequency of 200 kHz is chosen.

Step 5A: Transformer Design (Forward Converter)

The input volt-seconds for the transformer are known once N is selected. For the selected switching frequency, optimum Ferrite material should be selected to minimize core losses. Magnetics Inc.'s K material, TDK's PC-40 material or 3F3 material

from Philips are optimal choices for frequencies in the 200-500 kHz range. From the core loss data of the material, an acceptable level of flux excursion is selected. In the present example, with 200 kHz switching frequency and Mag Inc's K material as the Ferrite of choice, limiting the core losses to an acceptable level(260 mW/cm^3) allows the flux to operate at a maximum flux level(B_{max}) of 0.1T(1000G). One important characteristic of the active clamp converter is that it allows flux excursion in the first and third quadrants of the B-H curve. This has the effect of making core loss consideration the limiting factor in B_{max} choice instead of the possibility of saturation. In other words, the steady state flux excursion is well below the saturation level for the given ferrite. It will be shown later in this paper that transient conditions can cause flux excursions which may take the core closer to saturation in some cases. With the knowledge that $\Delta B = 2B_{max}$, the product of primary turns N_p and cross sectional area is determined using Faraday's law:

$$N_p A_e = \frac{V_{in} \bullet DT_s}{\Delta B} \qquad (10)$$

Selection of a proper sized core is an iterative process starting with eqn. 10. It involves choice of current density, conductor types, winding methods, core geometries, trade-off between copper and core losses etc. Simple spreadsheet routines can be written to assist in this process. For the forward converter design example, this process resulted in the choice of EE-43007 core (30mm x 30mm) with A_e = 0.6 cm^2 and V_e = 4 cm^3. With a predetermined N of 4.28, it yields N_p = 30 and N_s = 7. The window utilization (with bobbin) is lower than optimum, but leaves room for an additional bias winding. Standard magnet wire (AWG17 for secondary and AWG23 for primary) was used. For higher frequency and higher current circuits, Litz wire and/or copper foils should be considered.

Magnetizing Inductance Considerations (To gap or not to gap)

One salient feature of the active clamp forward converters is that they utilize the magnetizing energy for soft switching of the power switch. While transformers for conventional forward converters do not have any airgap, transformers for active clamp circuits are usually gapped in order to reduce the magnetizing inductance. If the transformer is not gapped, there is no impact on steady state operation of the active reset circuit, but the soft transition is difficult to achieve and the transformer is more exposed to the possibility of saturation under transient conditions. The peak magnetizing current of the transformer increases as a result of gapping. This magnetizing current adds to the reflected load current flowing through the main switch. It also increases circulating energy in the clamp circuit during the main switch off time. For the prototype forward converter circuit, using spreadsheet calculations, it was determined that the magnetizing current peak of 0.8A (compared to reflected peak load current of 1.55A) provided the optimum trade-off between conduction losses and switching losses for the given application. It results in a magnetizing inductance of 214µH and gapping of 0.317 mm for the selected core. Effects of different levels of gapping are presented in the results section to illustrate the effect of varying L_m.

Step 5B: Transformer Design (Flyback converter)

For the flyback converter, the transformer design is based on the requirement that the magnetizing energy supports the output during main switch off time. The core is always gapped for the flyback transformer. It is desirable that the active clamp circuit maintains the flux in the first quadrant of the B-H loop. The magnetizing inductance is picked so that it maintains CCM operation at the light load condition. The equation for L_m is:

$$L_m = \frac{\eta \bullet [V_{in} \bullet D \bullet T_s]^2}{2P_o(min) \bullet T_s} \qquad (11)$$

where η is the conversion efficiency, P_o(min) is the minimum output power, T_s is the switching period and D is the duty cycle at input V_{in}. The core gap is determined for the given L_m based on the core geometry and standard inductance equation. In the present example, the core selected is the same as the one for the forward converter. It

results in L_m value of 863µH with a gap of 0.0787 mm. The number of turns is 30 for the primary and 5 for the secondary.

Step 6: Semiconductor Selection

The peak voltage stress on the main and auxiliary switches is the sum of V_{in} and V_{cl}. While the clamp voltage can be calculated from eqn. 1(a), it should be remembered that it assumes a large value of clamp capacitance. As will be discussed in step 7, it is more practical to use a smaller C_{cl} and allow it to have additional ripple which adds to the peak voltage stress on the switches. As a rule of thumb, a 10-15% ripple should be acceptable. The selection of switching device for Q1 involves a trade-off between lower conduction losses and higher switching losses. Selection of low $R_{ds}(on)$ FETs helps keep conduction losses low, but results in higher parasitic capacitances. Higher capacitances make the task of achieving ZVS more difficult and add to the turn-off and gate drive losses. Lower $R_{ds}(on)$ switches also imply larger die size and higher cost. For this application, 600V, size 5 MOSFETs with 0.5-0.6 ohms of on resistance are chosen. The auxiliary switch (Q2) in a forward converter carries only the magnetizing current during the off time. It should be chosen as small as feasible to lower cost and gate-drive requirement, especially since it requires a floating drive circuit. For the flyback converter, however, the circulating current is much higher and it normally requires Q2 to be the same size as Q1. The output rectifiers, DR1 and DR2, for the forward converter are sized to handle voltage stresses of $V_{cl}(max)/N$ and $V_{in}(max)/N$ respectively. For the flyback converter, the output rectifier current becomes discontinuous due to the presence of clamp circuit (Fig. 4) and the RMS secondary current is higher. Hence, the output rectifier is larger compared to the one used in a conventional flyback converter.

Step 7: Clamp Circuit component selection

Selection of clamp circuit components is another critical design choice for optimal performance of the active clamp circuits. The leakage inductance value(and choice of additional series inductor) influences the zero voltage switching. For the flyback converter, additional series inductance is almost a necessity as the magnetizing inductance is not available to resonate CA down to zero. Even for a forward converter, the series inductance is the main contributor to zero voltage switching of the main switch at high input voltages. A high leakage inductance value delays the transfer of power to the output when the main switch is turned on and results in effective duty cycle loss in a forward converter. For a flyback converter, the duty cycle loss is not a concern, but higher L_l results in higher conduction losses. It should also be ensured that $L_l << L_m$ for minimizing switch voltage stress. Equations provided in step 9 describe the impact of the choice of L_l on circuit performance.

For analysis of the steady state operation of active clamp circuits, it is assumed that the clamp capacitor, C_{cl}, is large enough to approximate V_{cl} as a voltage source for the particular operating point. However, per eqn. 1(a), V_{cl} changes with the input voltage. Under transient conditions, V_{cl} has to be able to adapt quickly to changing operating conditions, requiring smaller C_{cl}. For example, in a forward converter, at minimum input voltage, V_{cl} is at its maximum. If the input voltage goes up abruptly and V_{cl} does not change fast enough, total stress across the switches (V_{in} +V_{cl}) can go higher than the designed steady state value. Similarly, when the duty cycle changes as a result of load removal, a high V_{cl} can continue to supply reset flux (negative volt-seconds) to the transformer when there is no forward flux. Neglecting any damping resistances, the resultant circuit can be approximated as a resonant circuit with L_m and C_{cl}. For given value of L_m, it can create a peak reverse magnetizing current given by following equation:

$$I_{m(rev)} = \frac{V_{cl}}{Z_{ca}\cos(\theta)} \tag{12}$$

where

$$Z_{ca} = \sqrt{\frac{L_m}{C_{cl}}} \tag{13}$$

and

$$\theta = \tan^{-1}\left(-\frac{Z_{ca}I_m}{V_{cl}}\right) \quad (14)$$

I_m is the magnetizing current peak under normal conditions and signifies nominal flux excursion. The peak-peak ripple voltage on the clamp capacitance is given by following equation:

$$V_{rip} = \left|\frac{V_{cl}}{\cos(\theta)}\right| - V_{cl} \quad (15)$$

Higher value of C_{cl} increases the $I_{m(rev)}$ value while V_{rip} is reduced. For the forward converter design under consideration, design curves are plotted in Fig. 6 where $I_{m(rev)}$ is normalized with respect to I_m. The $I_{m(rev)}$ values are plotted for low line conditions when V_{cl} is at its highest value giving the worst case conditions. On the other hand, the ripple voltage is plotted for its maximum values at the high line condition, when V_{cl} is lowest. These plots show that to keep the flux excursion to within 3 times the nominal value, ripple of about 70V must be tolerated. Based on Fig. 6, the value of C_{cl} selected for the present design is 9.4 nF.

For a flyback converter, the resonance during clamp circuit operation is limited to L_l and C_{cl} as L_m does not participate in the resonance. Therefore, the value of C_{cl} used in the flyback circuit must be greater to maintain the same low resonant frequency. The voltage ripple on the capacitor is also

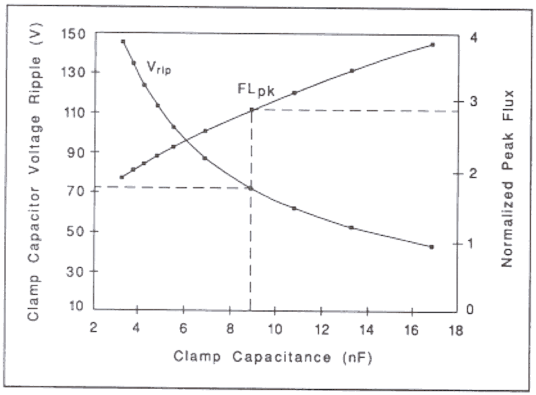

Figure 6. Effect of clamp capacitor value on switch voltage ripple and peak flux

reduced as a consequence. However, the current in the clamp circuit is higher for the flyback converter and the clamp capacitor has to be sized appropriately.

Step 8: Selection of other components

The input capacitor value for a rectified AC input with minimum peak value of V_{pl} and desired minimum DC voltage V_{min} is given by:

$$C_{in} = \frac{P_{in}(max)}{(V_{pl}^2 - V_{min}^2) \bullet f}\left[1 - \frac{\cos^{-1}\left(\frac{V_{min}}{V_{pl}}\right)}{\pi}\right] \quad (16)$$

where f is the input line frequency. For 60 Hz AC in with 85-260V RMS range, V_{pl} is 120V and for V_{min} of 85V, C_{in} works out to 173µF per 100W of input power.

For the forward converter, the output inductor is calculated using the standard equations based on the specified boundary of CCM operation. For the 20:1 load range, the inductance required to maintain CCM operation is calculated to be 100µH. The output capacitor calculation is also based on standard equations. However, in most high frequency converters, the output capacitor selection is based on cost, size and reliability constraints. Specifically, with the Aluminum Electrolyte capacitors most commonly used for cost and reliability purpose, the determining factor in capacitance selection is the contribution of the capacitor ESR to the output voltage ripple and deviation during transient load conditions. This is especially true for the active clamp flyback converter. With its high level of ripple current in the output capacitor, the output capacitor needs to have very low ESR levels.

Step 9: Zero Voltage Switching Design considerations

The time delay introduced between turn-off of one switch and turn-on of the other switch allows zero voltage turn-on of the switches. To derive conditions for zero voltage switching, certain assumptions are made. These include idealized (lumped) leakage and magnetizing inductances of the transformer, lumped parasitic capacitance and zero switching times of the switches.

Forward converter delay calculations:

Turn-off transition:

At the instant when the main switch is turned off, the primary switch current is the sum of the reflected load current(I_{op}) and positive peak of the magnetizing current(I_m). Assuming that the output filter inductor and magnetizing inductance are large enough, the parasitic capacitance at node A (CA in Fig. 2) charges up at a constant rate until its value equals V_{in}. This time is given by:

$$t_{2\text{-}1} = \frac{CA \bullet V_{in}}{(I_{op} + I_m)} \qquad (17)$$

This time will be longer for light load conditions and will also be proportional to V_{in}. For the forward converter being designed, with a 20:1 load range, at light load (0.33A) and high line (400V), this time works out to 262 ns. Beyond this point, CA continues to charge, now resonating with (L_m+L_l). It charges up till it reaches V_{in}+V_{cl} at which point D2 turns on. The equation for this phase is:

$$t_{3\text{-}2} = \frac{\sin^{-1}(V_{cl}/I_m Z_c)}{\omega} \qquad (18)$$

where

$$Z_c = \sqrt{\frac{(L_m + L_l)}{CA}} \qquad (19)$$

$$\omega = \sqrt{\frac{1}{(L_m + L_l) \bullet CA}} \qquad (20)$$

Since V_{cl} is inversely proportional to V_{in}(eqn. 1), this time decreases as input voltage increases and is independent of the load. For the converter under discussion, $t_{3\text{-}2}$ is 282 ns at low line. The sum of $t_{2\text{-}1}$ and $t_{3\text{-}2}$ gives t_{d1}(min) which is the time delay from the instant Q1 is turned off to turn-on of D2. Once D2 conducts, Q2 can be turned on with zero voltage across it. Thus, for the ZVS turn-on of Q2, minimum delay from Q1 turn-off to Q2 turn-on is given by the maximum value of ($t_{2\text{-}1}$ + $t_{3\text{-}2}$) under all operating conditions(calculated to be 337 ns in the current example). The conduction of D2 is feasible only till the current in the clamp branch reaches zero and tries to reverse direction. Q2 has to be turned on prior to this point to allow current reversal and discharge of C_{cl}. This sets the maximum time of delay from Q1 turn-off to Q2 turn-on. Assuming symmetrical clamp circuit current, this time is approximately half the off-time of the main switch, which is easily calculated for the forward converter for a given input voltage. Off-time is shortest at maximum duty cycle (low line) and in the present example, it is 966 ns. This sets up a window of 337 ns-483 ns for the Q1-to-Q2 delay for getting ZVT of Q2 under all operating conditions.

Turn-on transition:

When auxiliary switch (Q2) is turned off, the magnetizing current is at its negative peak (-I_m) and v_{CA} is at V_{in}+V_{cl}. Disconnection of Q2 results in a simple resonant circuit with initial conditions as shown in Fig. 7. CA is resonantly discharged till v_{CA} reaches V_{in}. The equations for this mode are:

$$v_{CA} = V_{in} + V_{cl} \frac{\cos(\phi + \omega t)}{\cos(\phi)} \qquad (21)$$

$$i_m = V_{cl} \frac{\sin(\phi + \omega t)}{Z_c \cos(\phi)} \qquad (22)$$

where

$$\phi = \tan^{-1}\left(\frac{Z_c I_m}{V_{cl}}\right) \qquad (23)$$

The time duration for this mode is derived by equating v_{CA} to V_{in} and solving for t:

$$t_{6\text{-}5} = \frac{\pi}{2\omega} - \frac{\phi}{\omega} \qquad (24)$$

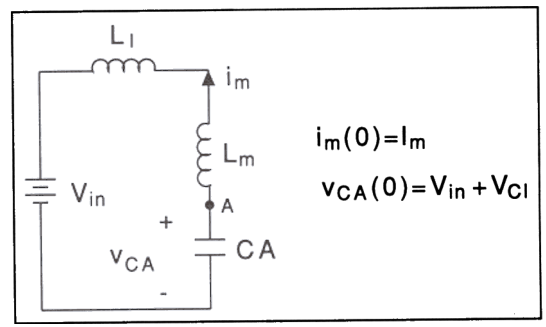

Figure 7. Resonant circuit with initial conditions

The current at that instant is given by:

$$I_{MA} = \frac{V_{cl}}{Z_c \cos\phi} \quad (25)$$

When voltage at node A reaches V_{in}, the voltage across the transformer falls to zero. This has the potential to turn the output diode (DR1) on and divert the magnetizing current to the output. As a result, the discharge of CA is abruptly slowed down. If the effects of primary and secondary leakage inductances are ignored, then I_{MA} is instantaneously diverted to the output and v_{CA} stays at V_{in}. In some designs, transformer magnetizing current is made large enough such that I_{MA} is larger than the reflected full load current. In that case, the excess current is still available to discharge CA down to zero. However, this approach increases the primary circulating current significantly. When practical leakage inductances are considered, the situation improves substantially.

First of all, the secondary leakage inductance slows down the transfer of the magnetizing current to secondary. Whatever current is not diverted to the load, continues to discharge CA below V_{in}. Also, the energy stored in the primary leakage inductance is still available to discharge CA as it is not clamped to the output. In many designs, an additional primary series inductance is added to facilitate zero voltage switching. Another approach has been to delay the current transfer to output by placing a saturable reactor in series with the output rectifier [3].

As can be seen, there are many avenues available for the designer to ensure zero voltage turn-on. It should be realized that all these approaches come at the expense of increased conduction losses and/or reduced duty cycle for power transfer. These trade-offs should be carefully considered for each individual design. In some low voltage DC-DC converter applications, it can be argued that the advantages of ZVS do not outweigh the additional conduction and duty cycle losses. In these applications, the active clamp approach is still advantageous because of the reduced switch voltage and higher duty cycle capability in comparison to dissipative clamps and clamp windings.

The energy required to facilitate ZVT can be calculated based on the lumped model of the transformer. In the previous paragraph, the impact of primary and secondary leakage inductances on the switching transition has been described as if they were separate physical entities. However, in reality, the transformer leakage inductance is a distributed parameter which can be lumped for analytical purposes. As illustrated in Fig. 8, the leakage inductance(L_l) is lumped in the primary for the sake of simplicity. After t_6, the primary side resonance involves CA and L_l with initial conditions of $i_l = I_{MA}$ and $v_{CA} = V_{in}$. Solving for this resonance, we get:

$$v_{CA} = V_{in} - I_{MA} Z_{c2} \sin(\omega_2 t) \quad (26)$$

$$i_l = -I_{MA} \cos(\omega_2 t) \quad (27)$$

$$Z_{c2} = \sqrt{\frac{L_l}{CA}} \quad (28)$$

$$\omega_2 = \sqrt{\frac{1}{L_l \cdot CA}} \quad (29)$$

It can be seen that for v_{CA} to be able to get down to zero, $I_{MA} \cdot Z_{c2}$ has to be greater than V_{in}. At higher values of V_{in}, this may require very high leakage inductance which will cause considerable

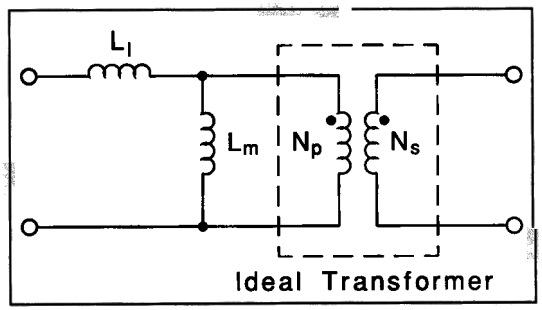

Figure 8. Transformer lumped model with parasitic inductances

duty cycle loss. The time required to get to zero voltage is given as:

$$t_{7\text{-}6} = \frac{1}{\omega_2} \sin^{-1}\left(\frac{V_{in}}{I_{MA} Z_{c2}} \right) \quad (30)$$

The above analysis is based on the assumption that CA is a constant. However, since CA represents FET output capacitance (plus some other parasitic capacitances), its value is nonlinear with respect to the voltage across it. Taking this non-linearity into account, the ZVS of main switch is possible with lower values of L_l. It is not possible to get a linear equation with the variable capacitance model. However, total energy required to discharge a FET capacitance from voltage V_{in} can be calculated as given in [8]:

$$E_{dis} = \frac{2}{3} C_x \sqrt{V_x} V_{in}^{1.5} \quad (31)$$

where C_x is the specified capacitance at the voltage V_x and V_{in} is the actual starting voltage. Normally, FET capacitances are specified at a voltage of 25V. From the energy standpoint, if the energy stored in the leakage inductance at t_6 is higher than E_{dis}, it is possible to discharge CA to zero. The energy in L_l is given by:

$$E_{leak} = \frac{1}{2} L_l I_{MA}^2 \quad (32)$$

For the prototype converter in this paper, simple spreadsheet calculations show that based on eqns. 26-29, it is not possible to achieve ZVS with a leakage inductance as high as 20% of the magnetizing inductance at high line voltage. However, when eqns. 31 and 32 are used, even with a leakage inductance which is 5% of the magnetizing inductance, ZVS is shown to be possible. However, the calculation of ZVS time is not feasible due to the non-linear capacitance. For this, a first cut approximation can be used by calculating an equivalent capacitance based on energy model:

$$\frac{1}{2} C_{eq} V_{in}^2 = \frac{2}{3} C_x \sqrt{V_x} V_{in}^{1.5} \quad (33)$$

and substituting C_{eq} in place of CA in eqns. 28-29. With the new values, eqn. 30 is applied to get the time ($t_{7\text{-}6}$) required to discharge C_{eq} from V_{in} to 0.

In the situations where the full ZVT turn-on is not achieved, the reduced voltage at turn-on still offers significant efficiency improvements. Eqn. 31 indicates the amount of energy that is dissipated at turn-on if the time-delays are not used. With the introduction of optimum time-delays, the difference between eqn. 31 and 32 is the energy lost if the leakage energy is not sufficient to discharge CA. It will be shown in the experimental results section that the goal of ZVS *under all conditions* is not always practical and can result in lower efficiency compared to designs where partial discharge of CA is achievable without excessive loss of duty cycle.

Flyback Converter Delay Calculations

Turn-off Delay:

When the main switch turns off in a flyback converter, the voltage across it rises at a rate dictated by I_m. There is no reflected load condition as in a forward converter. Due to the high value of Lm and short duration of charging, this is approximated as a linear charging with the time duration given by:

$$t_{2\text{-}1} = \frac{CA \bullet (V_{in} + V_{cl})}{I_m} \quad (34)$$

Referring to Figs. 2 and 4, at t2, diode D2 turns on and allows zero voltage turn-on of Q2 beyond this time. As in the forward converter, diode conduction can be approximated by half the off-time of the main switch and that gives the maximum timing window for Q2 turn-on.

Turn-on Delay:

When Q2 is turned off in an active clamp flyback converter, the negative peak leakage current is available to discharge the capacitance at node A. While the magnetizing inductance remains clamped to the output, resonance between L_l and CA continues until CA is completely discharged,

assuming that there is sufficient energy in L_l make it happen. Unlike the forward converter, there is no diversion of current to the output and L_m plays minimal role in this transition. Even though L_l is much smaller than L_m, the starting negative current for this resonance is higher than the I_m or I_{MA} values in forward converter.

3. Control Circuit Design

All the control functions required to effectively implement active clamp circuits are incorporated in the control IC UCC3580. A block diagram of UCC3580 is shown in Fig. 9. The IC contains an oscillator, precision reference, error amplifier, PWM comparator and logic, protection circuitry and two outputs (OUT1 and OUT2) with programmable delay or dead-time between them. OUT2 is available in inverted form (versions -1 and -2) for direct coupled drive of a P-channel auxiliary switch in boost clamp configurations. Depending on the power stage configuration, the outputs are used to drive the main and auxiliary switches (Q1 and Q2) in the active clamp circuits directly or through gate drive transformers.

Oscillator Set-up

The oscillator is configured to allow accurate settings of maximum duty cycle and switching frequency independent of each other. Simplified oscillator block diagram and waveforms are shown in Fig. 10. OSC1 and OSC2 pins are used to program the frequency and maximum duty cycle. Capacitor CT is alternately charged (through R1) and discharged (through R2) between levels of REF/3 and 2 • REF/3. The charging and discharging equations

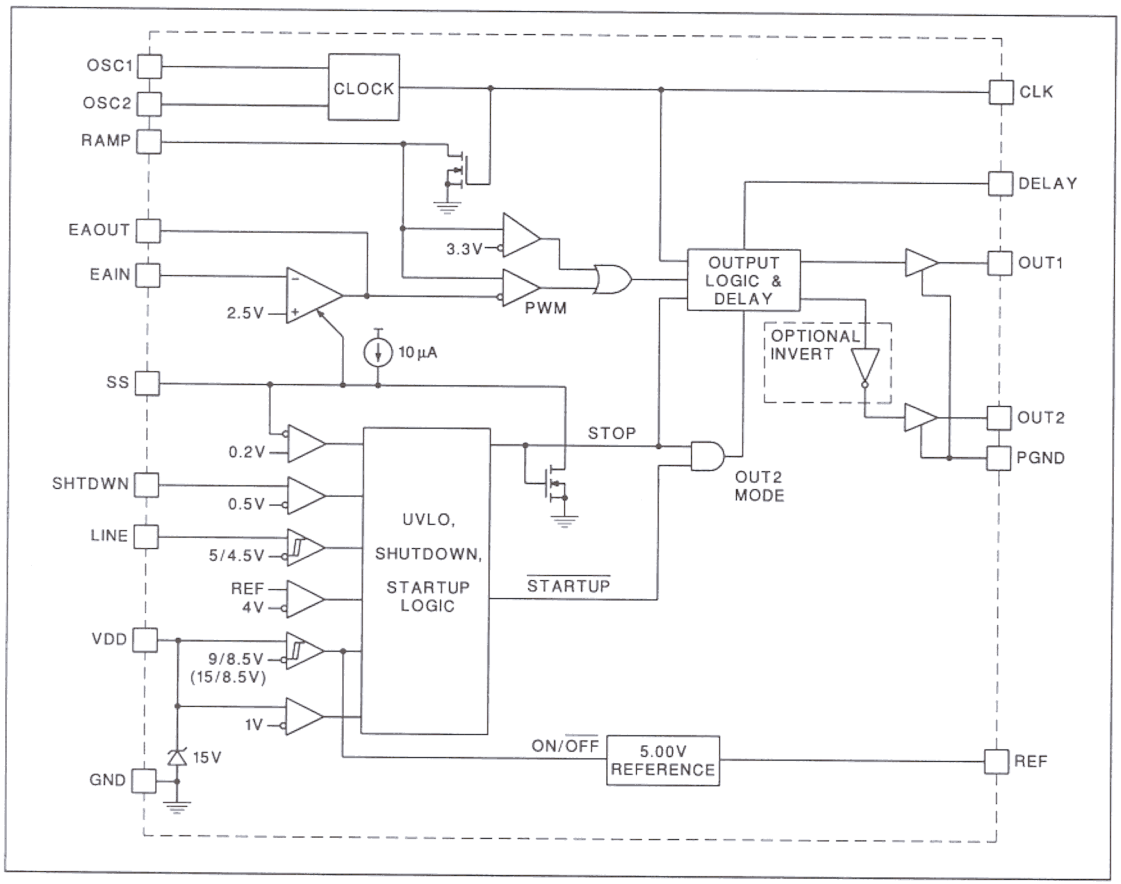

Figure 9. Simplified block diagram of the UCC3580

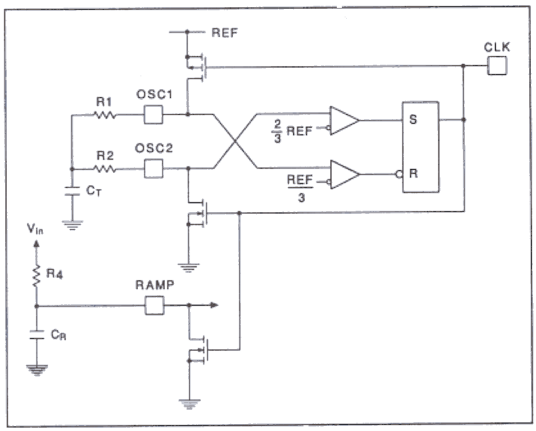

Figure 10(a). Simplified oscillator and ramp circuit of the UCC3580

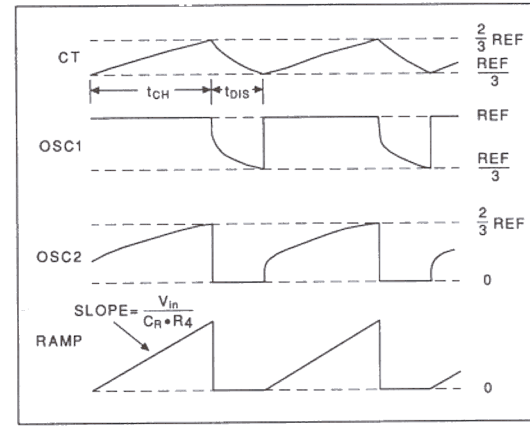

Figure 10(b). Oscillator and ramp circuit waveforms of the UCC3580

for CT are given by:

$$V_c(\text{charge}) = \text{REF} - \frac{2}{3}\,\text{REF}\, e^{-\frac{t}{\tau_1}} \qquad (35)$$

$$V_c(\text{charge}) = \frac{2}{3}\,\text{REF}\, e^{-\frac{t}{\tau_2}} \qquad (36)$$

where $\tau_1 = R1 \bullet C_T$ and $\tau_2 = R2 \bullet C_T$

The charge and discharge times are given by:

$$t_{CH} = 0.693 \bullet R1 \bullet C_T \qquad (37)$$

$$t_{DIS} = 0.693 \bullet R2 \bullet C_T \qquad (38)$$

The CLK output is high during the discharge period. It blanks the output to limit the maximum duty cycle of OUT1 and also discharges the RAMP capacitor. The frequency and maximum duty cycle are given by:

$$\text{freq} = \frac{1.44}{(R1 + R2) \bullet C_T} \qquad (39)$$

$$D_{max} = \frac{R1}{R1 + R2} \qquad (40)$$

Choosing CT = 100 pF and for D_{max} = 0.81 and freq = 200 kHz, we get R2 = 58.3k and R1 = 13.68k.

Voltage Feedforward and Volt-Second Clamp

UCC3580 has a provision for input voltage feedforward. As shown in Fig. 10, the ramp slope is made proportional to input line voltage by converting it into a charging current for CR. This provides a first order cancellation of the effects of line voltage changes on converter performance. The maximum volt-second clamp is provided to protect against transient saturation of the transformer core. It terminates OUT1 pulse when the RAMP voltage exceeds 3.3V.

$$\partial V_{ramp} = \frac{V_{in} \bullet dt}{R4 \bullet CR}$$

By setting the ramp current at high line(400V) to 2 mA, we get R4 = 200 k. The ramp voltage swing is restricted to 3V under nominal conditions to prevent the volt-second limit from interfering with normal operation. Substituting values at low line (85V) and D_{max} (0.81) in eqn. 41, we get CR of 560 pF.

UVLO and Start-up

For self biased off-line applications, -2 and -4 versions (UVLO on and off thresholds of 15V and 8.5V typical) of the IC are recommended. For all other applications, -1 and -3 versions provide lower on threshold of 9V. The IC requires a low start-up current of only 160µA when VDD is under the UVLO threshold, enabling use of a large trickle-charge resistor (with corresponding low power dissipation) from the input voltage. In the present example, a 600k (1/2 W) resistor allows sufficient start-up current at 75V input. VDD has an internal clamp at 15V which can sink up to 10 mA. The internal reference (REF) is brought up once the UVLO on threshold is crossed. The startup logic ensures that LINE and REF are above and SHTDWN is below their respective thresholds before outputs are asserted. LINE input is useful for monitoring actual input voltage and shutting off the IC if it falls below a programmed value. A resistive divider should be used to connect the input voltage to LINE input. This function protects the converter components from excessive currents at low line voltages. In the prototype circuit, the resistive divider (R5, R6) is programmed to allow operation at 75V input voltage. For LINE to be 5V at 75V input, R5 = 140k and R6 = 10k.

The soft-start pin provides an effective means to start the IC in a controlled manner. An internal current of 20µA starts charging a capacitor connected to the SS pin once the startup conditions listed above have been met. The voltage on SS pin effectively controls maximum duty cycle on OUT1 during the charging period. OUT2 is also controlled during this period (Fig. 11). Negation of any of the start-up conditions causes SS to be discharged immediately. Internal circuitry ensures full discharge of SS (to < 0.3V) before allowing charging to begin again (provided all the start-up conditions are met again).

Output Configurations

The UCC3580 family of ICs is designed to provide control functions for single-ended active clamp circuits. For different implementations of the active clamp approach, different drive waveforms for the two switches (main and auxiliary) are required. The -3 and -4 versions of the IC supply complementary non-overlapping waveforms (OUT1 and OUT2) with programmable delay which can be used to drive the main and auxiliary switches. Most active clamp configurations will require one of these outputs to be transformer coupled to drive a floating switch. The -1 and -2 versions have

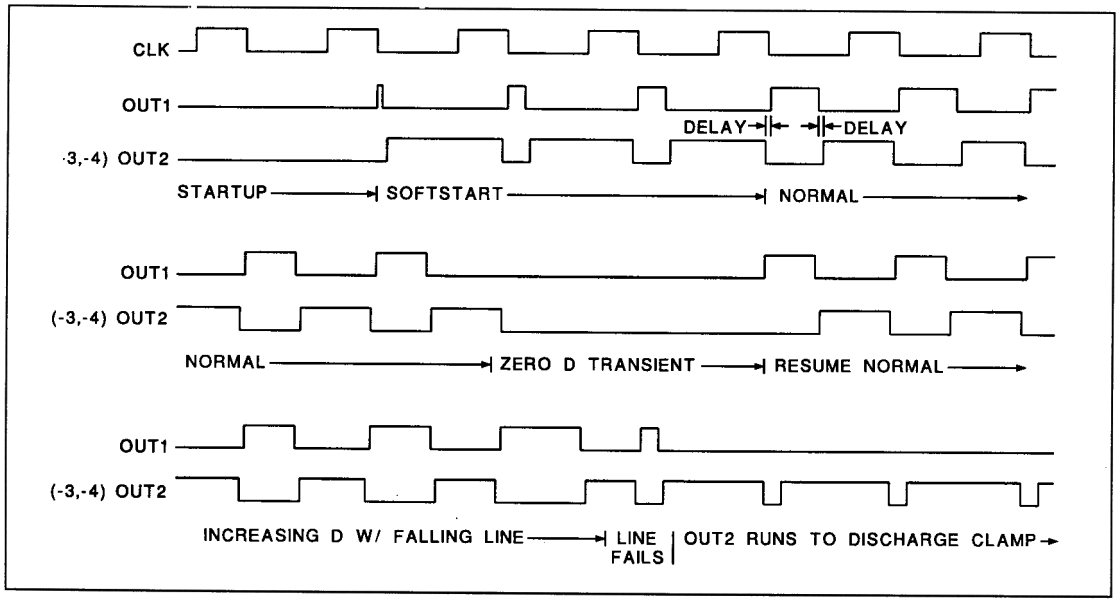

Figure 11. Output waveforms of the UCC3580 under different operating conditions

the phase of OUT2 inverted to give overlapping waveforms. This configuration is suitable for capacitively coupled driving of a ground-referenced P-channel auxiliary switch with the OUT2 drive while OUT1 is directly driving an N-channel main switch.

The programmable delay can be judiciously used to get zero voltage turn-on of both the main and auxiliary switches in the active clamp circuits. For UCC3580, a single pin is used to program the delays between OUT1 and OUT2 on both sets of edges. Figure 11 depicts the relationships between the outputs in a graphical manner.

The driver stage of UCC3580 has 1A peak turn-off current and 0.5A peak turn-on current for OUT1 and 0.3A peak drive current for OUT2. These drivers provide easy interface for controlling power MOSFET switches. In many applications, one of the switches (main or aux) is floating with respect to ground. In these cases, a transformer coupled drive circuit is required. The gate drive transformer should have low leakage and high magnetizing inductance for effective control of the switches.

Output Behavior during Fault modes

The UCC3580 family is designed to protect the power converter components against faults such as input line dropout, output overcurrent, etc. All these fault conditions are latched and require full soft-start recycling. The IC does not provide cycle-by-cycle current limiting as duty cycle hiccups can cause instabilities and/or cross-conduction in the active clamp type circuits. The IC has instead, a smart output sequencing feature to protect against transients. When the error amplifier output commands low duty cycle (of OUT1) as a result of load transient, the IC senses it and drives both switches (main and aux) off. As a result, the steady state operating conditions (such as clamp capacitance voltage) are not abruptly changed. In all other cases, normal logic prevails where OUT2 (-3,-4) is a true complement of OUT1 with delay (dead) times between them. When LINE goes low, OUT1 goes to zero duty cycle, but OUT2 (-3,-4) keeps pulsing at full duty cycle (switching period - 2 delay periods) in order to discharge the clamp capacitance to zero and prepare for full soft-start cycle.

As described earlier, the UCC3580 incorporates input voltage feedforward and maximum volt-second clamp. These features are useful in voltage mode controlled systems for preventing core saturation and providing first order cancellation of the input voltage change effects. In peak current-mode control systems, the cancellation of input voltage is automatically obtained. UCC3580 is also usable in a peak current-mode control system if the switch current signal is fed to the ramp pin. However, the maximum volt-second clamp feature is no longer available in this case. If the peak current signal is derived from resistive sensing, the ramp peak will be very low. With the use of a current transformer, ramp signal amplitude can be made larger to give better noise immunity. The UCC3580 internal circuitry is optimized for voltage mode feedforward operation and hence, the modulator gain, error amplifier range and noise immunity are sacrificed in the peak current-mode control application with resistive sensing.

Small Signal Behavior of Active Clamp Circuits

The small signal models of the active clamp circuits are marginally different from the corresponding single-ended circuits. Ideal clamp circuit does not interfere with the control-to-output transfer function of the forward converter. However, due to non-ideal nature of the clamp circuit, the available closed loop bandwidth is impacted [9]. It has been shown that the crossover frequency should be before the complex pole-pair introduced by L_m and C_{cl}. High value of C_{cl} forces the crossover frequency to be very low, in addition to posing core saturation potential during transients as discussed earlier.

With the voltage feedforward control, the open loop control-to-output transfer function of a buck-derived converter is given by:

$$G_d(s) = \frac{R4 \bullet CR}{T_S} \cdot \frac{1 + \frac{s}{s_{zl}}}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}} \qquad (42)$$

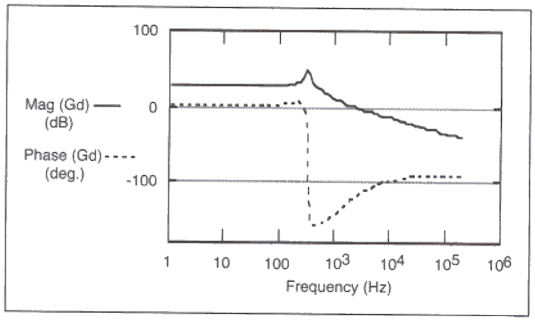

Figure 12(a). Control-to-output gain and phase plots of the forward converter

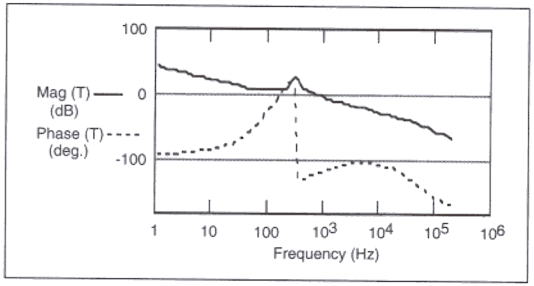

Figure 12(b). Loop gain and phase plots of the forward converter

where

$$\omega_0 = \frac{1}{\sqrt{L_f C_f}} \quad (43)$$

$$Q = \frac{R_0}{\omega_0 L_f} \quad (44)$$

$$s_{z1} = \frac{1}{R_{esr} \cdot C_f} \quad (45)$$

C_f and L_f are the output filter components, R_{esr} is the ESR of the output capacitor and R_o is the load resistance. R4, CR and T_s are already defined earlier. The double pole response of the open loop gain is best compensated using a feedback compensation network with 3-poles and 2-zeroes as shown in Fig. 13. The pole at DC gives high DC gain, two zeroes are placed before the resonant frequency of the output filter to provide sufficient phase boost and the high frequency poles offer ESR zero cancellation and high frequency roll-off.

For the present design, with C_f = 2500µF and L_f = 100µH, the double pole is at 325 Hz and ESR zero is estimated at 8.333 kHz. Q is about 20 for the full load. The DC-gain from eqn. (42) works out to 22.5. The compensation is designed so that cross-over occurs at about 800 Hz with sufficient phase margin. Figs. 12(a) and (b) provide the expected gain and phase plots for the control-to-output transfer function and loop gain of the converter respectively. From Fig. 12(b) it can be seen that the phase margin is 60° at the crossover frequency of 823 Hz.

For a flyback converter, the major effect of the clamp circuit is that C_{cl} is added in parallel to the actual output capacitance to determine the effective resonant frequency of the system. If the reflected clamp capacitance is negligible compared to the output capacitance, the effect is not noticeable. Also, due to higher series inductance of the active clamp circuit and associated duty cycle loss, the RHP zero of the open loop control-to-output gain is shifted lower. The RHP zero being difficult to compensate for, sets the maximum attainable bandwidth in this case.

4. Experimental Results

An experimental forward converter circuit with flyback type active clamp was designed using the design procedure outlined in sections 2 and 3. The complete circuit schematic is provided in Fig. 13. The circuit was breadboarded and its performance evaluated over a range of operating conditions. The measured efficiency is in the range of 88.5-89% at full load.

Operating waveforms of the converter are shown in Figs. 14-16. All plots are for the operating conditions of 170V input voltage and 60W output power. Fig. 14 shows primary-side switching waveforms with primary current (i_1) on top and the V_{ds} and V_{gs} of Q1 as the bottom waveforms. Fig. 15 shows the V_{ds} and V_{gs} waveforms on an expanded scale to get a better look at the Q1 turn-on transition. Fig. 16 shows the clamp circuit current (top waveform, i_{cl}) and the V_{ds} of Q1 with its ripple voltage measured using cursors. Figs. 14(a)-16(a) show the waveforms for nominal (optimized) conditions for this converter, which include magnetizing inductance(L_m) of 212µH and leakage

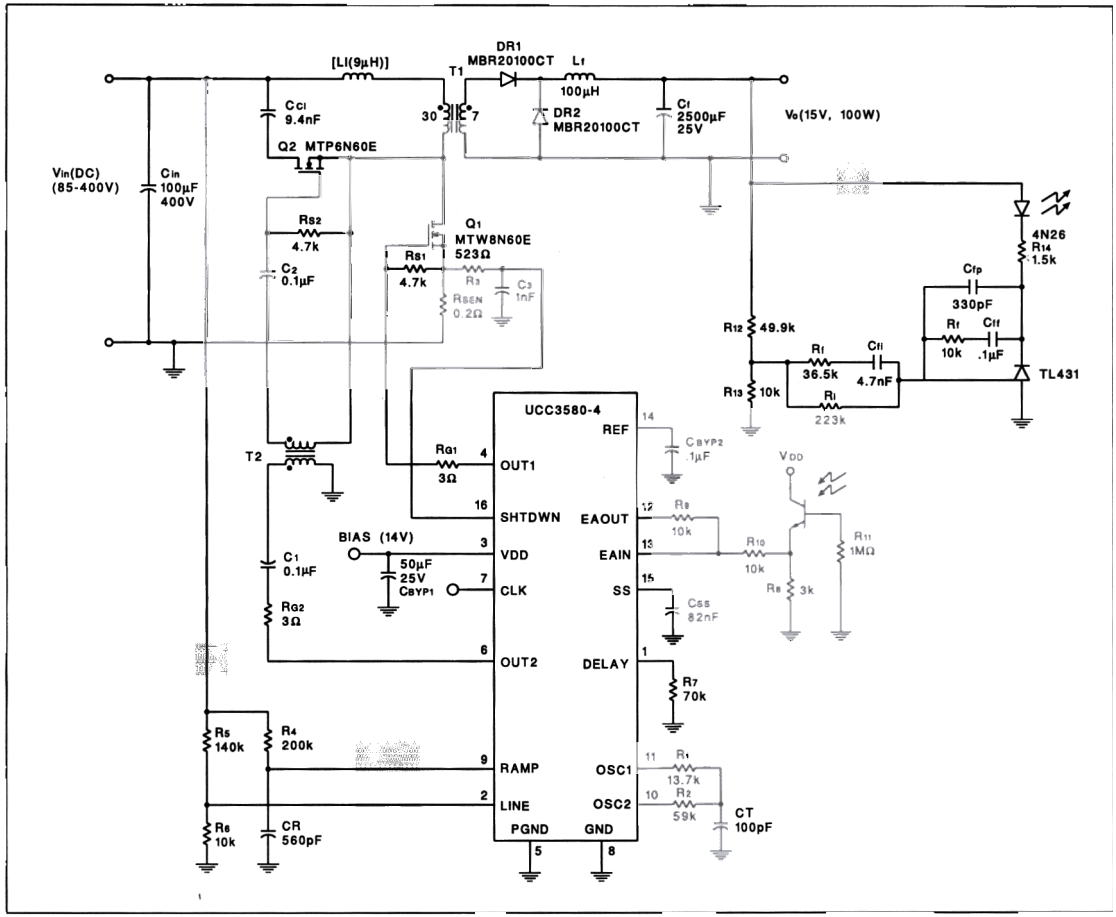

Figure 13. Detailed circuit schematic of the experimental forward converter

inductance(L_l) of about 2.5μH. The clamp capacitance(C_{cl}) is 9.4 nF. In Fig. 14(a), the current waveform indicates reflected load current of 1A and peak magnetizing current of 0.8A as designed. The steady state V_{ds} value is 274V with a D of 0.4 which matches the values derived from eqn. 1. Figs. 14(b)-16(b) show the effect of adding an external series inductance of 9μH (making total L_l = 11.5μH) which helps facilitate soft turn-on transition of Q1. As can be seen from Fig. 14(b), the actual duty cycle widens to 0.43 in this case for the same operating conditions. This effect is attributed to the loss of effective duty cycle introduced by the additional inductance. The steady-state V_{ds} is impacted and it is higher by 20V in this case. The impact on peak current levels is insignificant, but the slopes of the current waveform during switching transition are observed to be less steep as a result of higher series inductance. Figs. 14(c)-16(c) are for the conditions where the magnetizing inductance is reduced to 140μH while maintaining the 9μH series inductance. As shown in Fig. 14(c), the peak of the magnetizing current goes up by about 50% to 1.5 A. Finally, Fig. 14(d)-16(d) are for the conditions of lower magnetizing inductance and no additional series inductance. Fig. 15(a) shows that the resonant transition stops at about 100V before the switch is turned on, thus indicating a non-ZVS turn-on condition. With an added inductance, Vds can go down to a lower value(60V)

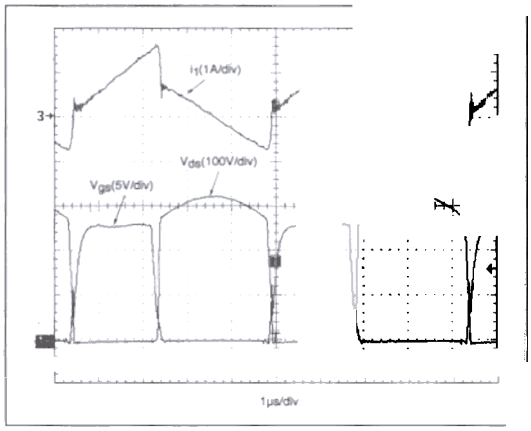

Figure 14(a). L_m = 212µH, L_l = 2.5µH

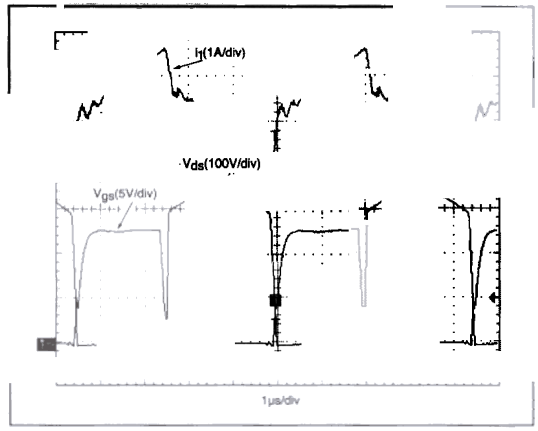

Figure 14(b). L_m = 212µH, L_l = 11.5µH

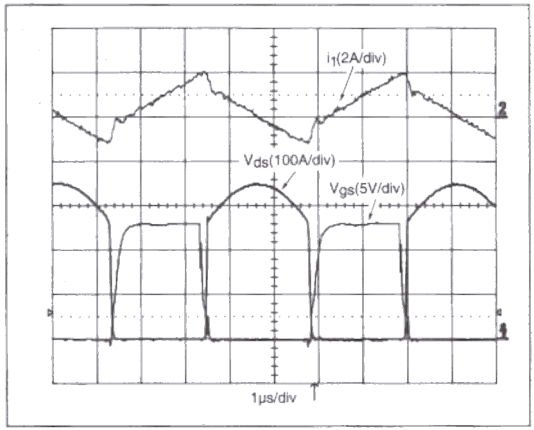

Figure 14(c). L_m = 140µH, L_l = 11.5µH

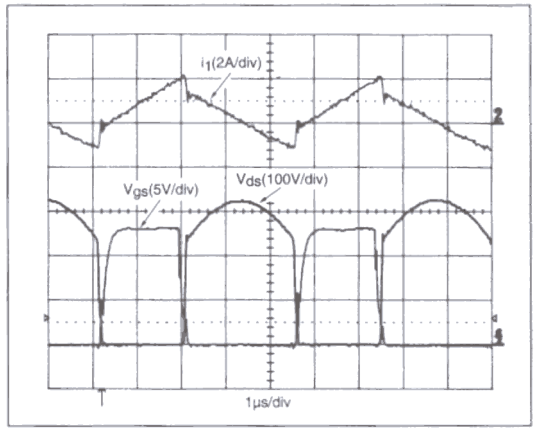

Figure 14(d). L_m = 140µH, L_l = 2.5µH

Figure 14. Primary side switching waveforms of the experimental converter

even if starts from a higher value as shown in Fig. 15(b). The resonant transition allows true ZVS for the circuit conditions depicted in Fig. 15(c). However, the circuit efficiency in this case is actually lower due to the higher peak current and loss of duty cycle contributed by the series inductance. As shown in Fig. 15(d), the lower magnetizing inductance contributes to a faster discharge (to 70V) of CA compared to Fig. 15(a) before the switch turn-on. From Figs. 16(a) and (b), it is seen that the V_{ds} voltage ripple is 50V for the nominal L_m and C_{cl} of 9.4 nF. By changing the L_m to a smaller value, the ripple voltage goes up to 80V. (Figs. 16(c) and (d)). Figs. 16(b) and (c) also show the spike contributed to the clamp circuit current by the additional inductance which also contributes to the conduction losses. Finally, the impact of a change in C_{cl} is illustrated in Fig. 16(e) where C_{cl} is increased from 9.4 nF to 11.5 nF and the ripple is reduced to 66V from 80V in Fig. 16(d).

An experimental flyback converter was also designed and built using the design procedure outlined in this paper. Major changes from the forward converter circuit included a flyback transformer (same core size), modification to the output circuit for flyback configuration, higher series inductance (13.5 µH), larger clamp switch (MTW8N60E) and larger clamp capacitor (0.1 µF). Other than the compensation circuit, most of the other control circuitry remains unchanged from the one shown in Fig. 13.

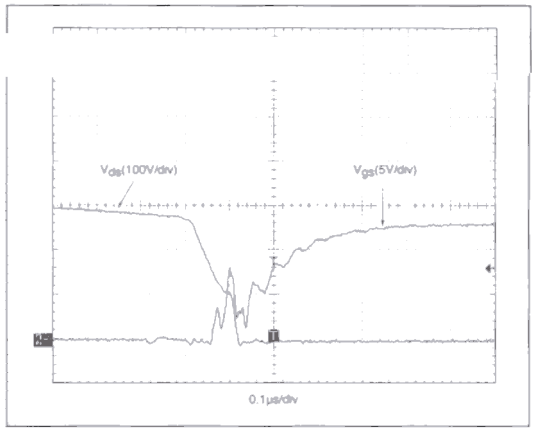

Figure 15(a). L_m = 212μH, L_l = 2.5μH

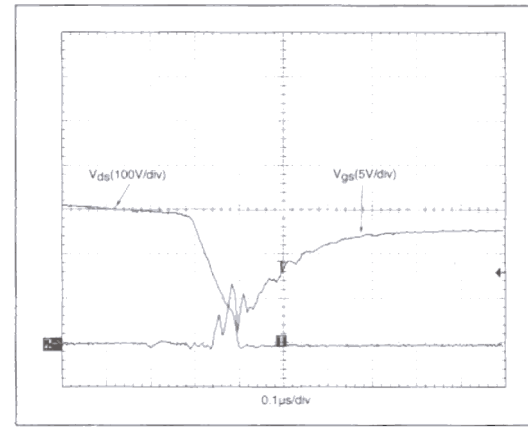

Figure 15(b). L_m = 212μH, L_l = 11.5μH

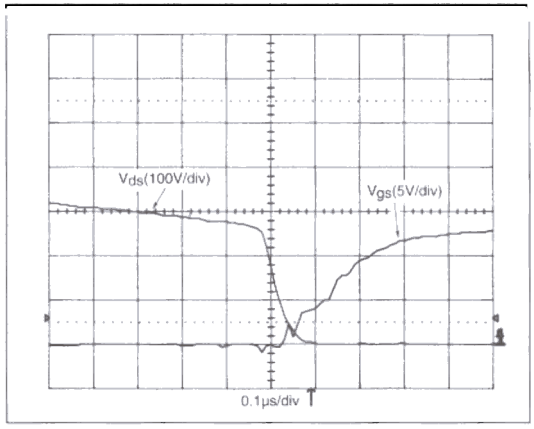

Figure 15(c). L_m = 140μH, L_l = 11.5μH

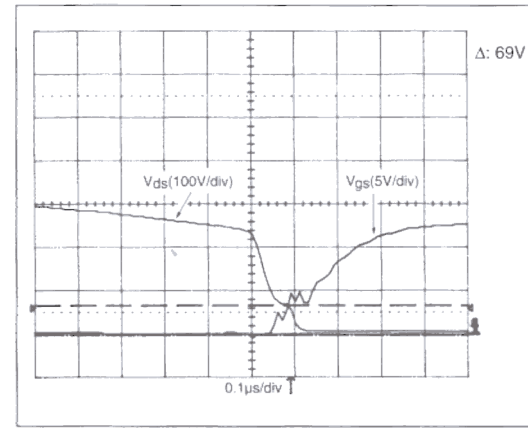

Figure 15(d). L_m = 140μH, L_l = 2.5μH

Figure 15. Expanded primary side waveforms (turn-on transition)

The converter efficiency was in the 83% range at low line (85V) and half load (50W) condition. The efficiency is lower compared to the forward converter due to higher ripple current as discussed in section 2. Some experimental waveforms of this circuit are shown in Fig. 17 for the same operating condition. It can be seen from the bottom waveform that the main switch drain to switch voltage is extremely well-clamped (in the absence of any snubbers). The top waveform also shows the higher level of clamp circuit current in this implementation.

Conclusions

Practical issues related to the active clamp techniques have been presented in this paper. A step by step design procedure is included as a guide for designing active clamp forward and flyback converters. Many of the performance trade-offs faced when designing real life converters have been highlighted and quantified as appropriate. Practical results are given to illustrate the effects of certain design choices on the converter performance.

The advantages of the active clamp circuits have been outlined and verified with a working lab prototype. The active clamp technique provides a great avenue for enhancing the performance of the single-ended converters. These performance enhancements include switch voltage clamping, higher duty cycle operation, lossless switching and reduced EMI. The additional circuit complexity

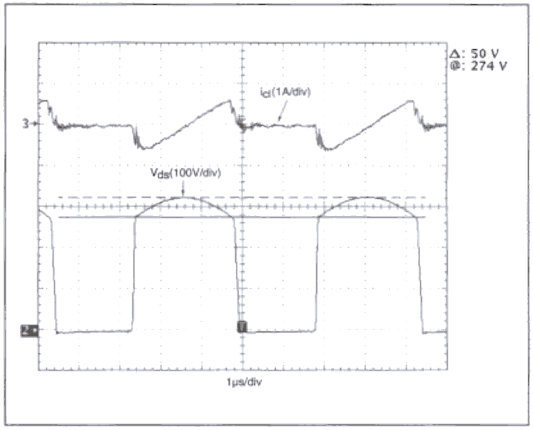

Figure 16(a). L_m = 212μH, L_l = 2.5μH

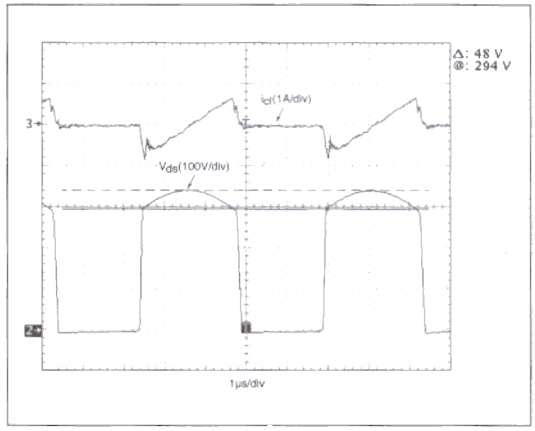

Figure 16(b). L_m = 212μH, L_l = 11.5μH

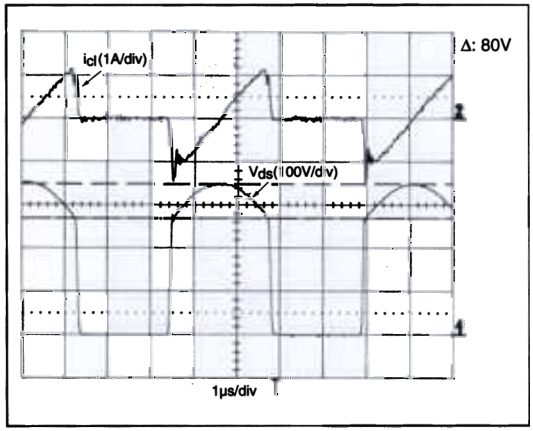

Figure 16(c). L_m = 140μH, L_l = 11.5μH

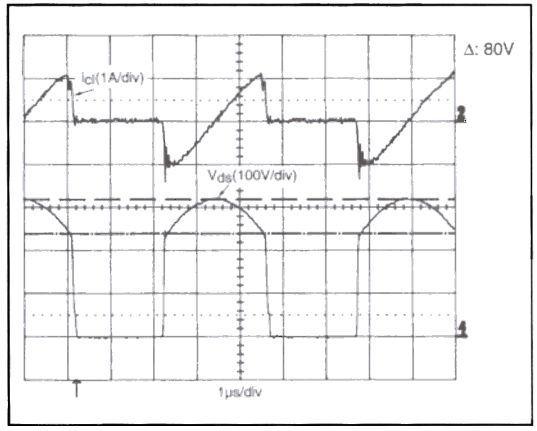

Figure 16(d). L_m = 140μH, L_l = 2.5μH

Figure 16. Clamp circuit current and switch voltage ripple

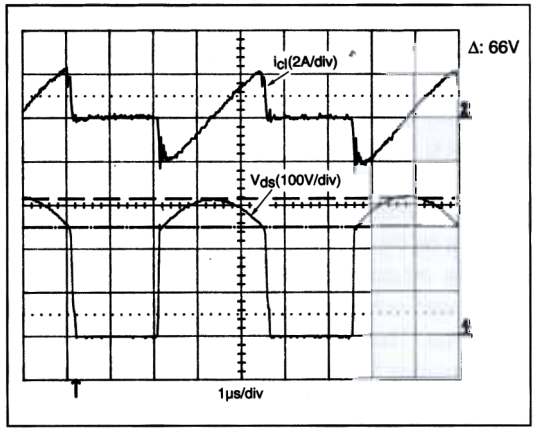

Figure 16(e). Effects of C_{cl} increase (9.4nF to 11.5nF)

introduced by the active clamp circuit is easily offset by these advantages. In lower power converters, the complexity can be reduced by using the boost type clamp circuit with p-channel switches.

In the past, the implementation of active clamp converters involved using conventional PWM controllers and additional logic and drive circuits. However, such discrete implementations did not fulfill some of the accuracy requirements specific to the active clamp circuits such as maximum duty cycle clamp, timing delays and unique protection circuits. A new control IC which facilitates easy implementation of the active clamp converters has

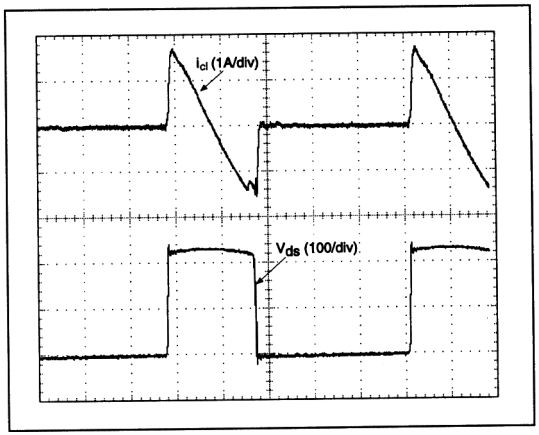

Figure 17. Clamp circuit current and main switch voltage for Active Clamp Flyback Converter

been described. It is shown that the optimization of active clamp forward and flyback converters is easily achievable with the use of this new control IC - UCC3580.

Acknowledgments

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