

# DACx0501 Delivers Multichannel Output using External S&H for Battery Test Equipment and Oscilloscope



Demultiplexing a single DAC output with external Sample and Hold circuit provides multitude of benefits: from being ultra-low cost per channel to providing channel level customization. Understanding the design trade-offs of this solution helps one strike the right balance between cost and performance.

End equipments such as [Battery Test Equipment](#) and [Oscilloscope](#) require precision control and calibration signals to achieve the target system accuracy. Precision DACs are typically used to generate these signals. The complexity and multi-module nature of these systems drive the need for multiple precision signals. For example, a multichannel [Battery Test Equipment](#) needs at least two analog signals per channel. On the other hand, an [Oscilloscope](#) needs at least 10 analog signals for various signal conditioning functions such as offset and gain control. The common approach for generating these signal is by using a multichannel DAC. But the cost constraint on these applications drives alternative approaches. One way to generate these signal is to use a single channel DAC with multiple sample and hold (S&H) circuits. With proper design, the user can generate a highly cost effective solution that can also provide a customized number of channels. The channels can be configured to provide outputs at different ranges and accuracy. We will discuss the fundamentals and the key parameters that can help design this solution in an optimized way. [Figure 1](#) shows a simplified circuit diagram of this solution.

## Theory of Operation of Sample and Hold

A basic sample and hold circuit consists of a signal source (DAC in this case), a switch, a capacitor, and a buffer. As the name suggests, the circuit has two modes of operation: sample and hold. In sample mode, the switch is closed connecting the DAC output to the hold capacitor  $C_H$ . The capacitor charges or discharges to the sampled DAC output. In hold mode, the switch opens disconnecting the DAC output from the capacitor  $C_H$ . Thus, the final output is held to the sampled value due to the charge stored on the hold capacitor  $C_H$ . The output buffer is needed for delivering the required current. In a practical circuit, the switch leakage and the amplifier input bias current make the capacitor drift from the stored value. Hence, we need to refresh the S&H circuit periodically even if the DAC value does not change. The refresh interval depends on the voltage drift target of the system.

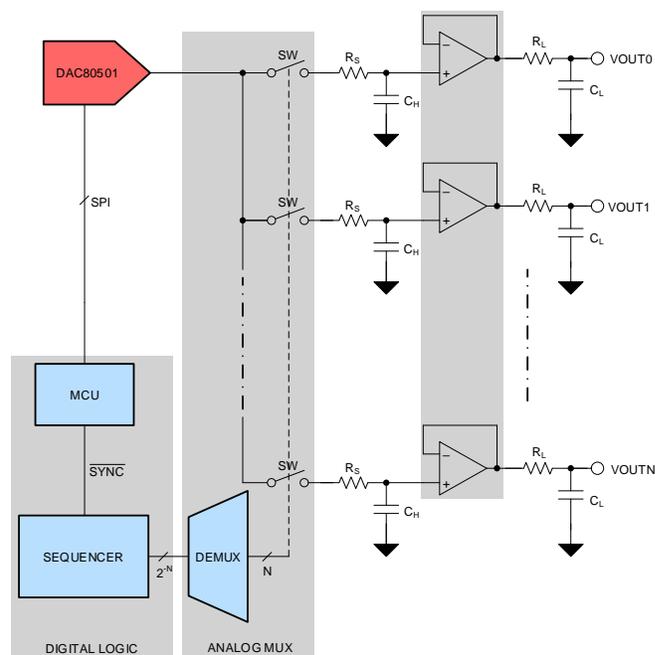


Figure 1. Block Diagram of Multichannel DAC using S&H

## Key Design Parameters

The main design parameters of an S&H are *Charge Injection*, *Voltage Droop*, and *Settling Time*. These three parameters in turn determine the key performance of this solution.

**Charge Injection:** refers to the charge induced on the hold capacitor due to the parasitic capacitance of the switch during the sample to hold transition. This charge results in a dc voltage that adds to the offset error at the output of each channel.

**Voltage Droop:** results from the hold capacitor leakage caused by the switch leakage resistance and the bias current of the output buffer. This error determines the minimum refresh rate of the S&H circuit.

Both Charge Injection and Voltage Droop can be minimized by increasing the value of the hold capacitor  $C_H$ . Increase in the value of  $C_H$  impacts the settling time of the system and the stability of the DAC output. A series isolation resistor  $R_S$  can be used for improving the stability of the DAC buffer. Note that the switch itself has an on-state resistance of the order of few ohms.

**Settling Time:** The total settling time of this circuit is determined by the setting times of the DAC, the S&H circuit ( $R_{ON-Switch} + R_S, C_H$ ), the output buffer, and the output filter ( $R_L, C_L$ ). A detailed derivation of the settling time equation can be found in [TIPD142](#).

**Update Rate:** The update rate of the multichannel system implemented using the S&H approach can be calculated by multiplying the settling time per channel with the number of channels in the system. Thus, it is imperative to optimize the settling time per channel for the highest update rate.

**Total Unadjusted Error (TUE):** The offset and gain errors are the biggest contributor to the TUE. The linearity is dominated by the choice of precision DACs. In most cases the linearity error from the DAC is negligible compared to the offset and gain errors. The offset error of the system is determined by the amount of charge injection as described above. The gain error of the system depends on the gain setting of the output buffer. The calculation of TUE is shown in [Equation 1](#).

$$TUE = \sqrt{(INL)^2 + (GainError)^2 + (OffsetError)^2} \quad (1)$$

**Crosstalk:** The channel to channel crosstalk is a critical parameter in some multichannel systems. This parameter refers to the voltage change on an output channel when other channels are being updated. This parameter depends on the component selection and PCB layout. We will discuss the component selection aspects in the next section.

### Component Selection

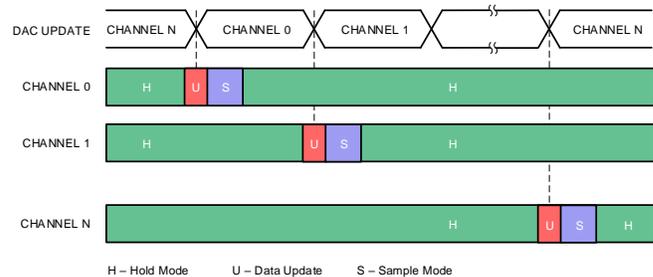
**DAC:** The DACx0501 is a 16-/14-/12-bit family of DACs in a tiny 2mm x 2mm package. It has an internal reference and the DAC can be programmed using SPI or I2C with hardware pin selection. The DAC can drive a 2-nF capacitor directly. With low temperature coefficient and an output settling time of 5- $\mu$ s, this DAC is a perfect choice for this application.

**Switch:** The switch plays an important role in the S&H circuit. The key parameter to minimize for this component are charge injection and leakage current. Alternatively, an analog multiplexer can be used instead of a switch. This works well for the systems where crosstalk is not critical.

**Hold Capacitor:** The hold capacitor should have high insulation resistance, low temperature coefficient, and low dielectric absorption. Low temperature coefficient NP0/C0G ceramic capacitors are most suited for this purpose.

**Output Buffer:** The key parameter for the amplifier in this system is low input bias current and low temperature coefficient. Additionally, channel to channel crosstalk must be low when using multichannel amplifier parts.

**Digital Logic:** The S&H circuit requires digital control signals apart from the SPI or I2C interface to the DAC. Typically, these signals are generated by the microcontroller ( $\mu$ C). Alternatively, a binary counter or a sequencer can be used to drive the switch in order to reduce the burden on the  $\mu$ C. A dedicated low-cost  $\mu$ C might be the best option to reduce both software and hardware load from the main controller. [Figure 2](#) shows a typical timing diagram of the update and refresh process of the S&H based multichannel circuit.



**Figure 2. Timing Diagram of the Refresh Cycle**

### Conclusion

With challenging cost constraints driven by the aforementioned applications, which go as low as sub-dollars per channel, alternative multichannel approaches come to the rescue. Using Sample and Hold for generating multichannel analog outputs provides multiple benefits as well. This approach provides the flexibility to the user to customize the number of channels and channel-specific parameters. One of the key components in this approach is the precision DAC. The optimized feature set and high performance attributes of DAC80501 combined with tiny package and an integrated reference makes it an ideal choice for the precision signal source.

**Table 1. Key Part Number Suggestions**

Component	Part Number
DAC	<a href="#">DAC80501</a>
Output Buffer	<a href="#">OPA4317 (Quad)</a>
Switch	<a href="#">TS12A4515 (SPST)</a>
Analog Mux	<a href="#">TS3A5017 (SP4T)</a>
Microcontroller	<a href="#">MSP430FR2xxx</a>

### References

- [TIPD142: Sample & Hold Glitch Reduction for Precision Outputs Reference Design](#)
- [TIDA-00760: Multi-Channel Analog Output Module With Multiplexed Single-Channel DAC for PLCs Reference Design](#)

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