

# TLC555-Q1

## Functional Safety FIT Rate, FMD and Pin FMA

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### Table of Contents

1 Overview.....	2
2 Functional Safety Failure In Time (FIT) Rates.....	3
3 Failure Mode Distribution (FMD).....	4
4 Pin Failure Mode Analysis (Pin FMA).....	5
5 Revision History.....	7

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## 2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TLC555-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)
Total component FIT rate	10
Die FIT rate	3
Package FIT rate	7

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 10.5 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

Table	Category	Reference FIT Rate	Reference Virtual T <sub>J</sub>
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T<sub>J</sub> (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

### 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TLC555-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

Die Failure Modes	Failure Mode Distribution (%)
Output open (Hi-Z)	20
Output saturated high	25
Output saturated low	25
Output functional, not in specification voltage or timing	30

## 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TLC555-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

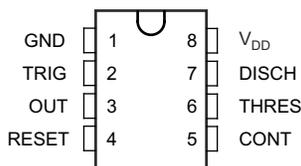
- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

**Table 4-1. TI Classification of Failure Effects**

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

[Figure 4-1](#) shows the TLC555-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TLC555-Q1 data sheet.



**Figure 4-1. Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- 'Short circuit to Power' means short to  $V_{DD}$
- 'Short circuit to GND or Ground' means short to GND

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TRIG	2	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
OUT	3	Depending on the circuit configuration, the device is likely forced into a short-circuit condition with the OUT voltage ultimately forced to the GND voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
RESET	4	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
CONT	5	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior and spiked current dissipated through the device.	B
DISCH	6	Depending on the circuit configuration, the application is not likely to function because of an inability to discharge the timing capacitors.	B
THRES	7	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
$V_{DD}$	8	Timer supplies are shorted together leaving the $V_{DD}$ pin at some voltage between the $V_{DD}$ and GND sources (depending on the source impedance).	A

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	Negative supply is left floating. The timer ceases to function because no current can source or sink to the device. There is a potential for damage if any input pins are biased.	A
TRIG	2	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
OUT	3	No negative feedback or ability for OUT to drive the application.	B
RESET	4	Leaving the RESET pin floating can effect application performance. Leaving the RESET pin open can force an output to either rail or cause irregular toggling of the output.	B
CONT	5	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
DISCH	6	Depending on the circuit configuration, the application is not likely to function because of an inability to discharge the timing capacitors.	B
THRES	7	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
V <sub>DD</sub>	8	Positive supply is left floating. The timer ceases to function because no current can source or sink to the device. There is a potential for damage if any input pins are biased.	A

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GND	1	2	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
TRIG	2	3	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
OUT	3	4	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
RESET	4	5	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
CONT	5	6	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
DISCH	6	7	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
THRES	7	8	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B
V <sub>DD</sub>	8	1	Timer supplies are shorted together, leaving the GND pin at some voltage between the GND and V <sub>DD</sub> sources (depending on the source impedance).	A

**Table 4-5. Pin FMA for Device Pins Short-Circuited to supply**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	Timer supplies are shorted together, leaving the GND pin at some voltage between the GND and V <sub>DD</sub> sources (depending on the source impedance).	A
TRIG	2	Timer supplies are shorted together, leaving the GND pin at some voltage between the GND and V <sub>DD</sub> sources (depending on the source impedance).	B
OUT	3	Depending on the circuit configuration, the device is likely forced into a short-circuit condition with the OUT voltage ultimately forced to the V <sub>DD</sub> voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
RESET	4	Depending on the circuit configuration, the application is likely not to function due to unexpected output behavior.	B
CONT	5	Depending on the circuit configuration, the application is likely not to function due to unexpected output behavior and spiked current dissipated through the device.	B
DISCH	6	Depending on the circuit configuration, the application is not likely to function because of an inability to discharge the timing capacitors. Potential for damage is high because of large currents flowing through the discharge transistor.	A
THRES	7	Depending on the circuit configuration, the application is not likely to function because of unexpected output behavior.	B

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision \* (November 2022) to Revision A (June 2023)

**Page**

• First public release.....	<b>2</b>
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