

Design Guidelines for the TLC320AD535/545

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ABSTRACT

This document provides board level design guidelines and techniques for designing with the TLC320AD535 and TLC320AD545. This includes topics such as printed-circuit board construction, power supply decoupling, reducing noise and general design guidelines and techniques. The intent is to provide guidelines that help users obtain first pass design success with the TLC320AD535 and TLC320AD545 devices.

A flow diagram explaining the initialization of the AD535 and AD545 after power-up reset is included.

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1 Introduction

The TLC320AD535 (AD535) and TLC320AD545 (AD545) devices are analog interface circuits that provide high resolution conversion from analog to digital (A/D) and digital to analog (D/A) using oversampling sigma-delta technology. They are mixed signal devices and the user should be careful to follow good mixed signal printed-circuit board design practices when designing with the AD535 and AD545. The AD535 is comprised of a two-channel codec, one for voice and one for data. The AD545 is similar to the AD535 but is a single channel device containing only the data channel.

This document will present design techniques to help achieve first pass success with the AD535 and AD545. Appendix A presents a sample flow diagram depicting the initialization scheme for the AD535 and AD545.

2 PC Board Construction

The printed-circuit board containing an AD535 or AD545 can be fabricated with as few as 4 layers. Standard FR4 type material can be used. For best performance, the layers should be configured as followed

- Top (layer 1): SIGNAL
- Internal Layer 2 : Ground
- Internal Layer 3: Power
- Bottom (layer 4): SIGNAL

The ground and power planes are sandwiched between the top and bottom signal carrying layers. This minimizes the coupling of RF noise into the system by providing a very low impedance between power and ground, and by shielding signal traces.

2.1 Ground Plane Details

The AD535 and AD545 are designed with separate analog and digital ground pins to avoid coupling digital signals into the analog circuits. See Table 1 for a description of the types of grounds each device contains.

Table 1. Types of Grounds on AD535 and AD545

PIN NAME	AD535	AD545
Data channel analog ground (DAV _{SS})	X	X
Data channel digital ground (DV _{SS})	X	X
Monitor amplifier ground (MV _{SS})	X	X
Voice channel analog ground (VAV _{SS})	X	
Internal substrate ground (V _{SS})	X	X

To obtain the best signal to noise ratio, it is recommended that the ground plane on the printed-circuit board be split into separate analog and digital sections, with the devices ground pins connected to their respective planes. The analog and digital ground planes should be joined together in only one place, preferably back at the power supply.

The analog and digital ground planes should be designed with the split occurring under the device package, between the analog and digital ground pins on the device. The splitting of the ground plane will prevent digital noise from corrupting the analog circuits within the device.

2.2 Power Plane Details

The AD535 and AD545 are designed with separate analog and digital power pins (xAV_{DD}, DV_{DD}), as well as a monitor supply pin (MV_{DD}). The monitor supply is also considered an analog power pin. Table 2 shows the possible power configurations:

Table 2. AD535 and AD545 Power Configuration

OPTION	ANALOG POWER (DAV _{DD} AND VAV _{DD})	DIGITAL POWER (DV _{DD})	MONITOR POWER (MV _{DD})
Option #1	5 V	5 V	5 V
Option #2	5 V	3.3 V	5 V
Option #3	3.3 V	3.3 V	3.3 V (see Note 1)
Option #4	3.3 V	3.3 V	5 V

NOTE 1: The power-on reset function will not operate on the AD535 with MV_{DD} connected to 3.3 V

For an ideal design, it would be recommended that separate analog and digital power be supplied to the AD535 and AD545. Because these devices can operate from a 5-V supply for the analog circuitry and a 3.3-V supply for the digital circuitry, this can be accomplished.

However, if either 5 V or 3.3 V is used to power both the analog and digital supplies on the AD535 or AD545, the use of two separate 5-V supplies rarely occurs. When a single supply is used to power both the digital and analog circuits on the AD535 and AD545, it is suggested that the power going to the analog supply pins is isolated from the digital supply as shown in Figure 1.

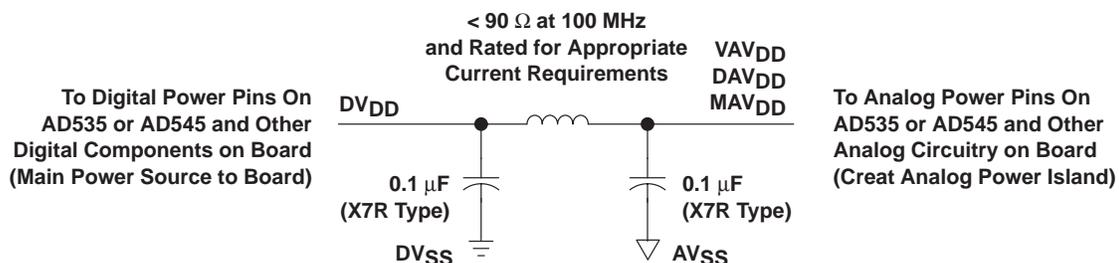


Figure 1. Isolating Analog and Digital Powers to the AD535 or AD545

A ferrite bead isolates and filters the power supplied to the analog supply pin. Two high frequency bypass capacitors are also used, one on either side of the ferrite bead. Basically a separate analog power island is created for the AD535 or AD545.

The connection from the ferrite bead to the HF decoupling cap and analog power pins on the AD535 and AD545 should be done as an *island* or small isolated plane. If this is not possible, very wide traces as wide as the pad on the surface-mount discrete components (or wider) should be used.

3 Special Connections

Several pins on the AD535 and AD545 should be either decoupled to a specific power or ground, or attached directly to those planes. The following section details these special connections

3.1 Analog Power and/or Ground Planes

The connections described in Table 3 must be connected directly to the analog power and/or ground planes:

Table 3. Connections to the Analog Power and/or Analog Ground Planes

PIN OR COMPONENT NAME	DESCRIPTION	DEVICE	CONNECTION
DAV _{SS}	Analog ground pin for the data channel	AD535 AD545	Connected directly to the analog ground plane
VAV _{SS}	Analog ground pin for the voice channel	AD535	Connected directly to the analog ground plane
V _{SS}	Internal substrate ground	AD535 AD545	Connected directly to the analog ground plane
MV _{SS}	Monitor amplifier ground pin	AD535 AD545	Connected directly to the analog ground plane
DAV _{DD}	Data channel analog power supply pin	AD535 AD545	Connected directly to the analog power plane or island
VAV _{DD}	Voice channel analog power supply	AD535	Connected directly to the analog power plane or island
HF bypass capacitor #1 (0.1 μ F)	HF decoupling of the data channel analog power supply	AD535 AD545	Connected between the analog power and analog ground planes, located at the DAV _{DD} pin on the device
HF bypass capacitor #2 (0.1 μ F, X7R type ceramic)	HF decoupling of the voice channel analog power supply	AD535	Connected between the analog power and analog ground planes, located at the VAV _{DD} pin on the AD535
HF bypass capacitor #3 (0.1 μ F, X7R type ceramic)	HF decoupling of the monitor power supply	AD535 AD545	Connected between the analog power and analog ground planes, located at the MV _{DD} pin on the device
HF bypass capacitor #4 (0.1 μ F, X7R type ceramic)	HF decoupling of the bandgap reference	AD535 AD545	Connected between the FILT pin and analog ground planes, located at the FILT pin on the device
LF bypass capacitor #1 (optional 22–47 μ F, electrolytic)	Optional low frequency decoupling of the data channel analog power	AD535 AD545	Connected between the analog power and analog ground planes, located at the DAV _{DD} pin on the device
LF bypass capacitor #2 (optional 22–47 μ F, electrolytic)	Optional low frequency decoupling of the voice channel analog power	AD535 AD545	Connected between the analog power and analog ground planes, located at the VAV _{DD} pin on the device
LF bypass capacitor #3 (optional 22–47 μ F, electrolytic)	Optional low frequency decoupling of the monitor power supply	AD535 AD545	Connected between the analog power and analog ground planes, located at the MV _{DD} pin on the device

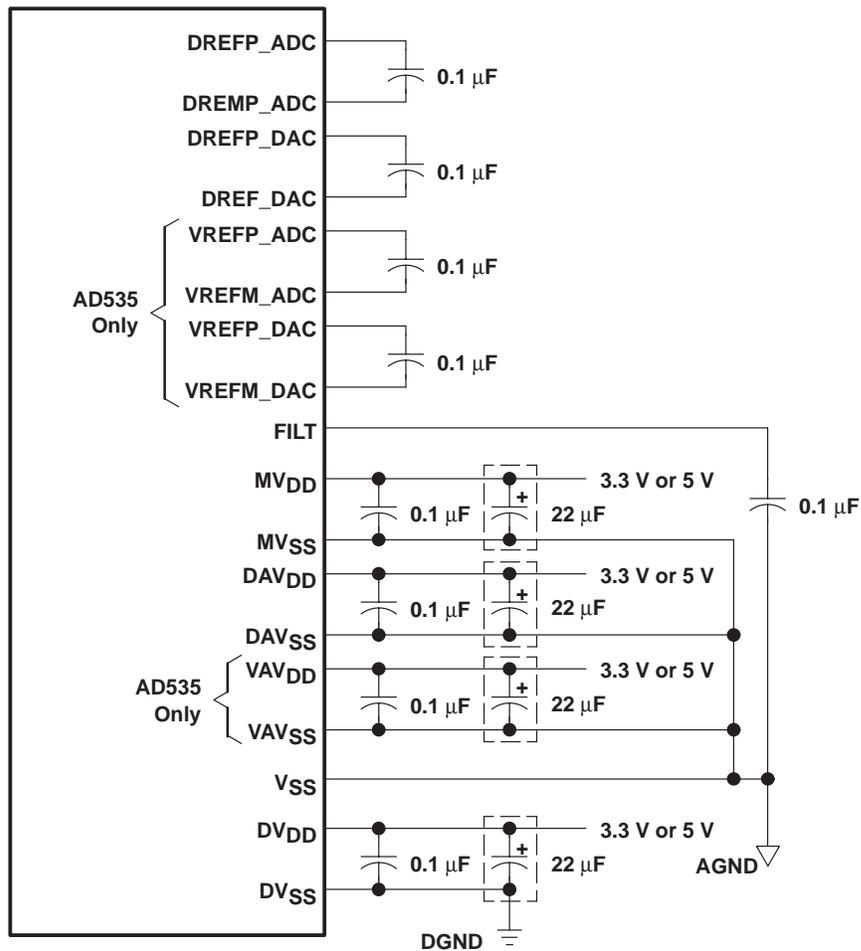
3.2 Digital Power and/or Ground Planes

The connections described in Table 4 must be connected directly to the digital power and/or ground planes. These connections are common to both the AD535 and AD545.

Table 4. Connections to the Digital Power and/or Digital Ground Planes

PIN OR COMPONENT NAME	DESCRIPTION	CONNECTION
DVSS	Digital ground pin	Connected directly to the digital ground plane
DVDD	Digital power supply pin	Connected directly to the digital power plane
HF bypass capacitor #5 (0.1 μ F, X7R type ceramic)	HF decoupling of the digital power supply	Connected between the digital power and digital ground planes, located at the DVDD pin on the device
LF bypass capacitor #4 (optional 22–47 μ F, electrolytic)	Optional low frequency decoupling of the digital power supply	Connected between the digital power and digital ground planes, located at the DVDD pin on the device

Refer to Figure 2 for a schematic showing required decoupling capacitors.



NOTE: Components in dashed boxes are optional, but suggested

Figure 2. Decoupling Requirements for the AD535 and AD545

3.3 Bandgap Voltage Reference Filter Decoupling

The internal bandgap voltage references for both the data channel DAC and ADC, as well as the voice channel DAC and ADC (AD535 only), are brought out to pins on the AD535 and AD545. External filtering of this bandgap reference voltage is required. A 0.1 μF ceramic capacitor must be used to decouple these references. A surface-mount component should be used. See Table 5 for the pins to be decoupled.

Table 5. Bandgap Filter Decoupling

PIN NAME	CAPACITOR VALUE	DEVICE	DESCRIPTION
DREFM_ADC, DREFP_ADC	0.1 μF (X7R type ceramic)	AD545 AD535	Data channel ADC voltage reference filter decoupling. Capacitor should be located at the DREFP_ADC pin.
DREFM_DAC, DREFP_DAC	0.1 μF (X7R type ceramic)	AD545 AD535	Data channel DAC voltage reference filter decoupling. Capacitor should be located at the DREFP_DAC pin.
VREFM_ADC, VREFP_ADC	0.1 μF (X7R type ceramic)	AD535	Voice channel ADC voltage reference filter decoupling. Capacitor should be located at the VREFP_ADC pin.
VREFM_DAC, VREFP_DAC	0.1 μF (X7R type ceramic)	AD535	Voice channel DAC voltage reference filter decoupling. Capacitor should be located at the VREFP_DAC pin.

3.4 Bandgap Filter Reference Decoupling

External decoupling of the power supply to the bandgap reference is required. The FILT pin is provided as this point in the circuit. A 0.1 μF ceramic capacitor must be located at the FILT pin and connected between FILT and analog ground (AV_{SS})

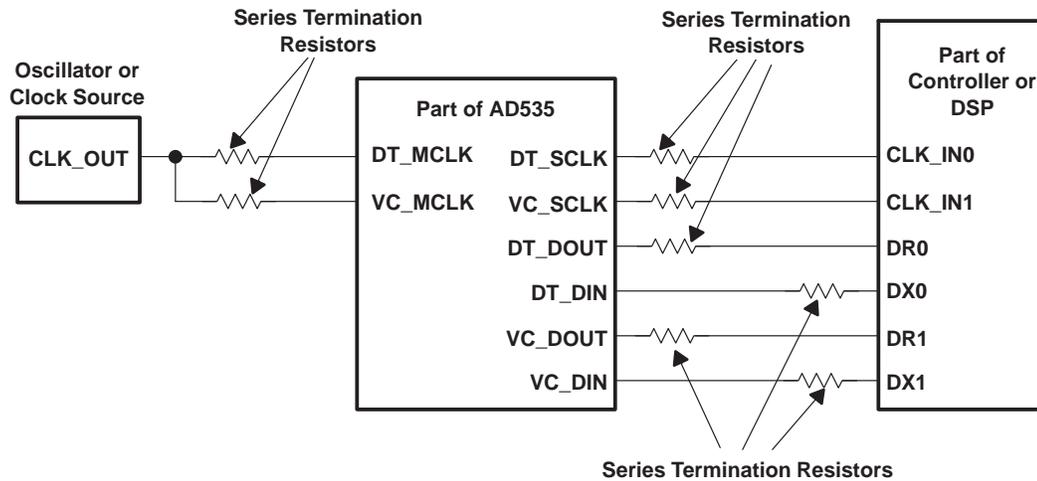
4 Clocks

Termination of high frequency digital signals, such as clock signals, depends on the frequency of the clocks being used, the length of the signal traces, and the rise and fall times of these clock signals.

In many cases, it is useful to place series termination resistors at the clock source pin. It is easier to place a shunt or zero ohm resistor across the pads if the termination is not required, than to spin a board just to add a series resistor. In a board design using the AD535 or AD545, it may be useful to place a series termination resistor at the following clock source points:

- At the oscillator or clock source for DT_MCLK
- At the oscillator or clock source for VC_MCLK (AD535 only)
- At the DT_SCLK pin
- At the VC_SCLK pin (AD535 only)

See Figure 3 for the optimum location of the series resistors. The value for these series resistors is driver, board, and transmission line dependent. Usually a value of 22 Ω to 68 Ω will be sufficient. The intention here is to reduce noise, undershoot, and overshoot on the signals. The designer must be very careful in the choice of values for the series resistor, so that the rise or fall time of the clocks is not adversely degraded. If this degradation occurs, double clocking of data is possible due to a slow rise time crossing the trigger threshold too slowly on the interconnected device.



NOTE: Separate oscillators or clock sources can be used for VC_MCLK and DT_MCLK

Figure 3. Termination of Clocks and Data (AD535 example)

It may also be useful to place series termination resistors at the source of the serial data stream, or a pull-down resistor on the signal driving the DIN pin on the AD535 or AD545. The series resistors are also shown in Figure 3.

5 General

Proper printed-circuit board design and layout is important in producing a low noise, high quality design. In addition to the techniques and tips suggested above, a few other items can help in producing a low noise system:

- Keep analog and digital signal traces physically separated from each other.
- Do not run analog and digital signals side by side.
- Run high-speed clock lines entirely on the top or bottom signal layers and avoid using vias on these lines.
- Keep clock trace paths as short as possible.
- Take care in routing clock signals so they are away from analog signals and circuitry, as well as any analog voltage references.
- Try to always use solid ground planes – do not use routed ground traces.
- Route analog signals and power plane over the analog ground plane (not the digital ground)
- Route digital signals and power plane over the digital ground plane (not the analog ground)
- Use surface-mount discrete components to minimize parasitic capacitance and inductance.
- Locate power supply decoupling capacitors at power supply pins on devices. Place ceramic capacitors (HF caps) closest to the IC pins when both HF and LF bulk caps are used.
- Locate switching power supplies away from analog circuits

- Power supply inputs to the PC board must be adequately filtered at the power supply input to the board. Both high and low frequency decoupling should be used.

5.1 Preventing Latch-Up

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic transistor that is present due to the inherent nature of CMOS. When a latch-up condition occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current is not limited.

Even though the AD535 and AD545 are heavily protected against latch-up, it is still possible to cause a latch-up condition under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the supply voltage drops momentarily below ground or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected.

To ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode with a forward voltage drop of less than or equal to 0.4V (1N5711 or equivalent) between the power supply and its ground.

5.2 Device Power-Up Sequence

Latch-up can also occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence be used:

- Ensure that no signals are applied to the device before the power-up sequence is complete.
- Connect GND.
- Apply power (analog powers then digital powers).
- Hold the device in reset.
- Connect the master clock.
- Release the device reset.
- Apply the analog signals.

When powering down the device, this procedure should be followed in reverse order.

5.3 Applying RESET to the AD535/AD545

The AD535 and AD545 require the signal applied to the RESET pin to remain active (low) for a minimum of 10 VC_MCLK and DT_MCLK cycles before asserting it inactive (high). The reset pulse does not have to be synchronous with either channel's MCLK signal, but it must encompass at least 10 of the channel's MCLK cycles in order for the channel and device to be properly reset.

5.4 Power-On Reset Function (AD535 only)

The power-on reset function ($\overline{\text{POR}}$ pin) is provided for resetting devices external to the AD535. The power-on reset function does not reset the AD535. It provides a means to reset other devices on the board, once the MV_{DD} power supply has crossed a defined threshold and become stable.

5.5 Interfacing the Data Channel to a Telephone Line

The hybrid circuitry in the data channel includes integrated amplifiers whose gains and filter pole frequencies are set by external resistors and capacitors. This allows maximum flexibility to make adjustments for board variations and international standards while providing integration of the function. A voltage reference (DT_REF) is provided as a reference for the transformer for the interconnection to the phone line.

Figure 4 gives an example of how to connect the data channel interface to the phone line with component values for the discrete matching network. A single ended configuration is shown. Figure 5 gives an example with a differential configuration.

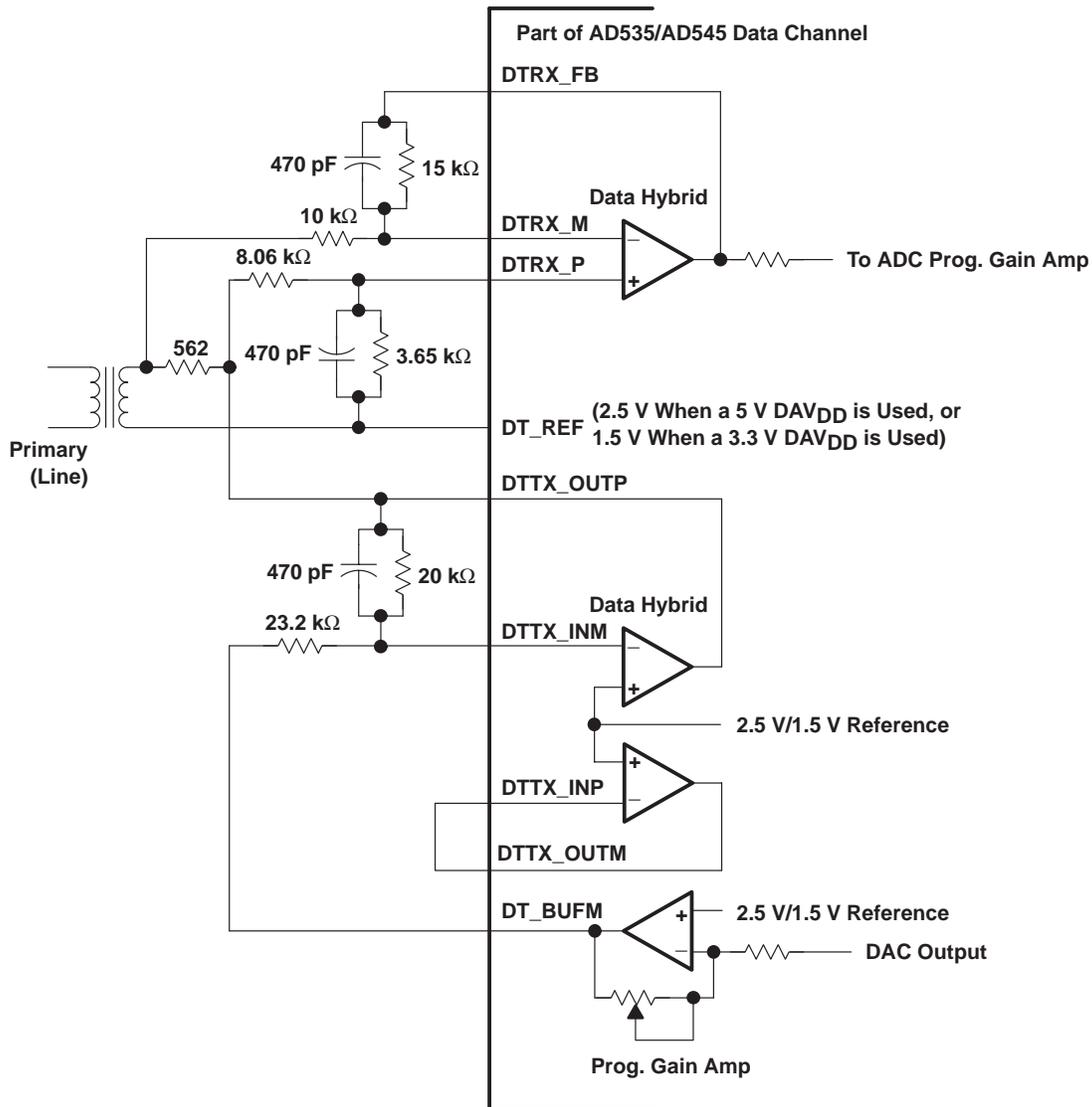


Figure 4. AD535/AD545 Data Channel Connection to Phone Line (Single-Ended Configuration)

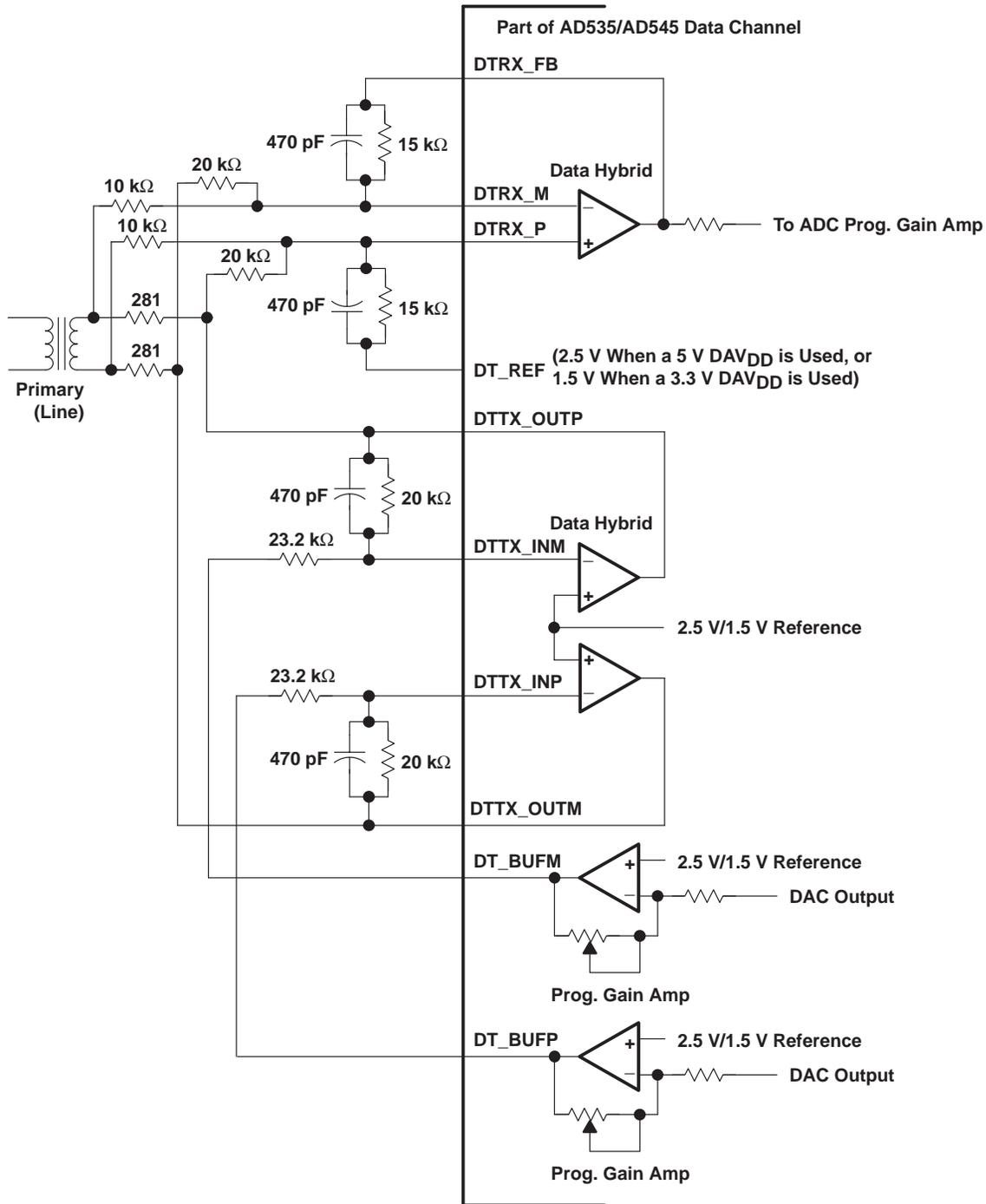
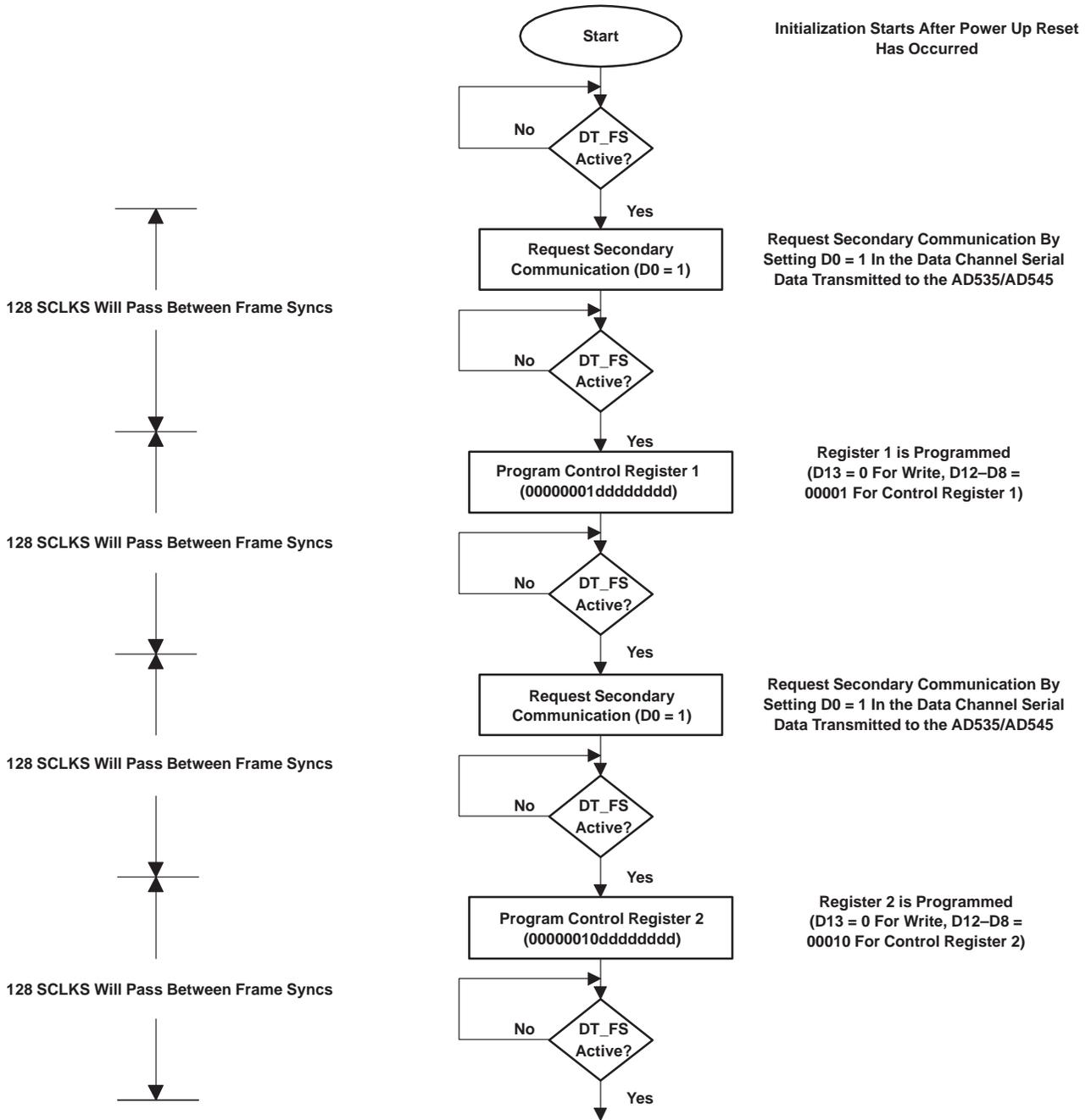


Figure 5. AD535/AD545 Data Channel Connection to Phone Line (Differential Configuration)

6 References

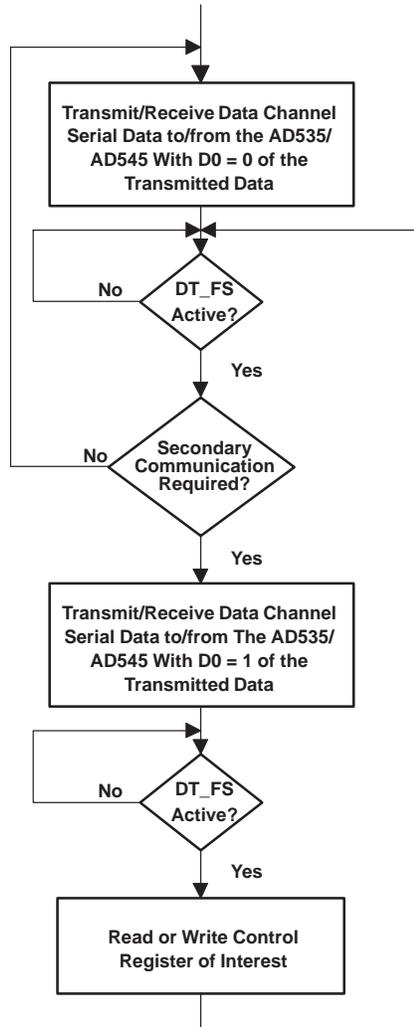
1. TLC320AD535C/I Data Manual, Dual Channel Voice/Data Codec (SLAS202)
2. TLC320AD545C/I Data Manual, Single Channel Data/Fax Codec (SLAS206)

Appendix A Flow Chart for Initializing a TLC320AD535 or AD545 (Data Channel Only)

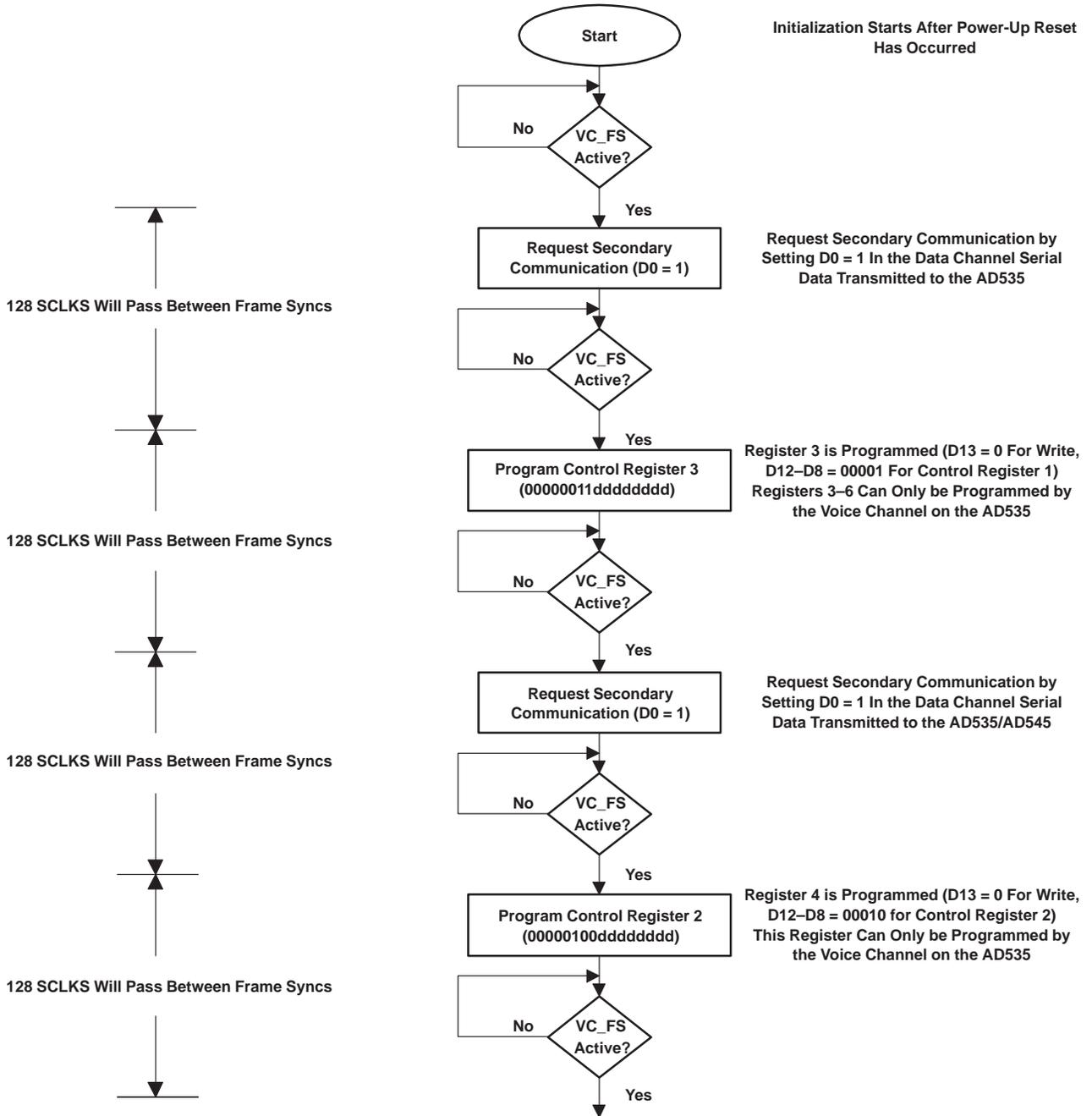


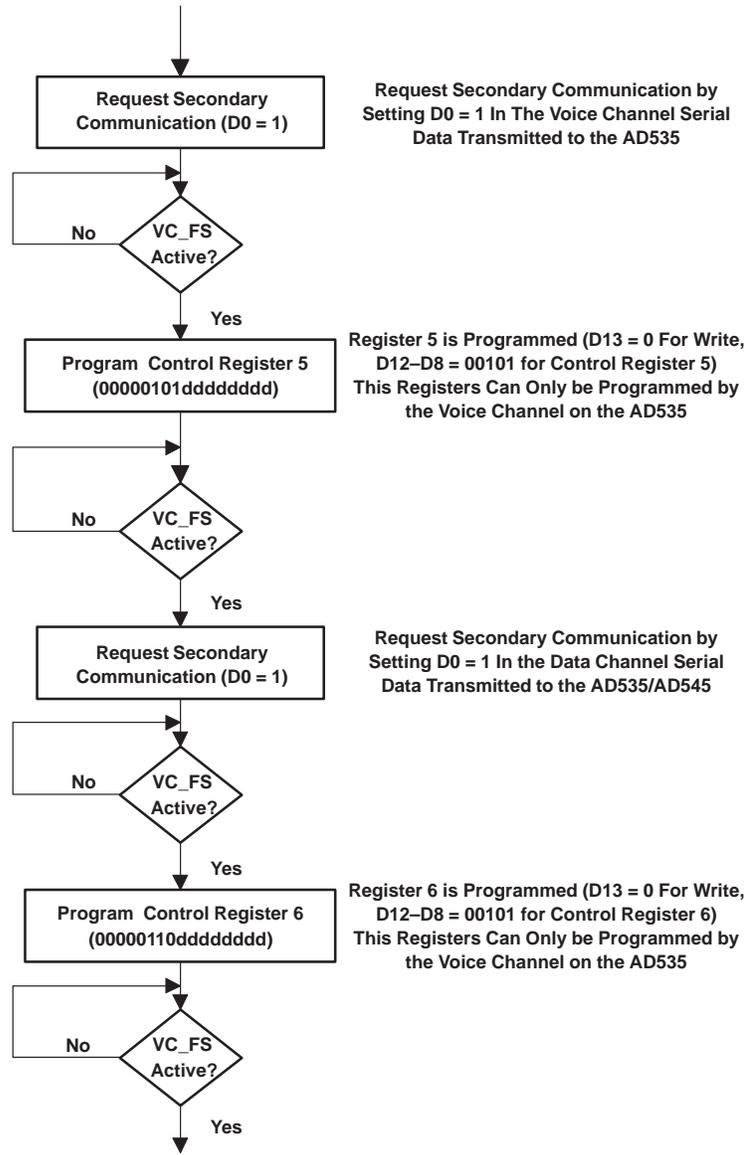
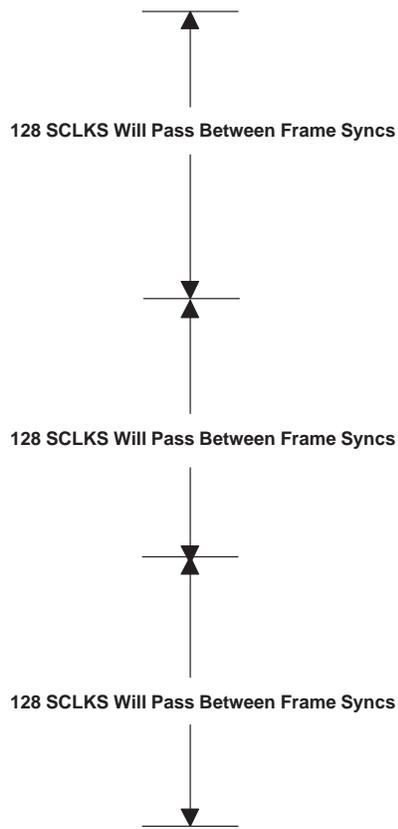
↑
256 SCLKS Will Pass Between Frame Syncs
When Only Primary Communications Are
Occurring

↓
128 SCLKS Will Pass Between Frame Syncs
For Primary Communications Followed By
Secondary Communications



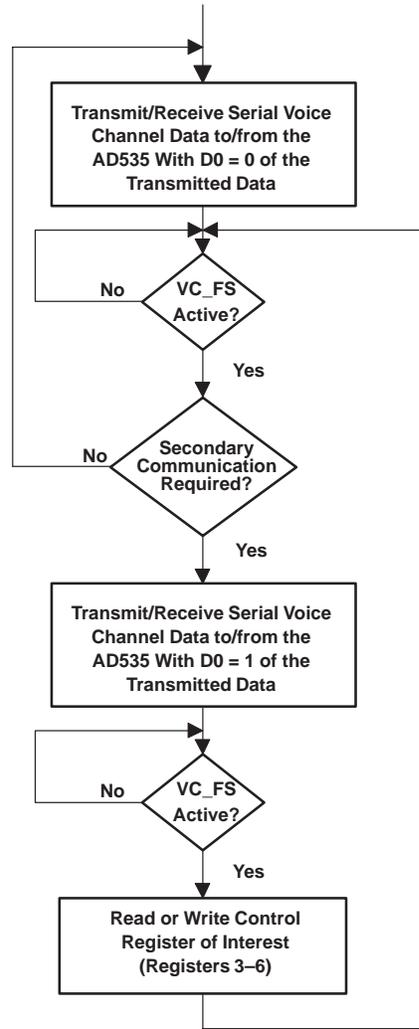
Appendix B Flow Chart for Initializing a TLC320AD535 (Voice Channel)





256 SCLKS Will Pass Between Frame Syncs
When Only Primary Communications Are
Occurring

128 SCLKS Will Pass Between Frame Syncs
For Primary Communications Followed By
Secondary Communications



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