

TPS720xxDRVEVM Evaluation Module

This user's guide describes the characteristics, operation, and use of the TPS720xxDRVEVM evaluation module (EVM). This EVM demonstrates the Texas Instruments TPS720xx, an ultralow input voltage low-drop out (LDO) linear regulator in a 2-mm x 2-mm SON-6 package that is capable of 350 mA of output current. This user's guide includes setup instructions, a schematic diagram, thermal guidelines, a bill of materials, and printed-circuit board layout drawings for the EVM.

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1 Introduction

The TPS720xxDRVEVM evaluation module helps designers evaluate the operation and performance of the TPS720xx LDO in the SON-6 package. The TPS720xx is a 350-mA, ultralow input voltage linear regulator with a bias pin.

1.1 Related Documentation from Texas Instruments

TPS720xx, 350mA, Ultra-Low V_{IN} , RF Low-Dropout Linear Regulator With Bias Pin data sheet ([SBVS100](#))

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS720xxDRVEVM.

2.1 Input / Output Connector Descriptions

2.1.1 J1 – VIN

This is the positive input supply voltage. Twist the leads to the input supply and keep them as short as possible to minimize EMI transmission. If the supply leads are greater than six inches, add more bulk capacitance between J1 and J3. An additional 47- μ F or greater capacitor improves the transient response of the TPS720xx and helps to reduce ringing on the input when long supply wires are used. The maximum input voltage is the smaller of 4.5 V or the value of voltage on pin 1 of J5 (Vbias).

2.1.2 J2 – VOUT

This is the positive connection from the output. Connect this pin to the positive input of the load.

2.1.3 J3 – GND

This is the return connection for the input power supply of the regulator.

2.1.4 J4 – GND

This is the return connection for the output.

2.1.5 J5 – Bias Supply

This connector is used to provide a bias voltage supply to the TPS720xx. Pin 1 is the positive voltage of the bias supply, and pin 2 of J5 is the ground connection of the bias supply. If an external bias supply is used, its voltage must be between 2.5 V and 5.5 V.

2.1.6 JP1 – ENABLE

This 3-pin jumper is used to enable or disable the converter. Placing a jumper between pins 1 and 2 of JP1 enables the converter to be on. Moving the jumper between pin 2 and 3 disables the converter to be off. Terminate the enable pin using a jumper or external signal generator, and leave it floating.

2.1.7 JP1 – Jumper

This 2-pin jumper is used to tie VBIAS to VIN for situations where a bias voltage supply is not used. Installing a jumper across the two pins shorts VBIAS to VIN. Remove the jumper isolated VBIAS from VIN so that an external bias voltage can be used.

3 Operation

This section provides information about the operation of the TPS720xxEVM.

3.1 Operation

Connect the positive input power supply to J1. Connect the input power return (ground) to J3. Connect the positive VBIAS voltage to pin 1 of J5 and the VBIAS return (GND) to pin 2 of J5. Connect the load across J2 (positive output voltage) and J4 (GND). Configure jumpers JP1 and JP2 for the desired operation based on the functions described in and .

The recommended maximum operating input voltage is the lower of 4.5 V or the voltage on VBIAS. The actual highest input voltage may be less due to thermal conditions. To determine the highest input voltage, see .

4 Thermal Guidelines

This section provides guidelines for the thermal management of the TPS720xxDRVEVM board.

4.1 Thermal Considerations

Thermal management is a key component of design of any power converter and is especially important when the power dissipation in the LDO is high. To help you design the TPS720xx family into your application, use the following formula to approximate the maximum power dissipation at a particular ambient temperature:

$$T_J = T_A + P_d \times \theta_{JA} \quad (1)$$

where T_J is the junction temperature, T_A is the ambient temperature, P_d is the power dissipation in the IC, and θ_{JA} is the thermal resistance from junction to ambient. All temperatures are in degrees Celsius.

The measured thermal resistance from junction to ambient for the TPS720xxEVM board has a typical value of 48.35°C/W. The recommended maximum operating junction temperature specified in the data sheet for the TPS720xx family is 125°C. With this information, the maximum power dissipation can be found by using [Equation 1](#).

Example Calculation:

For example, what is the maximum input voltage that can be applied to a TPS720105 with the output voltage of 1.05 V, if the ambient temperature is 85°C and the full 350 mA of load current is required?

Given: $T_J = 125^\circ\text{C}$, $T_A = 85^\circ\text{C}$, $\theta_{JA} = 48.35^\circ\text{C/W}$

Using [Equation 2](#), substitute in the preceding given values and find that the maximum power dissipation for the part is $P_d = 0.827 \text{ W}$.

$$125^\circ\text{C} = 85^\circ\text{C} + P_d (48.35^\circ\text{C/W}) \quad (2)$$

This means that the total power dissipation of the TPS720105 must be less than 0.827 W. The input voltage now can be calculated.

$$P_d = (V_{in} - V_{out}) \times I_{out} = (V_{in} - 1.05\text{V}) \times 0.350 \text{ A} = 0.827 \text{ W} \quad (3)$$

So, the maximum input voltage needs to be 3.412 V or less in order to maintain a safe junction temperature.

5 Board Layout

This section provides the TPS720xxDRVEVM board layout and illustrations.

5.1 Layout

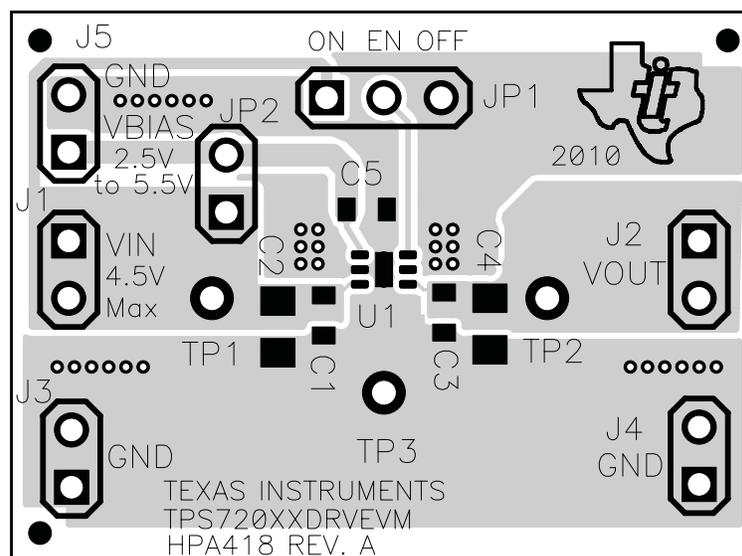


Figure 1. Assembly Layer

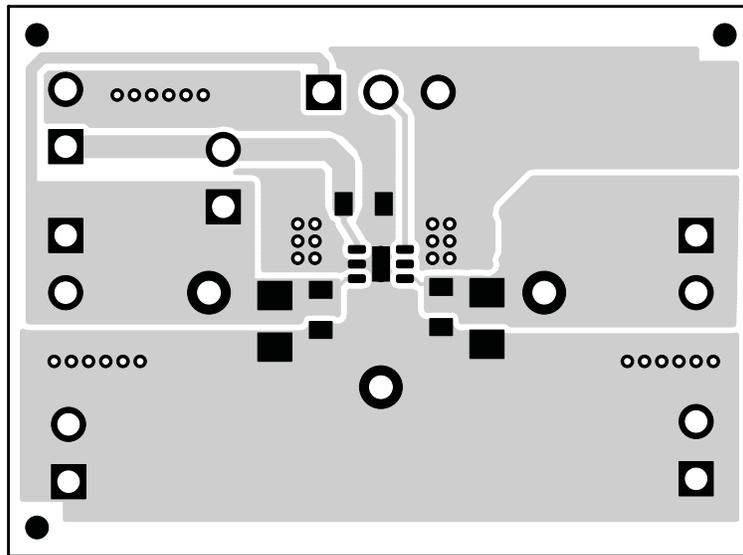


Figure 2. Top Layer Routing

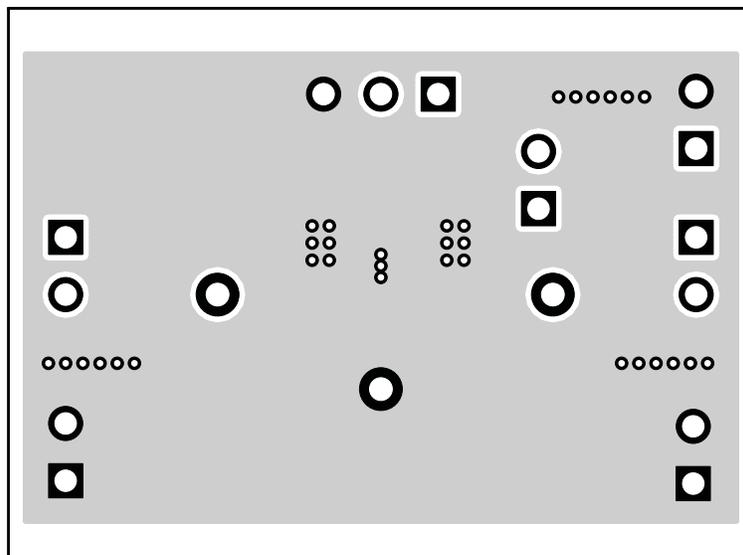


Figure 3. Bottom Layer Routing

6 Schematic and Bill of Materials

This section provides the TPS720xxDRVEVM schematic and bill of materials.

6.1 Schematic

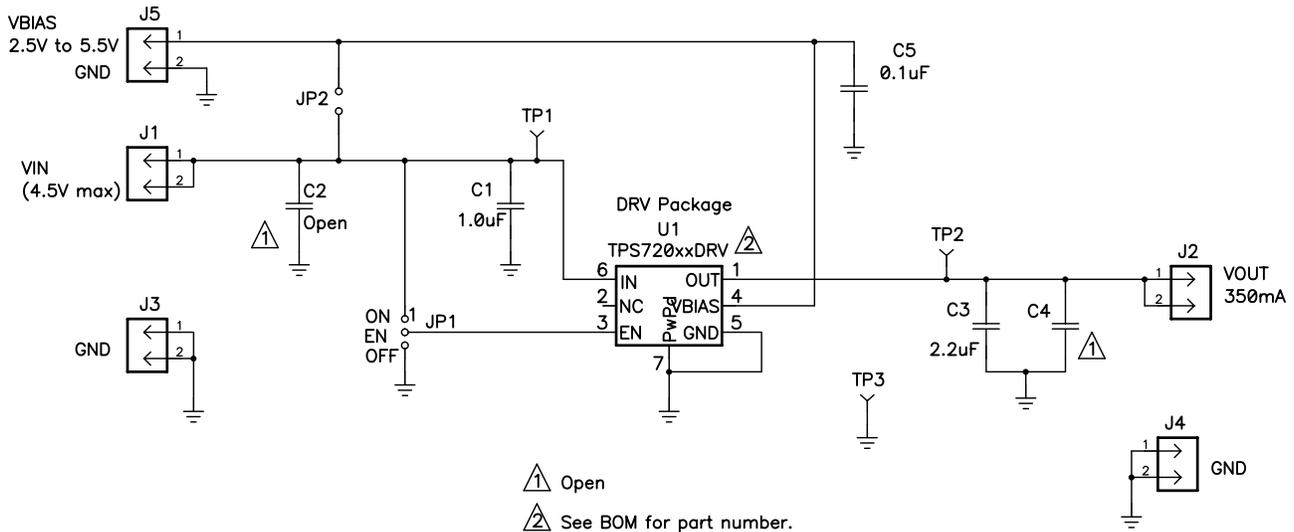


Figure 4. TPS720xxDRVEVM Schematic

6.2 Bill of Materials

Table 1. TPS720xxDRVEVM Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	1.0 µF	Capacitor, Ceramic, 10V, X5R, 20%	0603	Std	Std
0	C2	Open	Capacitor, Ceramic, 10V, X5R, 20%	0805	Std	Std
1	C3	2.2 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	Std	Std
0	C4	Open	Capacitor, Ceramic, 6.3V, X5R, 10%	0805	Std	Std
1	C5	0.1 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	Std	Std
5	J1–J5	PEC02SAAN	Header, 2-pin, 100 mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	JP1	PEC03SAAN	Header, 3-pin, 100 mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
1	JP2	PEC02SAAN	Header, 2-pin, 100 mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
3	TP1–TP3	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
1	U1	TPS720105DRV	IC, LDO Linear Regulator With Bias Pin, 350mA	SON-6	TPS720105DRV	TI
2	N/A		Shunt, Open-top		151-8000	Kobiconn
1	PCB		PCB, 1.300 In x 0.960 In x .062 In		HPA418	Any

- Notes:
1. These assemblies are ESD sensitive, ESD precautions shall be observed.
 2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
 3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
 4. Ref designators marked with an asterisk (***) cannot be substituted. All other components can be substituted with equivalent MFG's components.

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 1.1 V to 4.5 V and the output voltage range of 0.9 V to 3.6 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85° C. The EVM is designed to operate properly with certain components above 85° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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