Using the TPS40322EVM-679

User's Guide

Literature Number: SLUU506
June 2011

Dual Output Synchronous Buck Converter

1 Introduction

The TPS40322EVM-679 evaluation module (EVM) is a dual output synchronous buck converter. The EVM delivers 1.2 V at 10 A and 1.8 V at 10 A from a 12-V nominal DC input voltage. The module uses the TPS40322 Dual Output or Two-Phase Synchronous Buck Controller and the CSD86330Q3D Synchronous Buck NexFET™ Power Block in a 500-kHz application.

2 Description

TPS40322EVM-679 is designed to use a regulated 8.0-V_{DC} to 15.0-V_{DC} bus to produce two high-current, regulated outputs. Both outputs are capable of supplying up to 10 A of load current. The TPS40322EVM-679 is designed to demonstrate the TPS40322 in a typical regulated bus to dual-output, low-voltage application while providing a number of test points to evaluate the performance of the TPS40322 in a given application.

2.1 Typical Applications

- Multiple Rail Systems
- Telecom Base Stations
- Switcher/Router Networking
- xDSL Broadband Access
- Server and Storage Systems

2.2 Features

- 8-V to 15-V Input Range
- 1.2-V and 1.8-V Fixed Outputs
- 10-A_{DC} Steady-State Current Per Output
- 500-kHz Switching Frequency
- Output Sequence Capability
- Inductor DCR Current Sensing
- Voltage Mode Feedback Control With Input Feed Forward

3 Electrical Performance Specifications

Table 1. TPS40322EVM-679 Electrical Performance Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics						
VIN	Voltage range		8.0	12.0	15.0	V
	Maximum input current	VIN = $VIN_{(min)}$, I_{OUT1} = I_{OUT2} = 10 A		4.5		A
	No-load input current			55		mA
Output 1 Characteristics						
VOUT1	Output voltage	$I_{OUT1(min)} \le I_{OUT1} \le I_{OUT1(max)}$		1.2		V
I_{OUT1}	Output load current	$VOUT1_{(min)} \le VOUT1 \le VOUT1_{(max)}$	0		10	A
	Output voltage regulation	Line Regulation: $VOUT1_{(min)} \le VOUT1 \le VOUT1_{(max)}$			0.5%	
		Load Regulation: $I_{OUT1(min)} \le I_{OUT1} \le I_{OUT1(max)}$			0.5%	
	Output voltage ripple	$I_{OUT1} = I_{OUT1(max)}$			24	mV_{PP}
	Output over current	$VOUT1_{(min)} \le VOUT1 \le VOUT1_{(max)}$		14.6		A
Output 2 Characteristics						
VOUT2	Output voltage	$I_{OUT2(min)} \le I_{OUT2} \le I_{OUT2(max)}$		1.8		V
I_{OUT2}	Output load current	$VOUT2_{(min)} \le VOUT2 \le VOUT2_{(max)}$	0		10	A
	Output voltage regulation	Line Regulation: $VOUT2_{(min)} \le VOUT2 \le VOUT2_{(max)}$			0.5%	
		Load Regulation: $I_{OUT2(min)} \le I_{OUT2} \le I_{OUT2(max)}$			0.5%	
	Output voltage ripple	$I_{OUT2} = I_{OUT2(max)}$			36	mV_{PP}
	Output over current	$VOUT2_{(min)} \le VOUT2 \le VOUT2_{(max)}$		14.6		A
Systems Characteristics						
	Switching frequency			500		kHz
	Peak efficiency	VOUT1 = 1.2 V, 3.5 A ≤ I_{OUT1} ≤ 5.5 A, VIN = 8 V		89%		
		VOUT2 = 1.8 V, 2.5 A ≤ I_{OUT2} ≤ 6.5 A, VIN = 8 V		90%		
	Full load efficiency	VOUT1 = 1.2 V, $I_{OUT1} = I_{OUT1(max)}$, VIN = 12 V		86%		
		VOUT2 = 1.8 V, $I_{OUT2} = I_{OUT2(max)}$, VIN = 12 V		87%		
	Operating temperature			25		ºC

4 Schematic

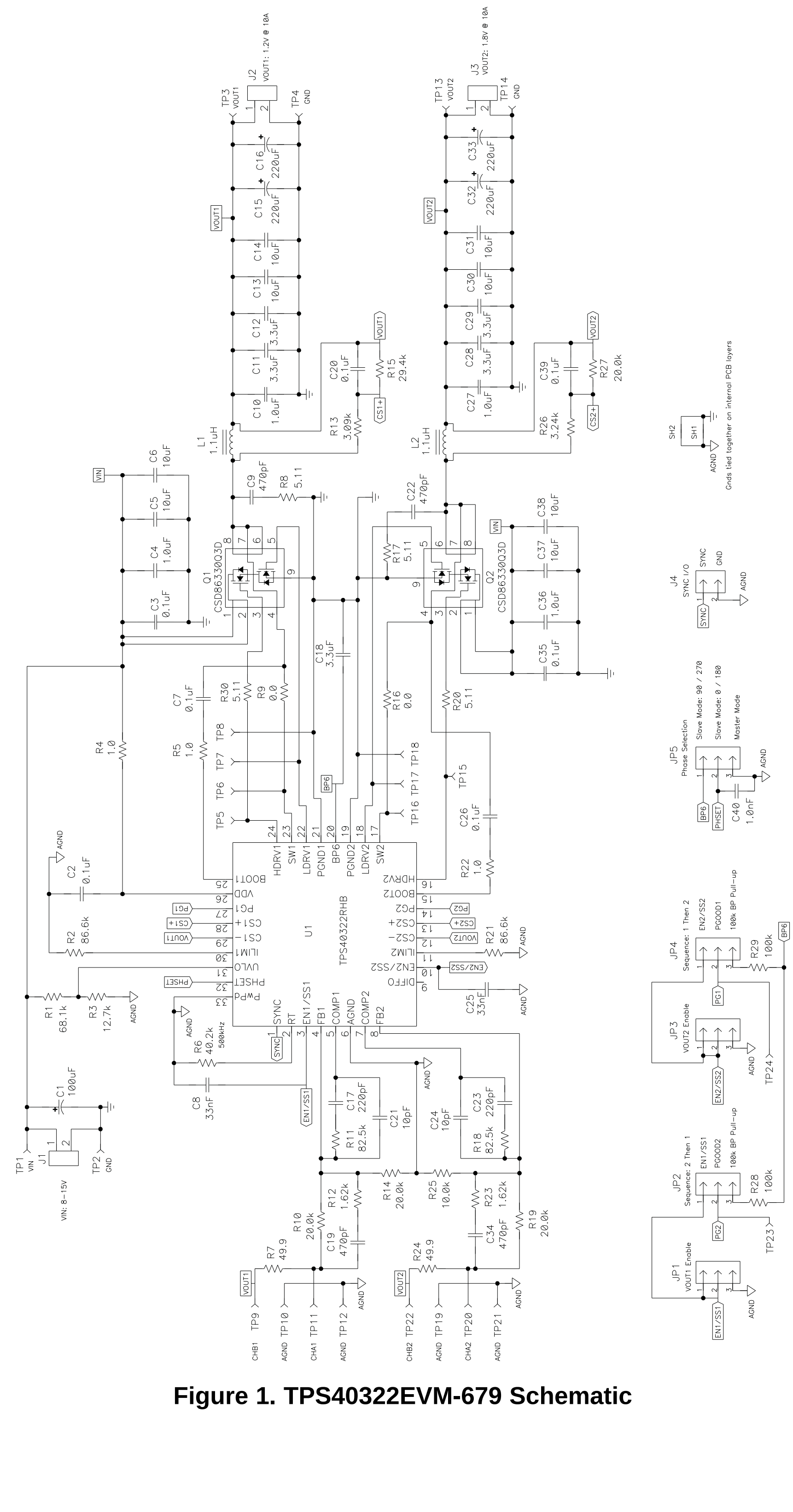

Figure 1. TPS40322EVM-679 Schematic

5 Test Setup

5.1 Test Equipment

Voltage Source: Input DC source, the input voltage source (VIN) shall be a 0-V to 15-V variable DC source capable of 10 A_{DC}. Connect VIN to J1 as shown in Figure 2.

Multimeters: Five Multimeters

1. Volt meter, V1, 0 V_{DC} to 5 V_{DC}.
2. Volt meter, V2, 0 V_{DC} to 5 V_{DC}.
3. Volt meter, V3, 0 V_{DC} to 15 V_{DC}.
4. Current meter, A1, 0 A_{DC} to 10 A_{DC}. (Optional: to improve current measurement use a 0-mV to 100-mV voltmeter and a 1-mV/A shunt)
5. Current meter, A2, 0 A_{DC} to 10 A_{DC}. (Optional: to improve current measurement use a 0-mV to 100-mV voltmeter and a 1-mV/A shunt)

Output Load: Loads, LOAD1 shall be an Electronic Constant Current Mode Load capable of 0 A_{DC} to 10 A_{DC} at 1.2 V. LOAD2 shall be an Electronic Constant Current Mode Load capable of 0 A_{DC} to 10 A_{DC} at 1.8 V.

Oscilloscope: A digital or analog oscilloscope can be used to measure the ripple voltage on VOUT. The oscilloscope should be set for 20-MHz bandwidth, AC coupled. Test points TP3 and TP4 can be used to measure VOUT1 and test points TP13 and TP14 can be used to measure VOUT2. Use the tip and barrel method shown in Figure 3 to avoid inducing additional noise due to the large ground loop area that would result from using the probe's ground lead.

Recommended Wire Gauge:

- **VIN to J1:** The connection from VIN to the J1 connector of the EVM can carry as much as 5 A_{DC}. The wire gauge shall be 18 AWG minimum and no longer than two feet for each connection, VIN+ to J1+, and VIN- to J1-.
- **J2 to LOAD1:** The connection from J2 of the EVM to LOAD1 can carry as much as 10 A_{DC}. The wire gauge shall be 14 AWG minimum and no longer than two feet for each connection, J2+ to LOAD1+, and LOAD1- to J2-.
- **J3 to LOAD2:** The connection from J3 of the EVM to LOAD2 can carry as much as 10 A_{DC}. The wire gauge shall be 14 AWG minimum and no longer than two feet for each connection, J3+ to LOAD2+, and LOAD2- to J3-.

5.2 Recommended Test Setup

Shown in Figure 2 is the basic test set up recommended to evaluate the TPS40322EVM-679.

Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.

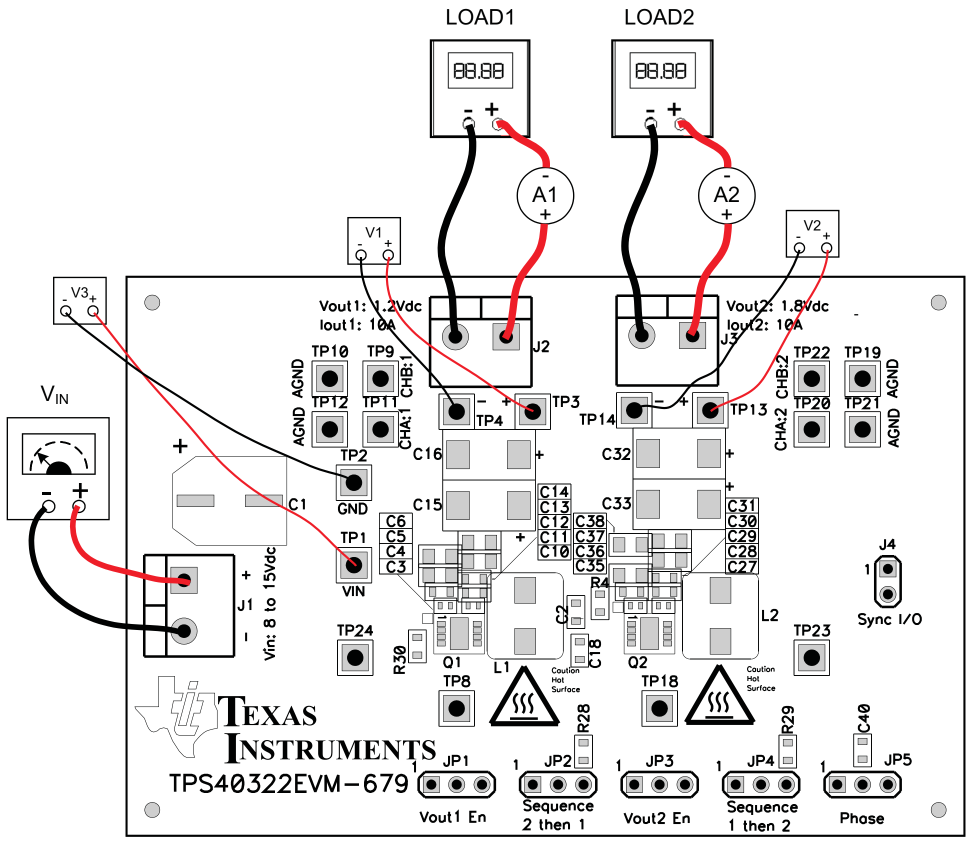

Figure 2. TPS40322EVM-679 Recommended Test Set Up

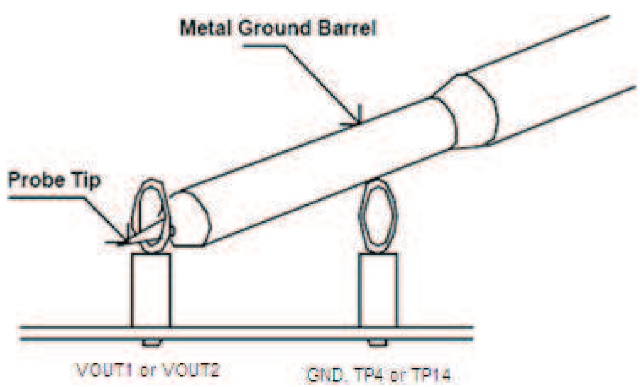

Figure 3. Tip and Barrel Voltage Ripple Measurement

5.3 List of Test Points

Table 2. Test Point Functional Descriptions

TEST POINT	NAME	DESCRIPTION
TP1	VIN	Input voltage positive sense point, reference to TP2
TP2	GND	Input voltage negative sense point
TP3	VOUT1	Output 1 positive sense point, reference to TP4
TP4	GND	Ground reference for TP3
TP5	HDRV1	Output 1 high drive test pad, reference to TP8
TP6	SW1	Output 1 switch node test pad, reference to TP8
TP7	LDRV1	Output 1 low drive test pad, reference to TP8
TP8	PGND1	Power ground for output 1
TP9	CHB1	Output 1 loop injection point, reference to TP10
TP10	AGND	Ground reference for TP9
TP11	CHA1	Output 1 loop injection point, reference to TP12
TP12	AGND	Ground reference for TP11
TP13	VOUT2	Output 2 positive sense point, reference to TP14
TP14	GND	Ground reference for TP13
TP15	HDRV2	Output 2 high drive test pad, reference to TP18
TP16	SW2	Output 2 switch node test pad, reference to TP18
TP17	LDRV2	Output 2 low drive test pad, reference to TP18
TP18	PGND2	Power ground for output 2
TP19	AGND	Ground reference for TP22
TP20	CHA2	Output 2 loop injection point, reference to TP21
TP21	AGND	Ground reference for TP20
TP22	CHB2	Output 2 loop injection point, reference to TP19
TP23	PG2	Output 2 power good indicator
TP24	PG1	Output 1 power good indicator

6 Test Procedure

6.1 Load Regulation Measurement Procedure

1. Ensure LOAD1 and LOAD2 are set to constant-current mode and to set to sink 0 A.
2. Increase VIN from 0 V to 12 V_{DC}. VOUT1 and VOUT2 should be in regulation once VIN is 7.8 V or greater.
3. Set LOAD2 to 10 A.
4. Vary LOAD1 from 0 A to 10 A. VOUT1 and VOUT2 should remain within regulation per Table 1.
5. Set LOAD1 to 10 A.
6. Vary LOAD2 from 10 A to 0 A. VOUT1 and VOUT2 should remain within regulation per Table 1.

6.2 Line Regulation Measurement Procedure

1. Set LOAD1 and LOAD2 to constant-current mode and to set to sink 10 A.
2. Vary VIN from 8.0 V to 15.0 V_{DC}. VOUT1 and VOUT2 should remain within regulation per Table 1.

6.3 Control Loop Gain and Phase Measurement Procedure

1. Connect a 1-kHz to 1-MHz isolation transformer to TP11, CHA1, and TP9, CHB1, for Output 1 or TP20, CHA2, and TP22, CHB2, for Output 2.
2. Connect the input signal amplitude measurement probe (Channel A) to TP11 with the ground lead connected to TP12 for Output 1 or TP20 with the ground lead connected to TP21 for Output 2.
3. Connect the output signal amplitude measurement probe (Channel B) to TP9 with the ground lead connected to TP10 for Output 1 or TP22 with the ground lead connected to TP22 for Output 2.
4. Inject a 25-mV, or less, signal across TP11 and TP9 for Output 1 or across TP20 and TP22 for Output 2 through the isolation transformer.
5. Sweep the frequency from 100 Hz to 1 MHz with 10-Hz or lower post filter.
6. Control loop gain can be measured by 20 x LOG(ChB/ChA)
7. Control loop phase is measured by the phase difference between ChA and ChB.
8. Disconnect the isolation transformer from the EVM before making other measurements. The signal injection into the feedback may interfere with the accuracy of other measurements.

6.4 Enabling/Disabling the Outputs

1. The user may disable Output 1 by shorting pin 2 on JP1 to pin 3 on JP1.
2. The user may disable Output 2 by shorting pin 2 on JP3 to pin 3 on JP3.

6.5 Sequencing the Outputs

1. The user can sequence the outputs so that Output 2 starts before Output 1 by shorting pin 1 of JP2 to pin 2 of JP2.
2. The user can sequence the outputs so that Output 1 starts before Output 2 by shorting pin 1 of JP4 to pin 2 of JP4.

6.6 Equipment Shutdown

1. Shut down LOAD1 and LOAD2.
2. Shut down VIN.

7 Performance Data and Typical Characteristic Curves

Figure 4 through Figure 18 present typical performance curves for the TPS40322EVM-679. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

7.1 Efficiency

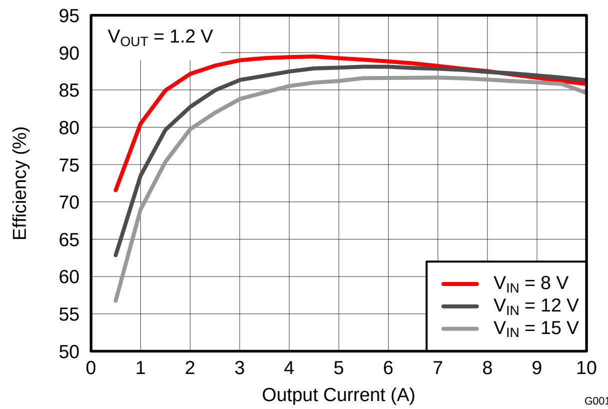

Figure 4. TPS40322EVM-679 VOUT1 Efficiency, (VOUT2 disabled)

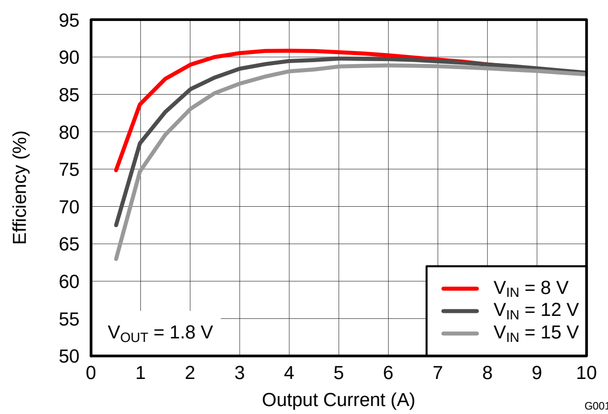

Figure 5. TPS40322EVM-679 VOUT2 Efficiency, (VOUT1 disabled)

7.2 Load Regulation

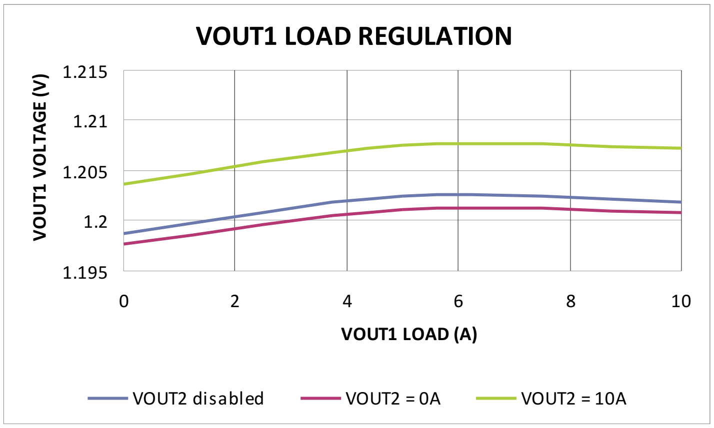

Figure 6. TPS40322EVM-679 VOUT1 Load Regulation, (VIN = 12 V)

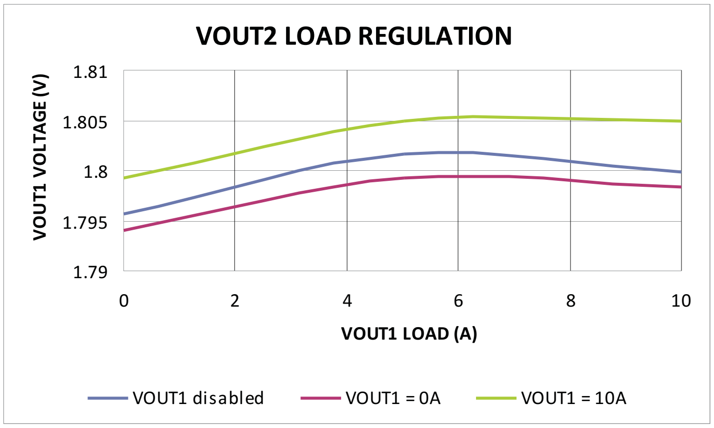

Figure 7. TPS40322EVM-679 VOUT2 Load Regulation, (VIN = 12 V)

7.3 Line Regulation

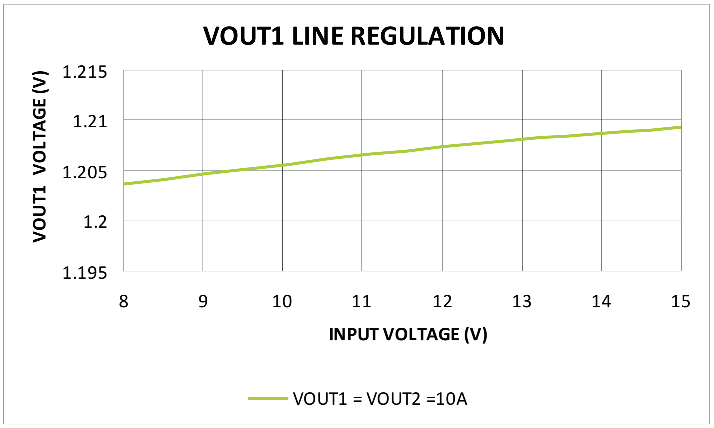

Figure 8. TPS40322EVM-679 VOUT1 Line Regulation

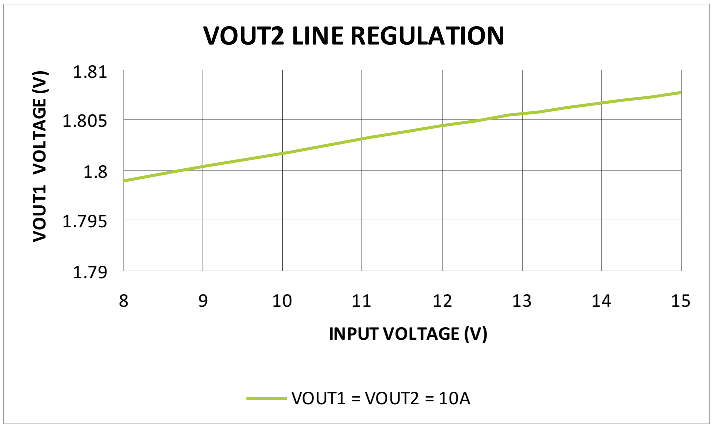

Figure 9. TPS40322EVM-679 VOUT2 Line Regulation

7.4 Bode Plot

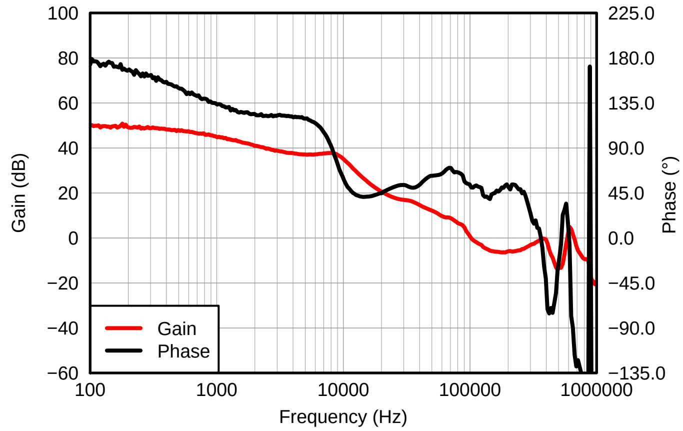

Figure 10. TPS40322EVM-679 VOUT1 Loop Response Gain and Phase, (VIN = 12 V I_{OUT1} = 10 A)

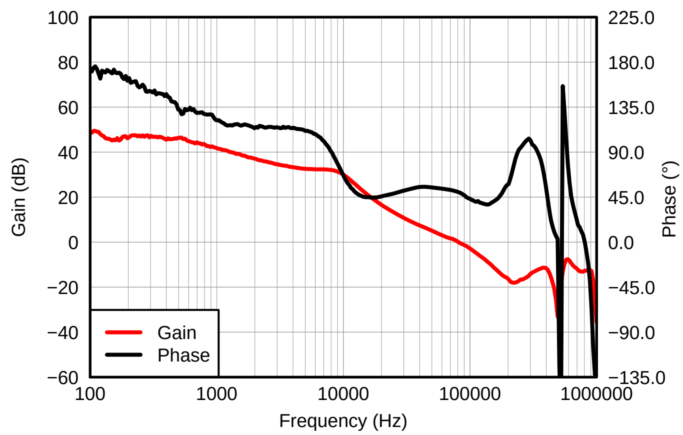

Figure 11. TPS40322EVM-679 VOUT2 Loop Response Gain and Phase, (VIN = 12 V I_{OUT2} = 10 A)

7.5 Output Ripple

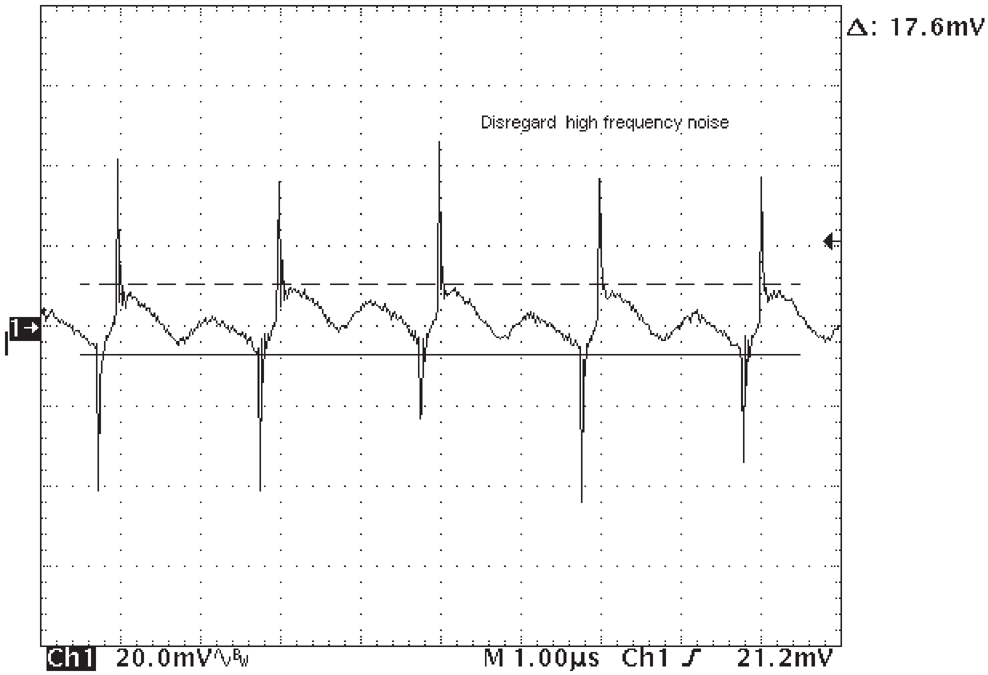

Figure 12. VOUT1 Output Ripple, (VIN = 12 V, I_{OUT1} = 10 A)

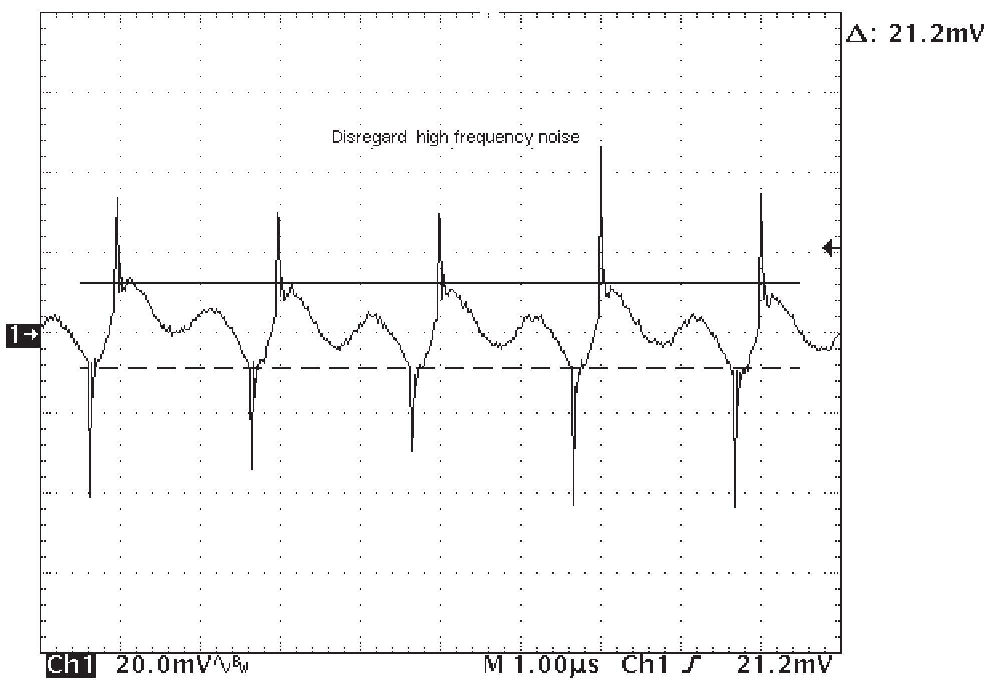

Figure 13. VOUT2 Output Ripple, (VIN = 12 V, I_{OUT2} = 10 A)

7.6 Switching Waveforms

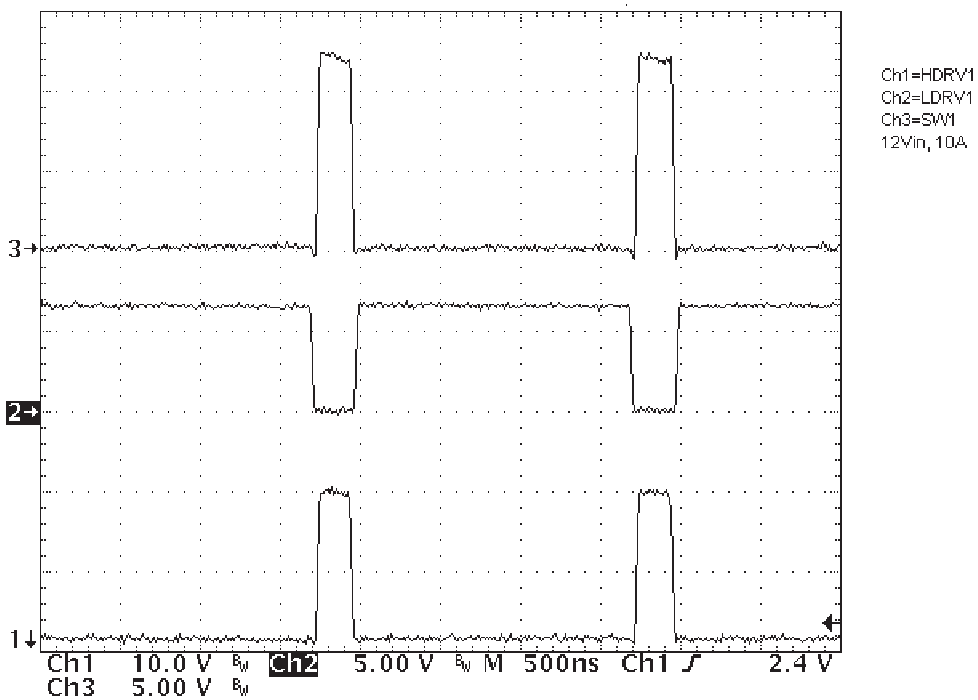

Figure 14. Output 1 Switching waveform, (Ch1 = HDRV1, Ch2 = LDRV1, Ch3 = SW1, VIN = 12 V, I_{OUT1} = 10 A)

7.7 Turn-On Waveform

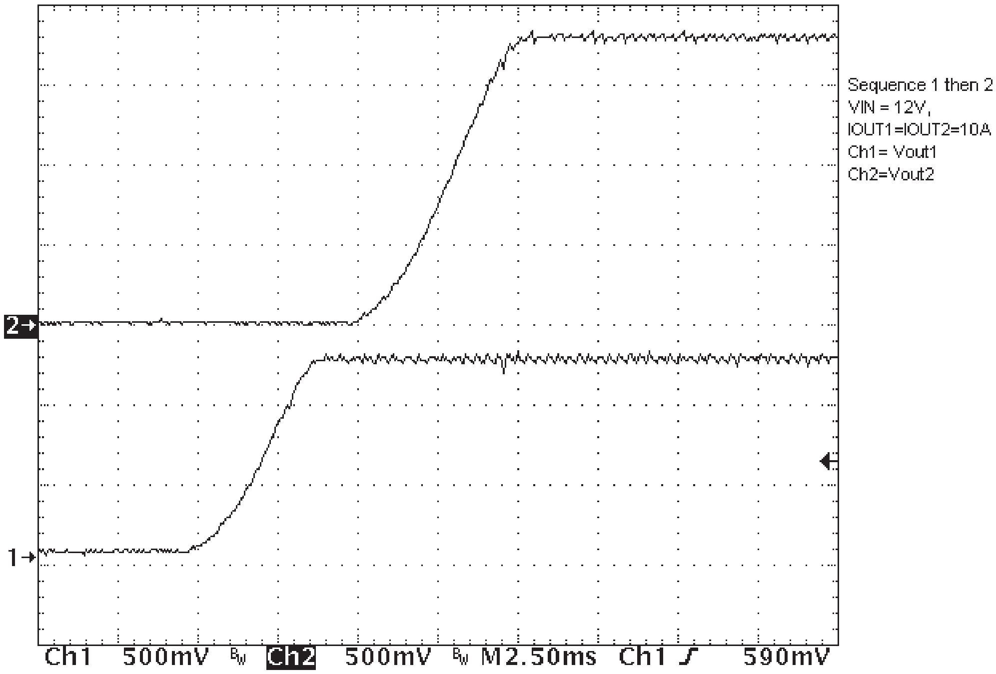

Figure 15. Enable Turn-On Waveform, (Sequencing VOUT1 then VOUT2, Ch1 = VOUT1, Ch2 = VOUT2, VIN = 12 V, I_{OUT1} = I_{OUT2} = 10 A)

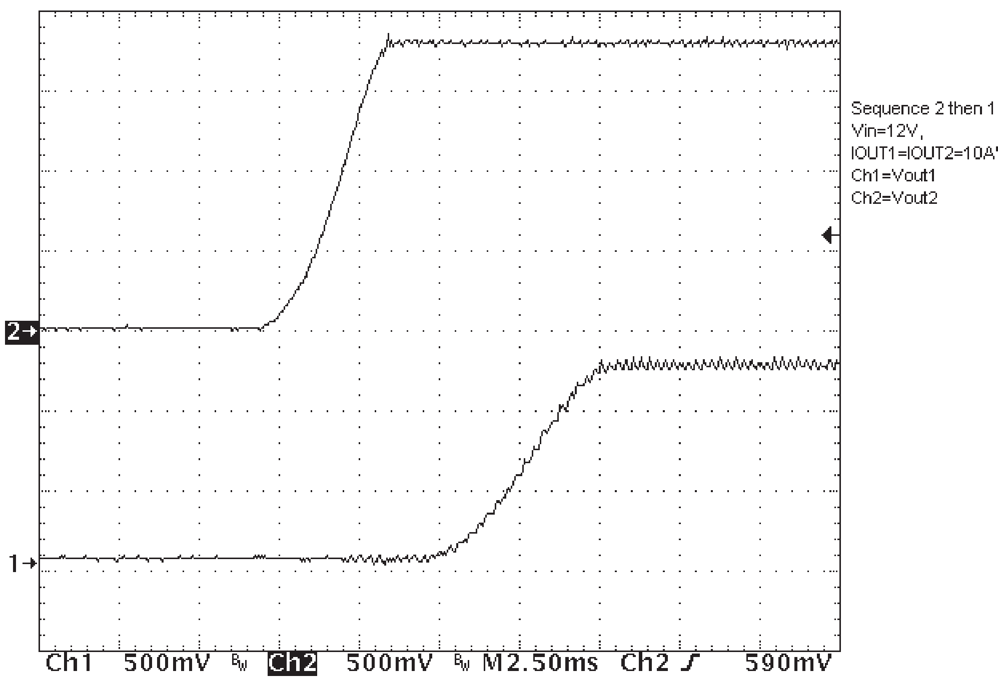

Figure 16. Enable Turn-On waveform, (Sequencing VOUT2 then VOUT1, Ch1 = VOUT1, Ch2 = VOUT2, VIN = 12 V, I_{OUT1} = I_{OUT2} = 10 A)

7.8 Turn-Off Waveform

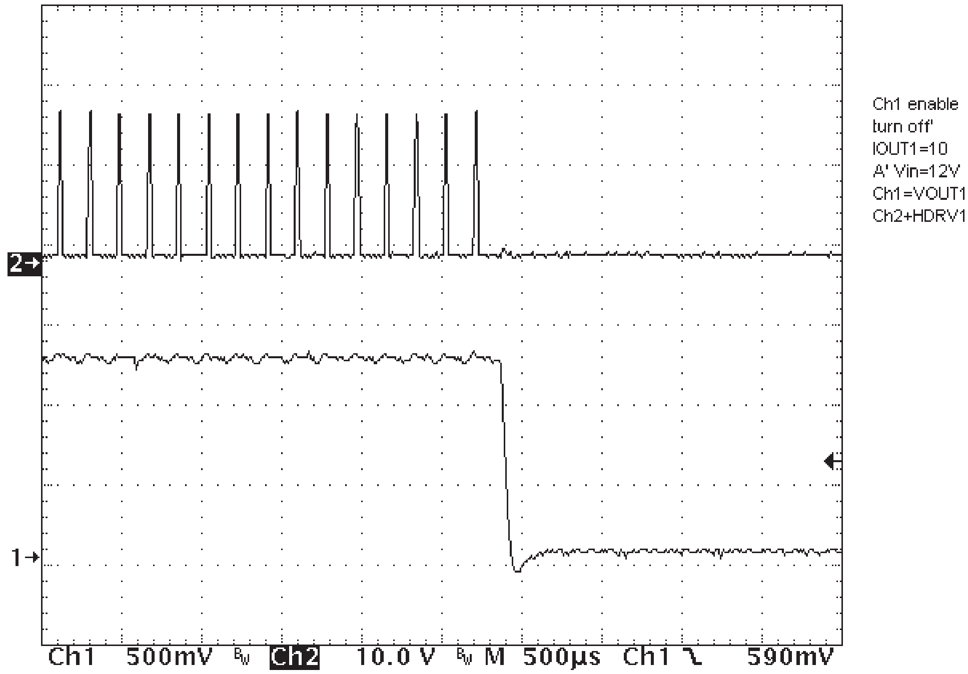

Figure 17. Enable Turn-Off waveform, Ch1 = VOUT1, Ch2 = HDRV1, VIN = 12 V, I_{OUT1} = 10 A

7.9 Master Mode Function

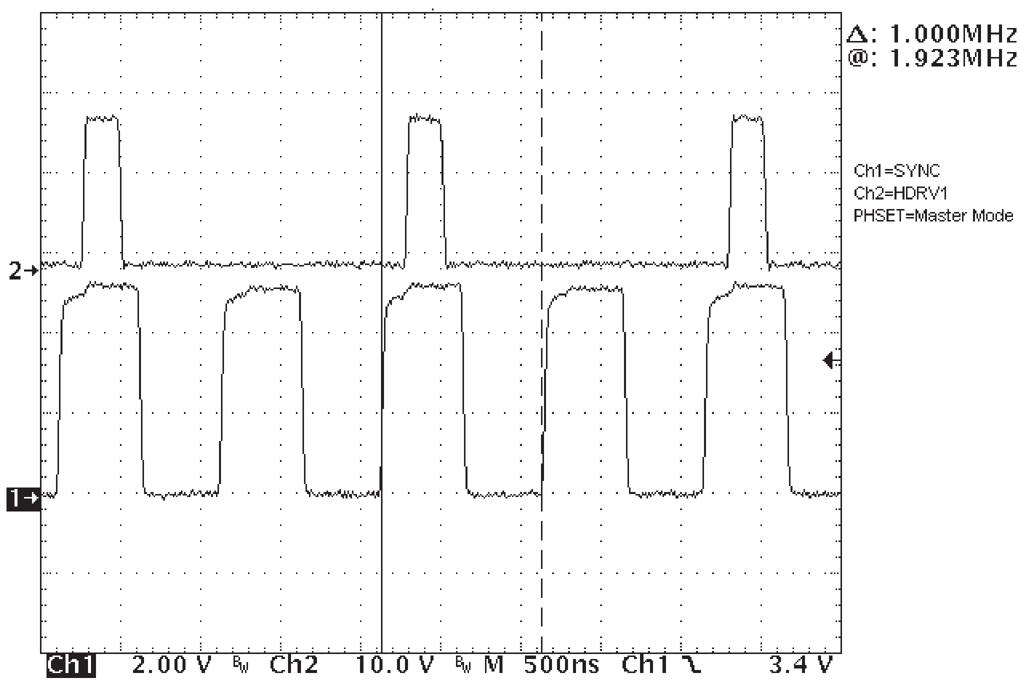

Figure 18. PHSET Shorted to Master Mode (JP5 pin 2 to JP5 pin 3, Ch1 = SYNC 1.00 MHz, Ch2 = HDRV1)

8 EVM Assembly Drawings and PCB layout (TPS40322EVM-679)

Figure 19 through Figure 26 show the design of the TPS40322EVM-679 printed circuit board, HPA679.

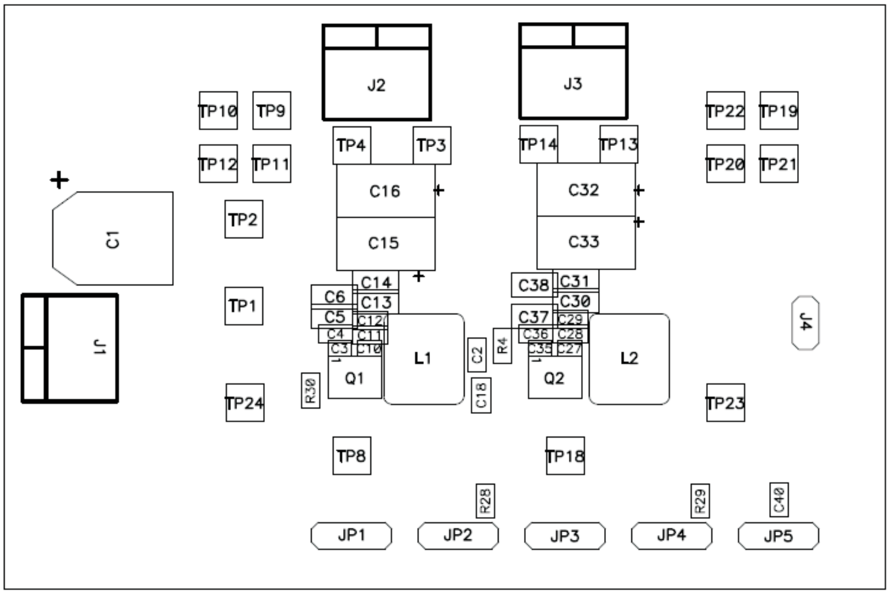

Figure 19. Top Layer Assembly Drawing (top view)

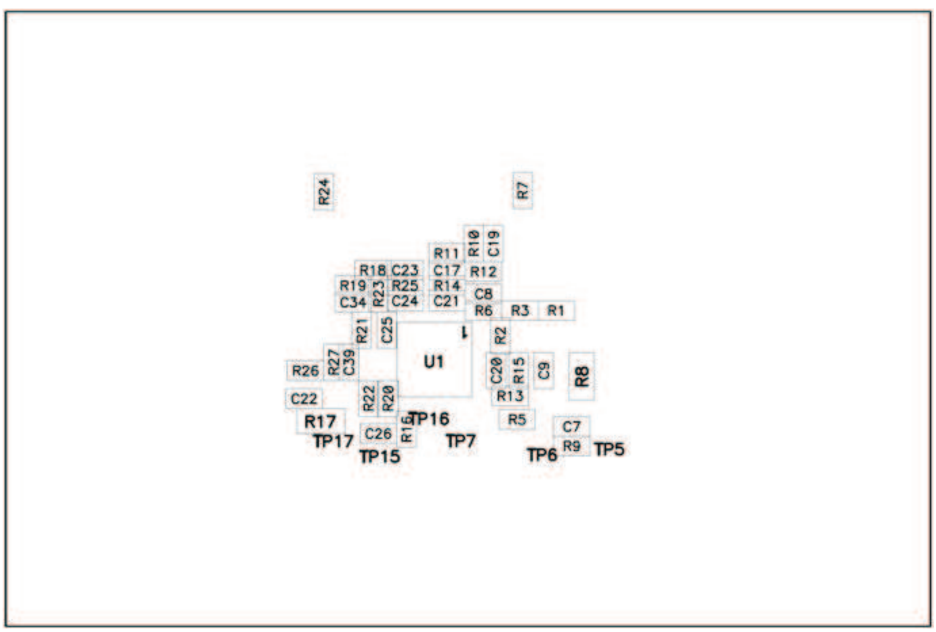

Figure 20. Bottom Assembly Drawing (bottom view)

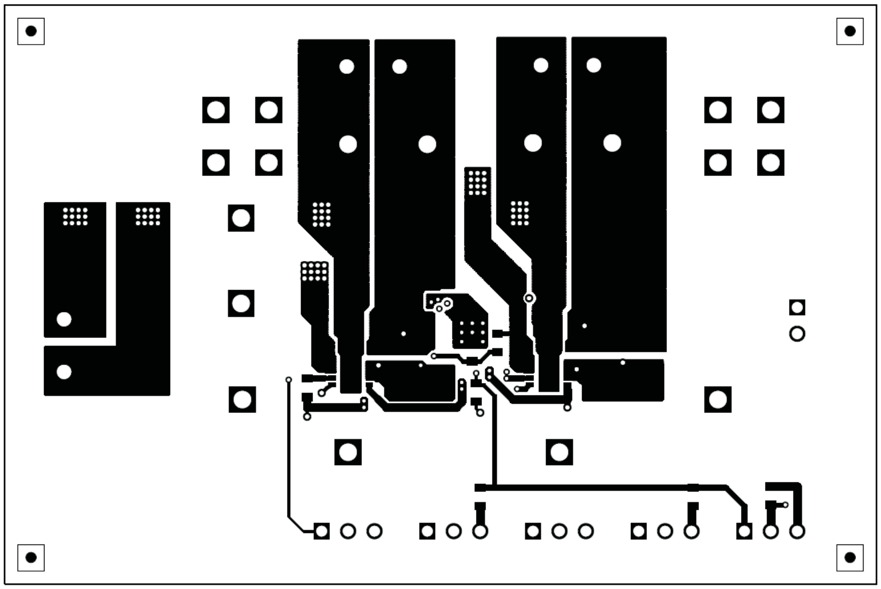

Figure 21. Top Copper (top view)

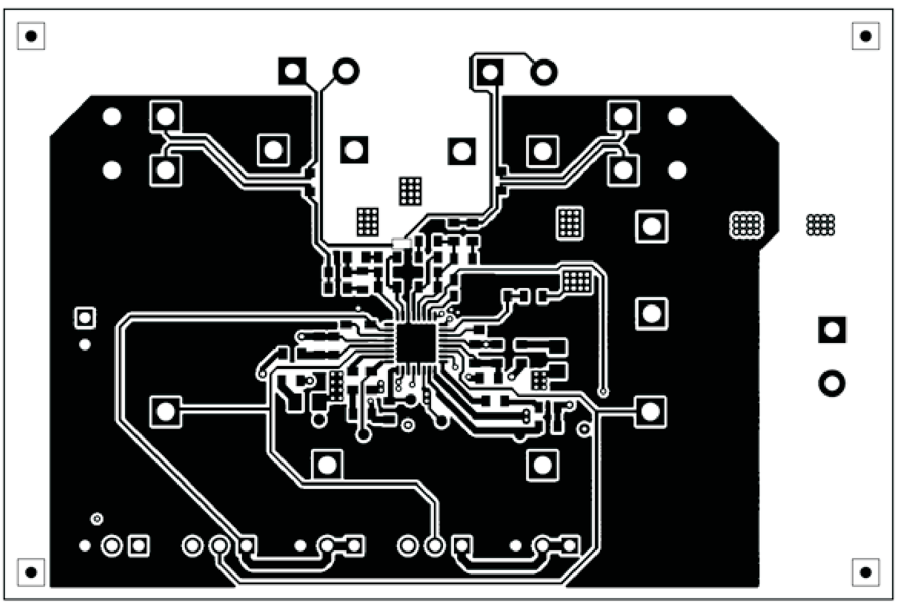

Figure 22. Bottom Copper (bottom view)

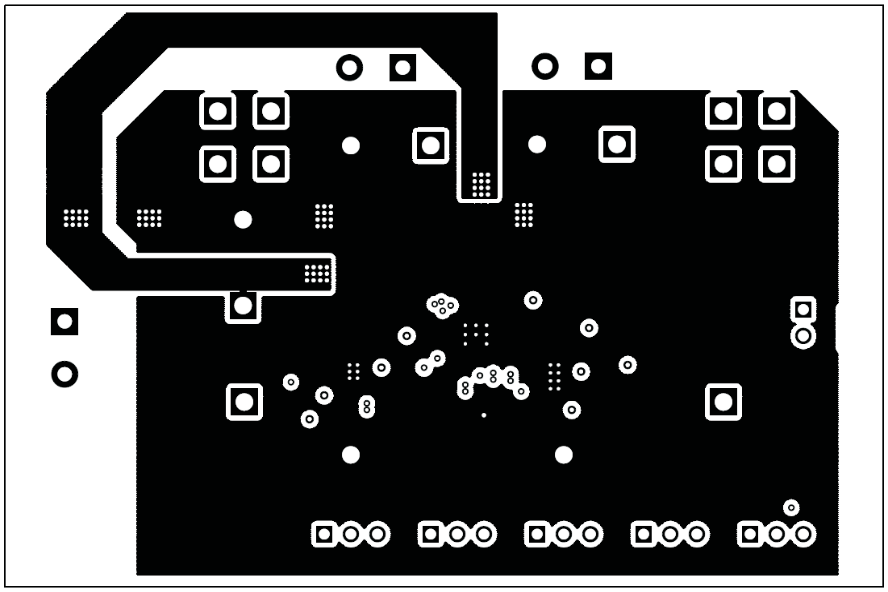

Figure 23. Internal Layer 1 (top view)

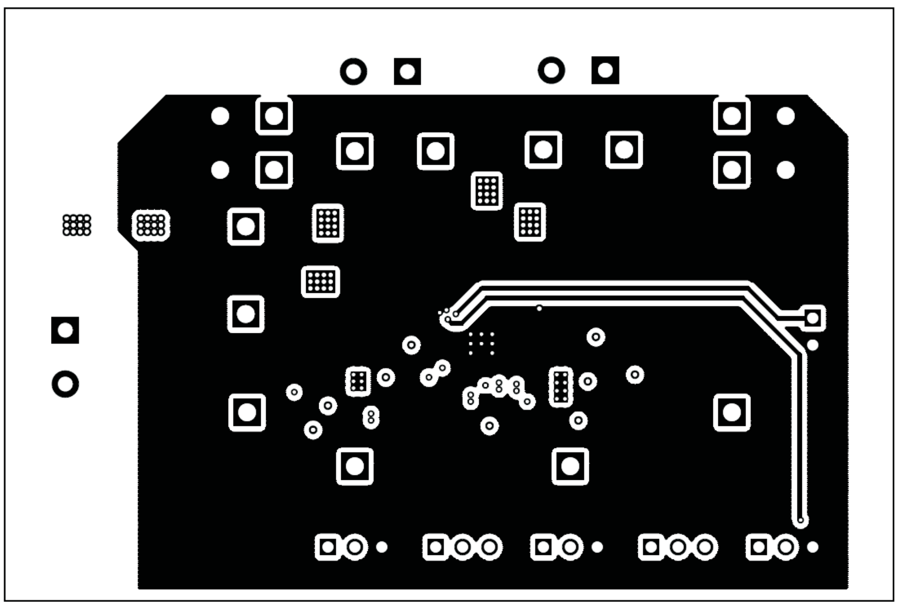

Figure 24. Internal Layer 2 (top view)

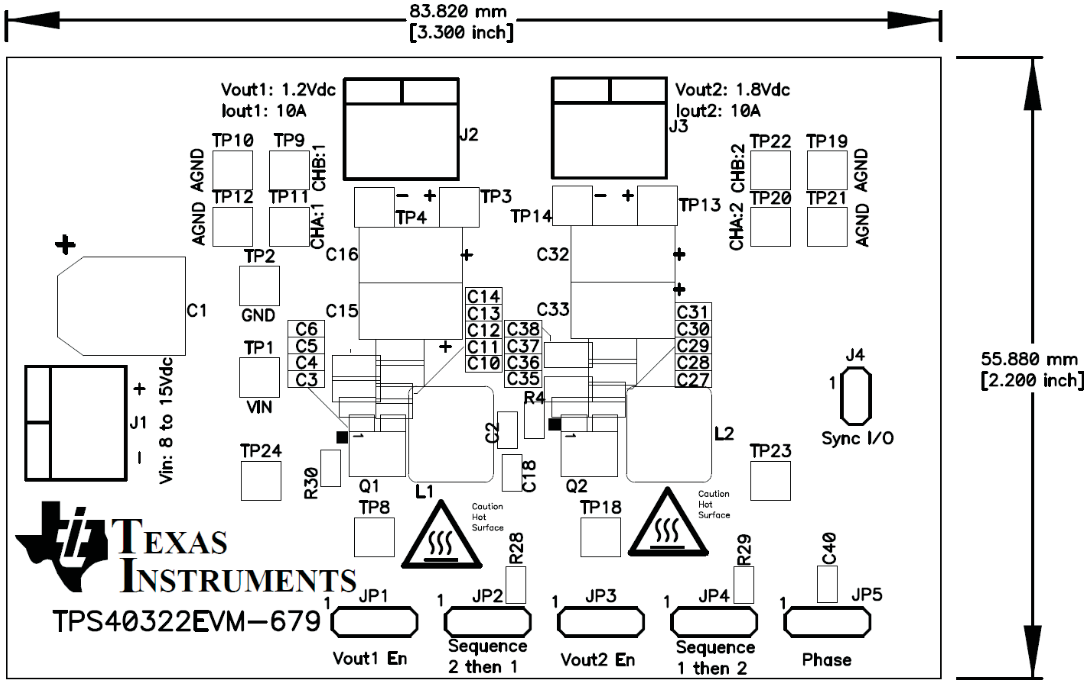

Figure 25. Top Silk (top view)

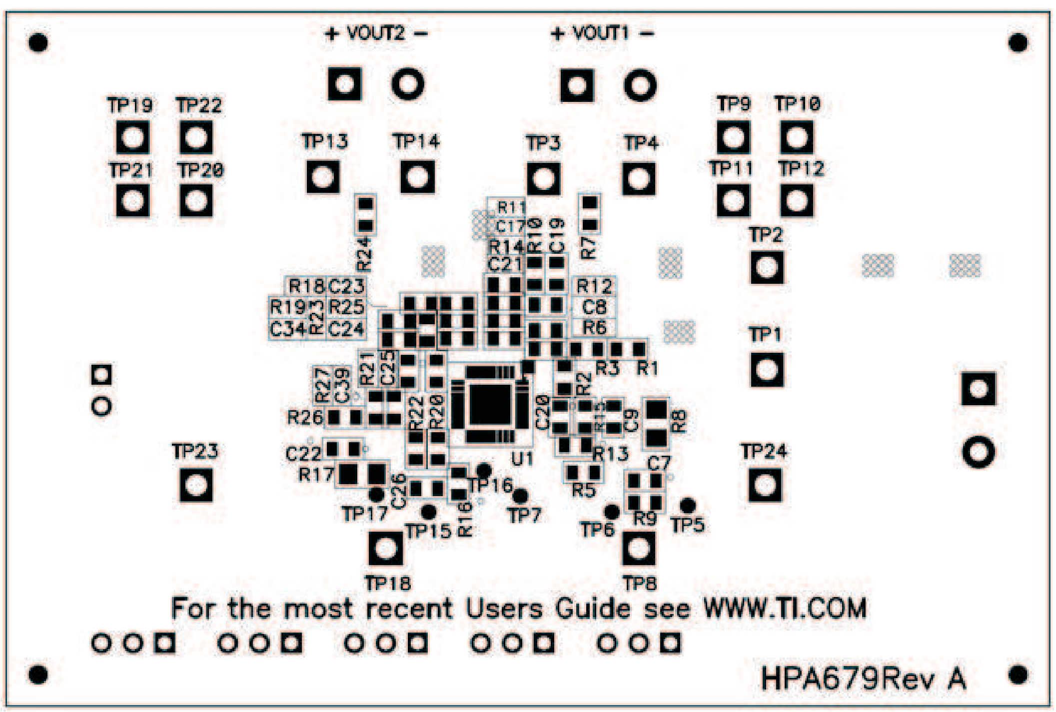

Figure 26. Bottom Silk (bottom view)

9 List of Materials

List of materials for the TPS40322EVM-679.

Table 3. List of Materials

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
1	C1	Capacitor, aluminum, 100 μF, 35 V, ±20%, 0.328 x 0.328 inch	EEV-FK1V101GP	Panasonic - ECG
5	C2, C7, C20, C26, C39	Capacitor, ceramic, 0.1 μF, 50 V, X7R, ±10%, 0603	Std	Std
2	C3, C35	Capacitor, ceramic, 0.1 μF, 25 V, X5R, ±10%, 0402	Std	Std
2	C4, C36	Capacitor, ceramic, 1.0 μF, 25 V, X7R, ±10%, 0603	Std	Std
4	C5, C6, C37, C38	Capacitor, ceramic, 10 μF, 25 V, X5R, ±10%, 0805	Std	Std
2	C8, C25	Capacitor, ceramic, 33 nF, 16 V, X7R, ±10%, 0603	Std	Std
4	C9, C19, C22, C34	Capacitor, ceramic, 470 pF, 25 V, C0G, NP0, ±5%, 0603	Std	Std
2	C10, C27	Capacitor, ceramic, 1.0 μF, 6.3 V, X5R, ±10%, 0402	Std	Std
5	C11, C12, C18, C28, C29	Capacitor, ceramic, 3.3 μF, 10 V, X5R, ±10%, 0603	C1608X5R1A335K	TDK Corporation
4	C13, C14, C30, C31	Capacitor, ceramic, 10 μF, 6.3 V, X7R, ±10%, 0805	Std	Std
4	C15, C16, C32, C33	Capacitor, polymer aluminum, 220 μF, 4 V, ±20%, 5 mΩ ESR	EEF-SE0G221ER	Panasonic - ECG
2	C17, C23	Capacitor, ceramic, 220 pF, 50 V, C0G, NP0, ±5%, 0603	Std	Std
2	C21, C24	Capacitor, ceramic, 10 pF, 50 V, C0G, NP0, ±5%, 0603	Std	Std
1	C40	Capacitor, ceramic, 1.0 nF, 25 V, C0G, NP0, ±5%, 0603	Std	Std
2	L1, L2	Inductor, power choke, 1.1 μH, ±20%, 3.15 mΩ, 7.0 x 6.9 mm	744314110	Wurth Elektronik
2	Q1, Q2	MOSFET, Synchronous Buck NexFET Power Block, QFN-8 POWER	CSD86330Q3D	Texas Instruments

Table 3. List of Materials (continued)

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
1	R1	Resistor, chip, 68.1 kΩ, 1/10 W, ±1%, 0603	Std	Std
2	R2, R21	Resistor, chip, 86.6 kΩ, 1/10 W, ±1%, 0603	Std	Std
1	R3	Resistor, chip, 12.7 kΩ, 1/10 W, ±1%, 0603	Std	Std
3	R4, R5, R22	Resistor, chip, 1.00 Ω, 1/10 W, ±1%, 0603	Std	Std
1	R6	Resistor, chip, 40.2 kΩ, 1/10 W, ±1%, 0603	Std	Std
2	R7, R24	Resistor, chip, 49.9 Ω, 1/10 W, ±1%, 0603	Std	Std
2	R8, R17	Resistor, chip, 5.11 Ω, 1/8 W, ±1%, 0805	Std	Std
2	R9, R16	Resistor, chip, 0 Ω, 1/10 W, ±1%, 0603	Std	Std
4	R10, R14, R19, R27	Resistor, chip, 20.0 kΩ, 1/10 W, ±1%, 0603	Std	Std
2	R11, R18	Resistor, chip, 82.5 kΩ, 1/10 W, ±1%, 0603	Std	Std
2	R12, R23	Resistor, chip, 1.62 kΩ, 1/10 W, ±1%, 0603	Std	Std
1	R13	Resistor, chip, 3.09 kΩ, 1/10 W, ±1%, 0603	Std	Std
1	R15	Resistor, chip, 29.4 kΩ, 1/10 W, ±1%, 0603	Std	Std
2	R20, R30	Resistor, chip, 5.11 Ω, 1/10 W, ±1%, 0603	Std	Std
1	R25	Resistor, chip, 10.0 kΩ, 1/10 W, ±1%, 0603	Std	Std
1	R26	Resistor, chip, 3.24 kΩ, 1/10 W, ±1%, 0603	Std	Std
2	R28, R29	Resistor, chip, 100 kΩ, 1/10 W, ±1%, 0603	Std	Std
1	U1	TPS40322 Dual Synchronous Buck Controller, QFN-32	TPS40322RHB	Texas Instruments

Evaluation Board/Kit Important Notice

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During normal operation, some circuit components may have case temperatures greater than 50° C. The EVM is designed to operate properly with certain components above 50° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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