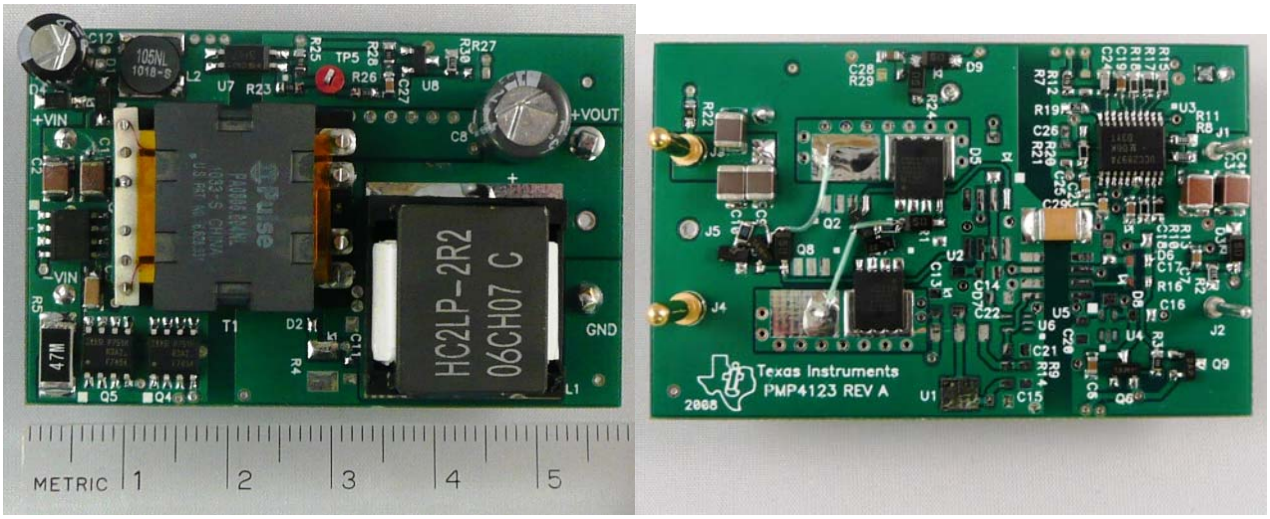
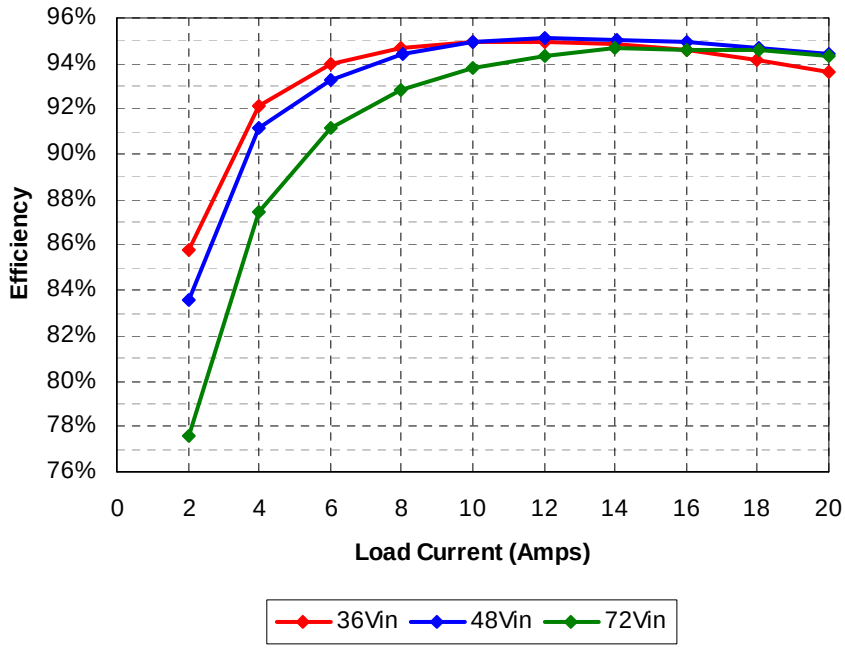
1 Photo

The photos below show the top and bottom views of the PMP5364 Rev B assembly. This circuit was built using a PMP4123 Rev A circuit board.



2 Efficiency

The efficiency data is shown in the tables and graph below.



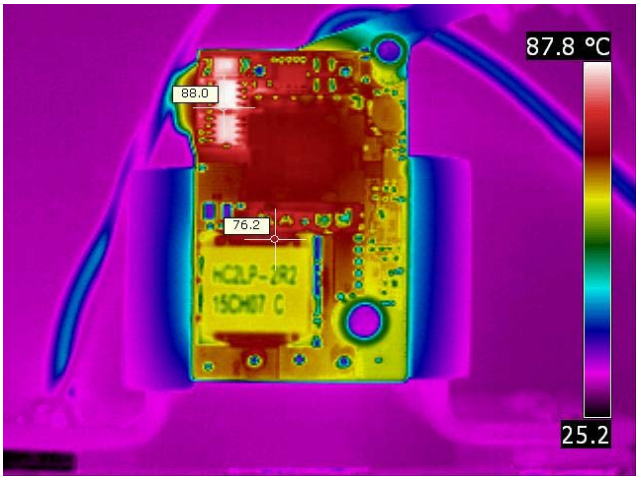
Vin	Iin	Iout	Vout	Pout	Losses	Efficiency
36.0	0.053	0.000	4.99	0.00	1.908	0.0%
36.0	0.323	1.999	4.99	9.98	1.652	85.8%
36.0	0.602	4.000	4.99	19.96	1.709	92.1%
36.0	0.885	6.00	4.99	29.94	1.916	94.0%
36.0	1.171	8.00	4.99	39.92	2.231	94.7%
36.0	1.460	10.00	4.99	49.90	2.653	95.0%
36.0	1.753	12.01	4.99	59.93	3.178	95.0%
36.0	2.047	14.00	4.99	69.86	3.823	94.8%
36.0	2.343	15.99	4.99	79.79	4.546	94.6%
36.0	2.644	18.00	4.98	89.64	5.531	94.2%
36.0	2.955	20.0	4.98	99.60	6.780	93.6%

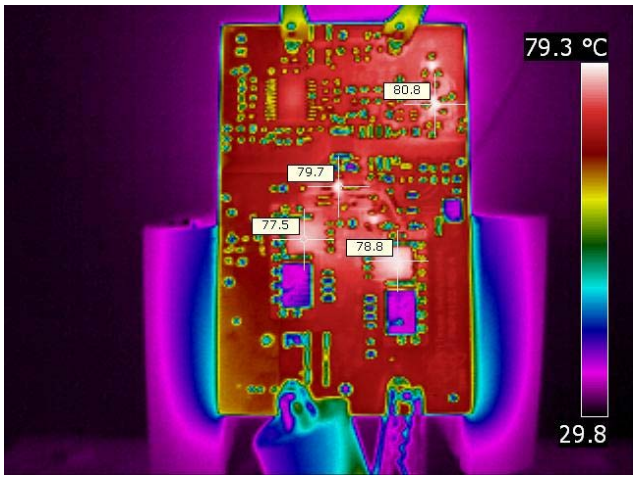
Vin	Iin	Iout	Vout	Pout	Losses	Efficiency
48.0	0.044	0.000	4.99	0.00	2.112	0.0%
48.0	0.251	2.017	4.99	10.06	1.982	83.6%
48.0	0.456	3.998	4.99	19.95	1.935	91.2%
48.0	0.669	6.00	4.99	29.94	2.168	93.2%
48.0	0.882	8.01	4.99	39.97	2.360	94.4%
48.0	1.096	10.01	4.99	49.95	2.650	95.0%
48.0	1.313	12.01	4.99	59.93	3.085	95.1%
48.0	1.534	14.02	4.99	69.96	3.661	95.0%
48.0	1.753	16.01	4.99	79.89	4.241	95.0%
48.0	1.977	18.01	4.99	89.87	5.011	94.7%
48.0	2.200	20.0	4.98	99.65	5.932	94.4%

Vin	Iin	Iout	Vout	Pout	Losses	Efficiency
72.0	0.042	0.000	4.99	0.00	3.024	0.0%
72.0	0.179	2.004	4.99	10.00	2.888	77.6%
72.0	0.317	4.002	4.99	19.97	2.854	87.5%
72.0	0.456	6.00	4.99	29.94	2.892	91.2%
72.0	0.597	8.00	4.99	39.92	3.064	92.9%
72.0	0.739	10.00	4.99	49.90	3.308	93.8%
72.0	0.883	12.02	4.99	59.98	3.596	94.3%
72.0	1.026	14.01	4.99	69.91	3.962	94.6%
72.0	1.173	16.01	4.99	79.89	4.566	94.6%
72.0	1.320	18.01	4.99	89.87	5.170	94.6%
72.0	1.469	20.0	4.99	99.80	5.968	94.4%

3 Thermal Images

The thermal images below show a top view (left) and bottom view (right) of the board. The ambient temperature was 26ºC with no forced air flow. The output was loaded with 15A and the input was 48V.

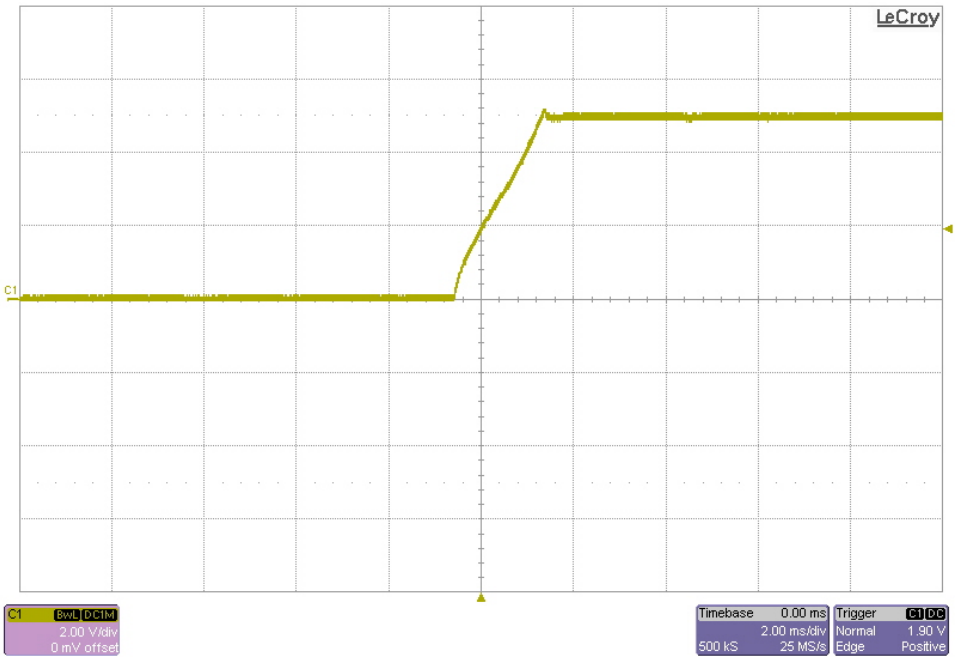




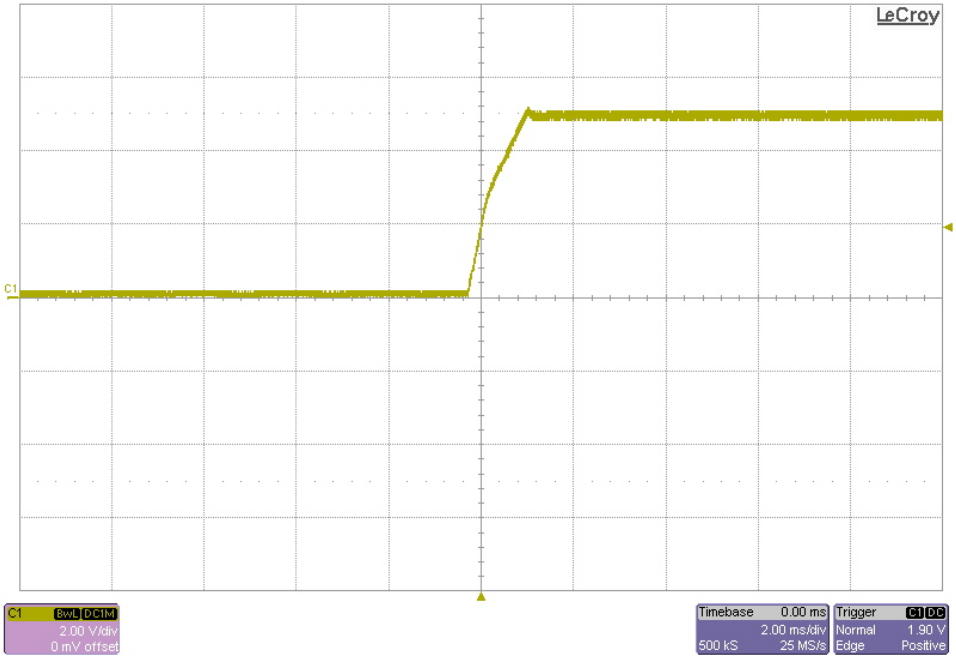
4 Startup

The output voltage at startup is shown in the images below.

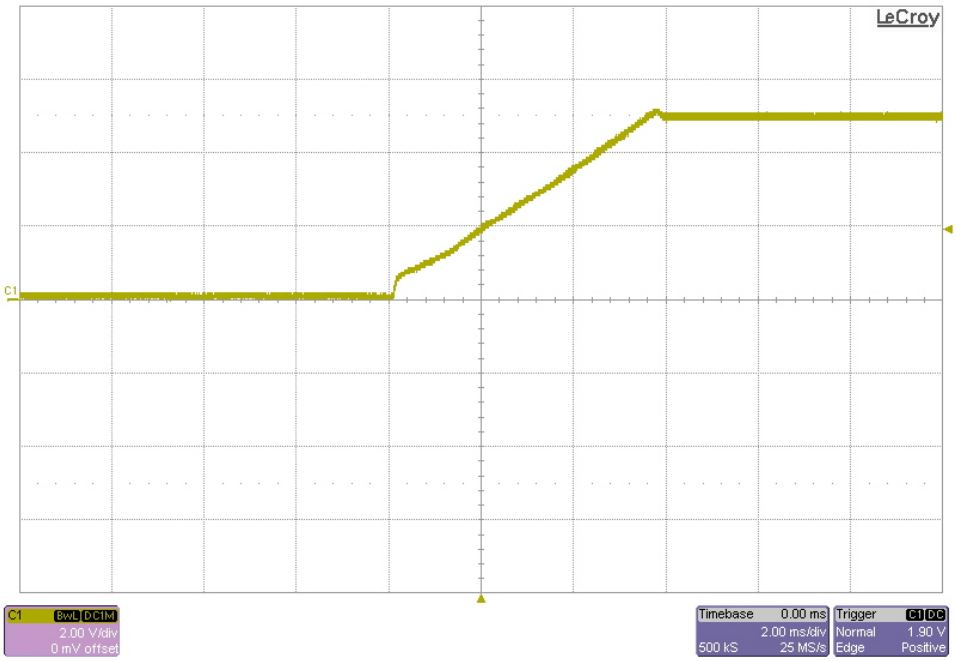
4.1 36Vin No Load



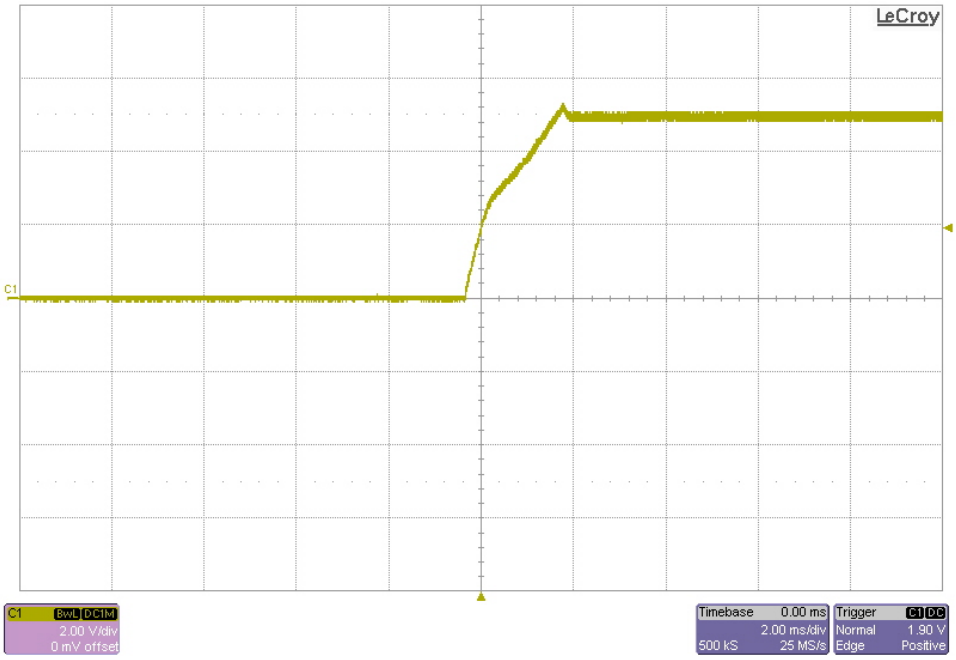
4.2 72Vin No Load



4.3 36Vin, 20A Load

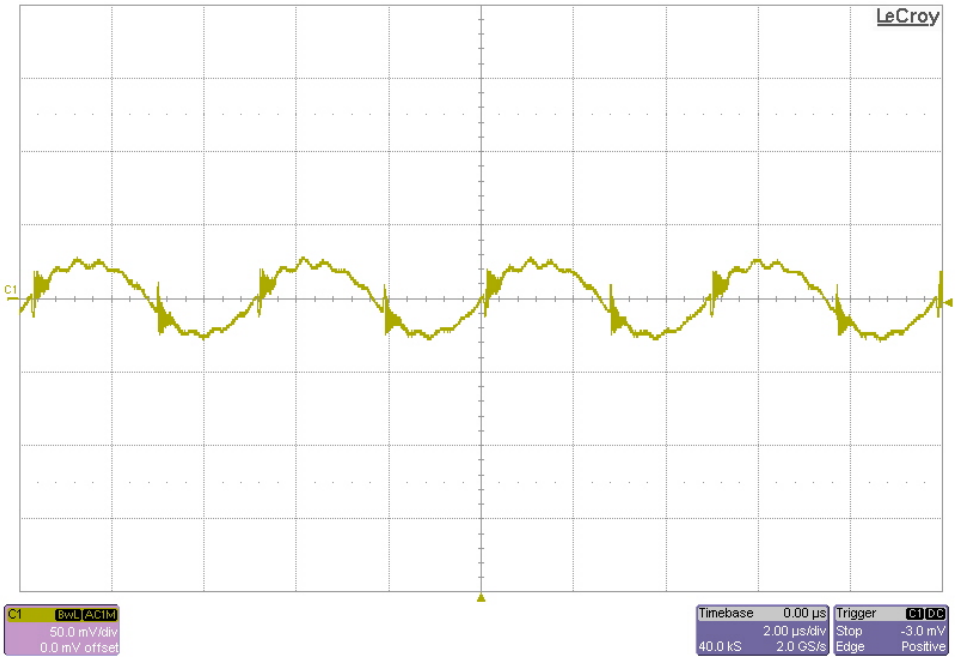


4.4 72Vin, 20A Load



5 Output Ripple Voltage

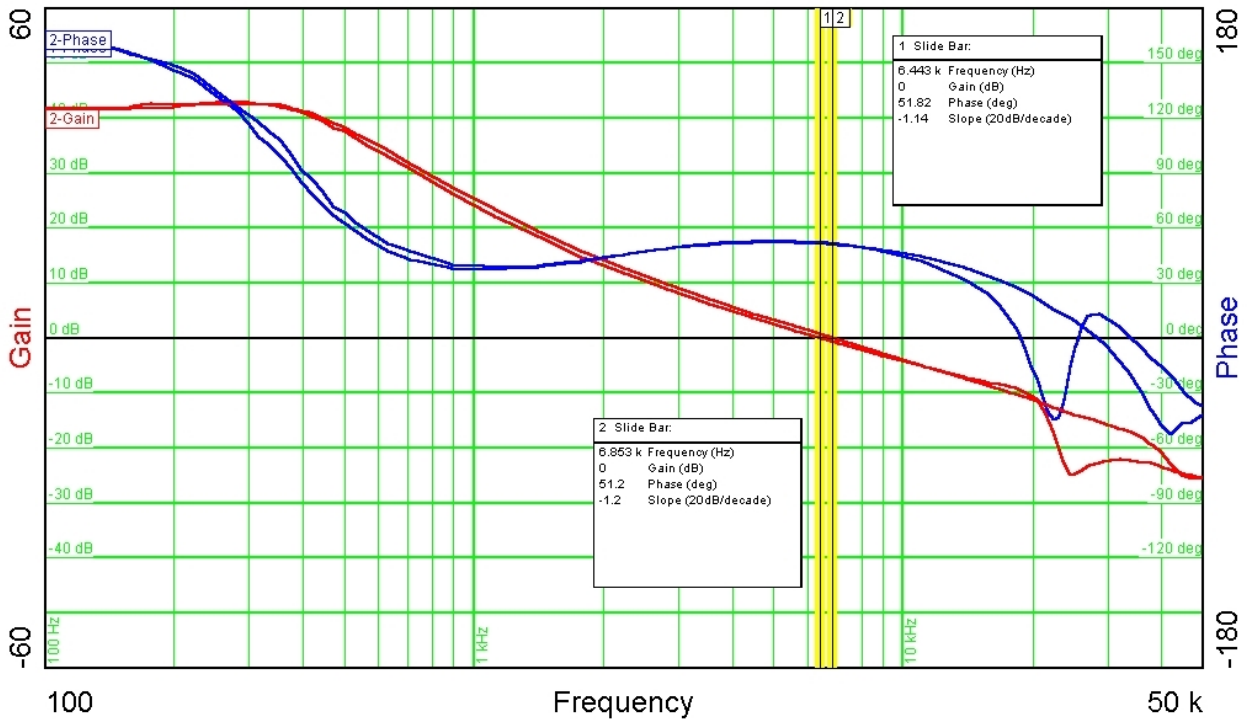
The output ripple voltage during full load operation (20A load) is shown in the plot below. The input voltage was set to 48VDC.



6 Loop Response

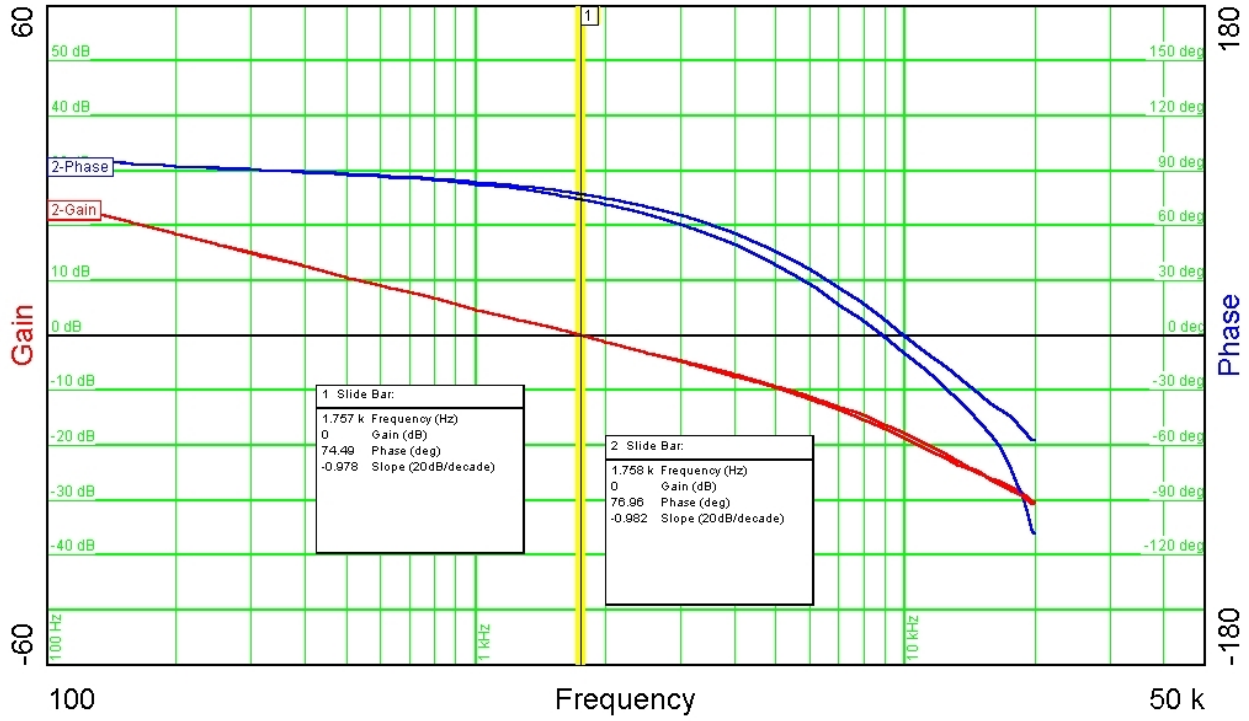
6.1 Loop Measured at R22

The image below shows the loop response of the converter measured across R22 (20 Ohms). For the upper gain/phase plot, the input was 72Vdc. For the lower gain/phase plot, the input was 36Vdc. The output was loaded with 20A.



6.2 Loop Measured at R26

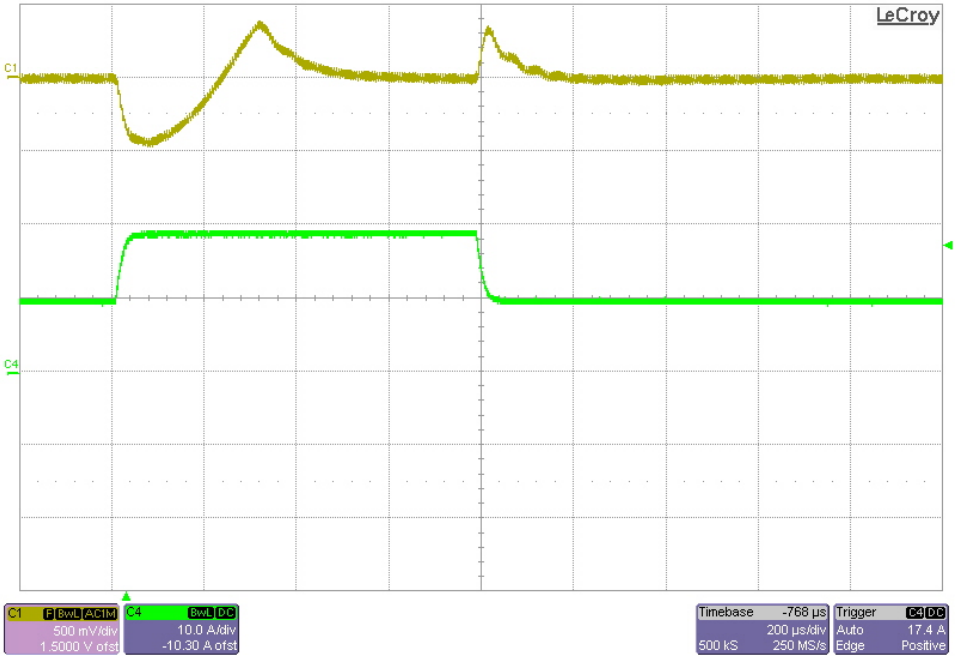
The image below shows the loop response of the converter measured across a 50 ohm resistor connected in series with R26.). For the upper gain/phase plot, the input was 72Vdc. For the lower gain/phase plot, the input was 36Vdc. The output was loaded with 20A.

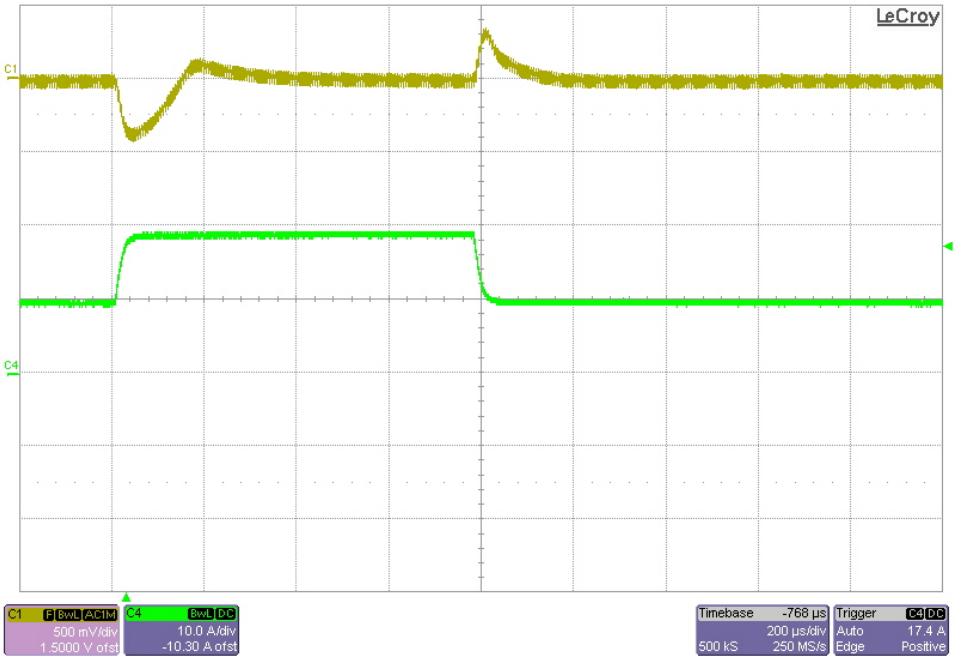


7 Load Transients

The image below shows the response to a 10A to 20A load transient. For the upper plot, the input voltage was set to 36VDC. For the lower plot, the input voltage was 72VDC.

Channel 1: Vout (ac coupled) 500mV/div Channel 4: Iout 10A/div

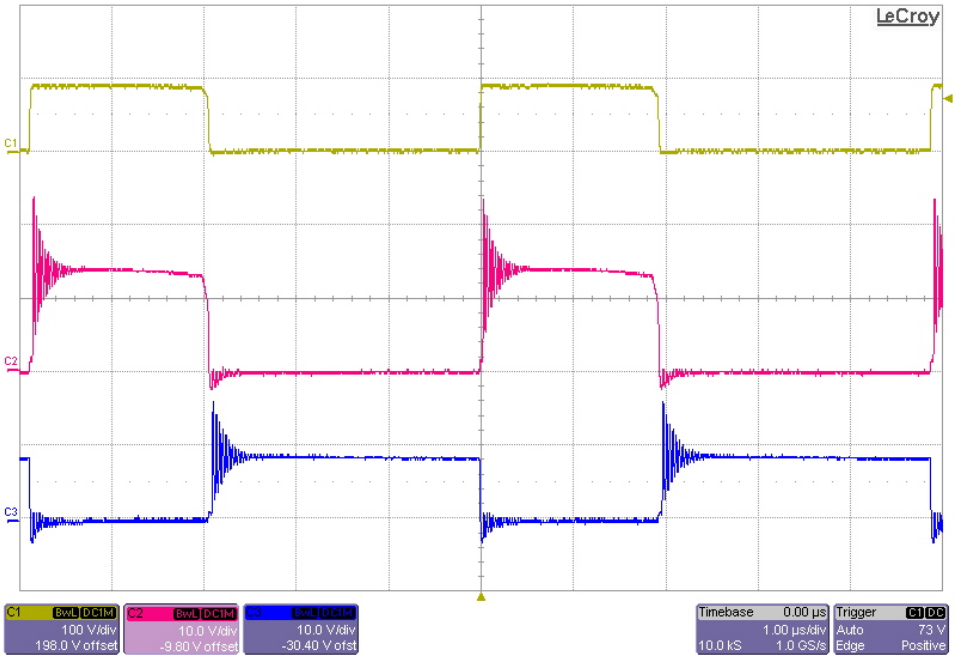


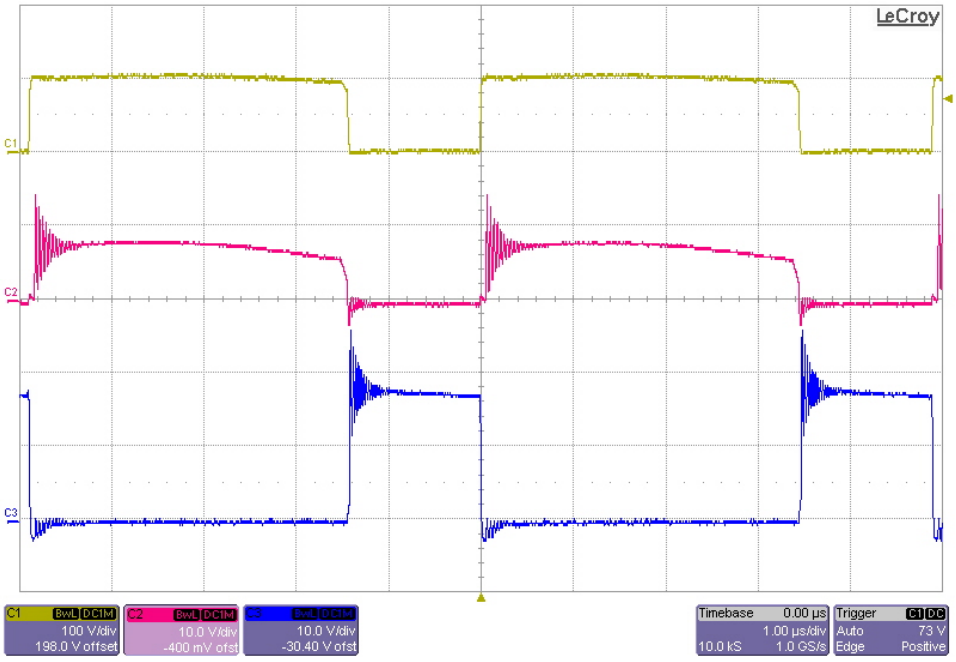


8 Switching Waveforms

The images below show the drain-to-source voltage waveforms on the switching MOSFETs. The output was loaded with 20A. For the top image, the input was set to 36V. For the bottom image, the input was set to 72V.

Channel 1: Q4 & Q5 Vds Channel 2: Q1 Vds
Channel 3: Q7 Vds




LeCroy
C1
C2
C3
C1 BwL DC1M
100 V/div
198.0 V offset
C2 BwL DC1M
10.0 V/div
-400 mV ofst
C3 BwL DC1M
10.0 V/div
-30.40 V ofst
Timebase 0.00 µs
1.00 µs/div
10.0 kS 1.0 GS/s
Trigger C1 DC
Auto 73 V
Edge Positive

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