

Krunal Bhargav, Neelima Muralidharan, Tarkesh Pande

ABSTRACT

AM62x Sitara processors are TI's entry-level automotive-grade processors targeted for safety critical automotive applications like driver monitoring systems and entry-level digital cluster. This application note describes how important IP features in AM62x can enable the implementation of an entry-level digital cluster concept.

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1 Introduction

A digital cluster is a digital instrumentation panel that displays important vehicle information like speed, engine RPM, and fuel gauge status and other vehicle diagnostics through a conventional set of dials and warning lights. Cluster technology evolution, from analog meters and gauges to all digital, has been accelerated by the need in the automotive industry for displaying increased features with improved graphics, while simultaneously meeting critical safety requirements. The AM62x processor family has been architected with entry-level digital cluster requirements in consideration.

The AM62x processor is a heterogeneous processor architecture which consists of different compute cores for different tasks, thus enabling efficient low-power computation. The main application processor consists of up to Quad A-53 ARM[®] processors alongside a powerful 3D graphics engine. There is an integrated safety island with an M4F MCU channel that can operate independently from the main processing cores and is designed to meet ASIL-B automotive functional safety requirements. AM62x also meets both SHE 1.1 and EVITA compliance. Automotive grade security is enabled with the presence of a hardware security manager (HSM) module, which consists of dual M4F cores.

This application note takes a system-level overview of how an entry-level cluster design can be implemented on AM62x. With advancing embedded technologies, car manufacturers are able to take advantage of new hardware as well as software features, to provide an enhanced and safe driving experience to the consumer. As automotive safety standards and regulations gain prominence, providing safety designs for any automotive application becomes imperative. These safety design can include the use of tell-tales, which are warning lights or indicators on the digital cluster that are crucial for the safety of the vehicle. The accuracy and timeliness of a tell-tale display on the instrument cluster is safety critical.

As a cluster design involves displaying a digital display, this application note begins by first going through the display pipeline, consisting of the GPU and Display Subsystem. After the display pipeline is introduced, how the AM62x provides all the necessary safety features to meet ASIL-B as per the ISO 26262 standard is discussed, using an example software cluster tell-tale application.



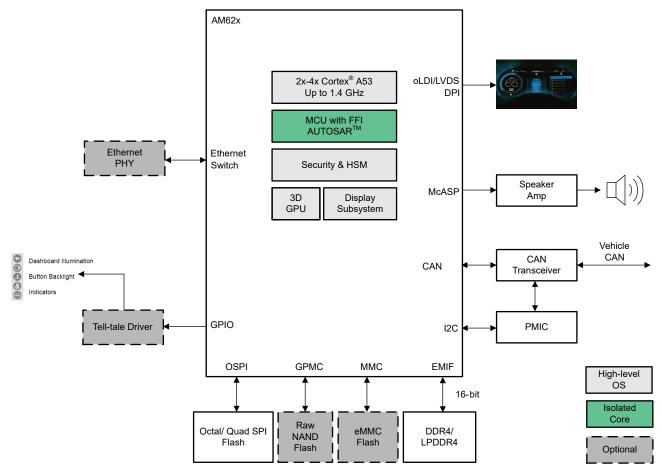


Figure 1-1. Block Diagram of Cluster Design

Figure 1-1 shows a high-level system block diagram for a digital cluster design based on the TI AM62x processor. In a typical application, the processor runs a high-level operation system such as Linux[®], QNX[®], or INTEGRITY[®] and manages all system components.

In addition to the application processor, the block diagram includes many other system components, such as:

- Display Subsystem paired with 2 × OLDI (4 Lanes) for driving LCD panels.
- Flash to store boot images and the files system.
- MCU to manage input and output, full system wake-up and potentially the controller area network (CAN) stack.
- Camera input to feed input from driver-monitoring cameras. This input can be useful in instances where a system design needs to support an entry-level driver monitoring and cluster application.
- Graphical processing unit (GPU) for 3D rendering.

2 Graphics Performance

In a standard digital cluster application, a screen inside a vehicle shows various information such as speed, tire rotations per minute, fuel percentage, tire pressure, engine faults, trip information, and more. The intent is to have modern graphics run inside a vehicle and display various system critical information. To run such rich graphical content, graphics performance is one of the most critical criteria for a digital cluster system.

The AM62x includes a 3D GPU core, the AXE-1-16M[™], from Imagination Technologies. The 3D GPU core has the capability to draw eye-catching graphics inside a vehicle display. Figure 2-1 demonstrates how a GPU is used in a typical digital cluster application. There are various images for gauges, needles and backgrounds which are stored in memory. The GPU must read various images from memory and combine all the images to show critical statistics about the vehicle. In Figure 2-1, a cluster dashboard is shown using the GPU.

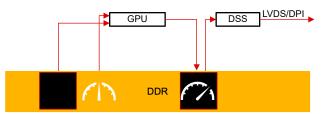


Figure 2-1. Representative GPU Rendering

In the use case shown in Figure 2-1, the GPU is used to perform the following operations:

- 1. Read multiple images for the left and right dials.
- 2. Read multiple images for the left and right needle.
- 3. Scale images based on the output resolution.
- 4. Rotate or transform the needles based on the acceleration or deceleration of the vehicle.
- 5. Composite all components into a final image.

Once the GPU writes the final image to memory, the display controller reads the image and sends the image on a screen that is attached to the processor. On the AM62x, this use case is implemented a summary of the images is provided in Table 2-1.

Table 2-1. Image Resolution Size Used by GPU for Rendering Cluster Output

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Input or Output	Resolution (Width × Height)	Pixel Format
Standard Gauge PNG	609 × 520	
Standard Needle PNG	682 × 683	ARGB8888
Display Framebuffer	1920 × 1080	

Based on the resolutions in Table 2-1, only 16% of the GPU compute power is utilized and the GPU is able to draw at 60 FPS. Many cluster applications have a strict requirement on updating the needles and dials at 60 FPS. The required performance is achieved with the AM62x processor.

The performance numbers from Table 2-1 are measured using the PVRTune tool from Imagination Technologies. The PVRTune tool is useful for capturing all the necessary GPU statistics while the GPU is being utilized. The PVRTune data for the AM62x cluster example is shown in Figure 2-2.

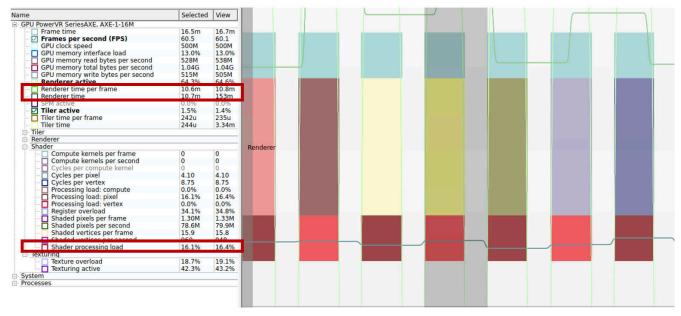


Figure 2-2. Resource Utilization From PVRTune

Various counters are displayed on the left side of Figure 2-2. The counters measure information such as FPS, GPU clock speed, total memory bandwidth consumed every frame, shader core utilized, and more. In the captured statistics, the GPU render time per frame is 10.6 ms and shader processing load is 16.1%. Based on the percentage load, there are still margins available for the GPU to render additional 3D scenes, such as navigation or media player. In most cases, designers prefer to select GPUs with higher processing power but depending on the use case or end-application such processing power is not even required. In summary, the AM62x processor can have less GFLOPS in comparison to other processors but has enough compute power to drive digital cluster applications.

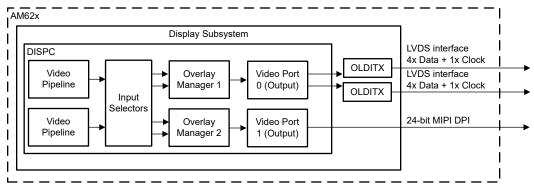
In addition to running a custom OpenGL[®] ES[®] test, a Kanzi[®] Performance Analyzer (KPA) is also run on the AM62x platform. KPA is designed by Rightware[®] and the objective of KPA is to run a set of demanding tests based on automotive use cases. Upon running the tests, KPA outputs insightful reports and analysis for a given platform. The report generates a score that various original equipment manufacturers (OEMs) and Tier 1 suppliers can use to compare performance of the SoC. The AM62x score for the Fast Cluster KPA test, is provided in Table 2-2. In addition to the KPA, Altia[®] designed a more realistic digital cluster demonstration that runs on AM62x and the GPU renders 3D content at 60 FPS.

Test	Resolution (Width × Height)	Score	
Fast Cluster	1920 × 1080	244	



3 DSS Features

In addition to a GPU, the AM62x SoC also has a display subsystem (DSS). Figure 3-1 shows an overview of the DSS.





The key features of the DSS are:

- 1. Video Pipeline and Video Lite Pipeline:
 - a. Two independent input pipelines
 - b. Supports various RGB and YUV input formats
 - c. Color space conversion from YUV to RGB
 - d. Upscaling and downscaling (Video Lite Pipeline does not support scaling)
- 2. Overlay Manager 1 and 2:
 - a. Ability to perform composition of the two input pipelines
 - b. Support for alpha blending
- 3. Video Port 0 and 1:
 - a. Supports gamma correction, color space rotation, and RGB or YUV output
- 4. Dual display support and capability of driving 1920 × 1200 display at 60 FPS.
 - a. Display 1: OLDITX can support native dual link LVDS panels, and Table 3-1 summarizes the various modes panels that can be connect with the DSS
 - b. Display 2: Native RGB24 or DPI-based TDT panels

within the Region of Interest (ROI) area.

Table 3-1. OLDI Supported Modes						
# of Modes	LVDS Link Mode	Link_1 (4 data + 1 clock)	Link_2 (4 data + 1 clock)	Description	Supported	
1	Single Link Mode - One Stream	165 MHz, wuxga (1920 × 1200 at 60 FPS)	Unused	One video stream	Yes	
2 Single Link Mode - One Unused Stream		Unused	165 MHz, wuxga (1920 × 1200 at 60 FPS)	One video stream	Yes	
		165 MHz, wuxga (1920 × 1200 at 60 FPS)	165 MHz, wuxga (1920 × 1200 at 60 FPS)	One stream duplicated in two links	Yes	
4	Dual Link Mode	85 MHz, wuxga (1920 × 1200 at 60 FPS)		One video stream over	Yes	
		Odd pixels	Even pixels two links			
5	Single Link Mode - Two Stream (Distinct)	165 MHz, wuxga (1920 × 1200 at 60 FPS)	165 MHz, wuxga (1920 × 1200 at 60 FPS)	Two independent video streams	No	

Table 3-1 OLDI Supported Modes

For safety critical system applications, the DSS supports the safety features shown in Table 3-2 in the hardware.

Table 3-2. Safety Features in DSS Hardware				
Feature Description				
Data correctness check	Verifies that the intended data is shown correctly on the display.			
Freeze frame detection	Provides a notification of a possible frame freeze when there is no change in the display frame over a multiple frame periods.			

These features are implemented by collecting signatures from user-defined regions within each pipeline output frame and the final display output frame, and comparing them to reference signatures provided by the user (software) and or to previously saved signatures. The signature from each region is generated using a multiple input signature register (MISR) module. The 32-bit MISR module generates a unique signature for all pixel data

4 Relevance of Functional Safety for Automotive Cluster Tell-tale Applications

Auto manufacturers use the digital instrument cluster to display safety critical information using audio or visual alerts. To tie the safety criticality of an application to a certain ASIL safety integrity level, following the ISO 26262 standard, OEMs have to perform HARA (Hazard Analysis and Risk Assessment) where the various malfunctions leading to system hazards and the associated risk is analyzed. Performing this analysis and assessment leads to understanding safety goals linked to the application. The safety goals considered for the cluster tell-tales are related to avoiding unreasonable risk due to unintended activation of tell-tales, due to faulty tell-tales being displayed or due to absence of tell-tale notification when the display of the information is needed. Based on severity, exposure and controllability of the hazards, cluster tell-tale applications typically target ASIL-B safety integrity levels, following the ISO 26262 standards, shown in Table 4-1.

Standard	ASIL	PMHF	SPFM	LFM
ISO 26262	A	< 1000 FIT	N/A	N/A
	В	< 100 FIT	≥ 90%	≥ 60%
	С	< 100 FIT	≥ 97%	≥ 80%
	D	< 10 FIT	≥ 99%	≥ 90%

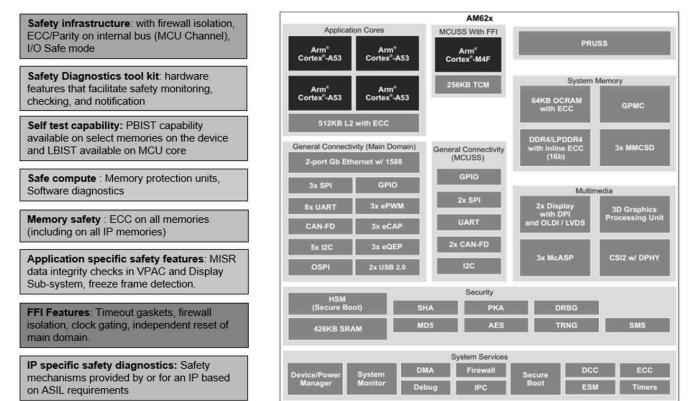
Table 4-1. Required Targets for ASIL Performance	Table 4-1	I. Required	Targets for	ASIL	Performance
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5 Safety Features on TI Sitara[™] AM62x Processor

To target ASIL-B automotive applications, AM62x offers several on-chip diagnostic features, including freedom from interference features. Figure 5-1 shows the various safety features present on the device. More details on the device safety features and diagnostics, systematic safety development process and recommendations of software diagnostic mechanisms are available in the device safety manual.





Note

Assumptions of Use When Using the AM62x

The AM62x is developed as Safety Element Out of Context following ISO 26262-10. Assumptions of Use (AoU) are therefore needed to place requirements on external components such as external power supply, voltage monitoring device and responsibilities on the system integrator. A comprehensive list of all AoU are available in the device safety manual.

6 Application-specific Task Partitioning and Safety Concept for Tell-tales

Tell-tales are the warning lights or indicators on the digital cluster that are crucial for the safety of the vehicle. Tell-tales can be used to convey different types of information from failure, such as low oil level, high engine temperature, and low tire pressure, to information like brake lights and turn signals. As tell-tales are safety critical, there are two main methods in which tell-tale displays are supported in AM62x, either hardware- or software-based.

The hardware-based method for supporting tell-tale displays in the AM62x uses the Safety Island Cortex[®] M4F to directly run the hardware tell-tale signs driver. Figure 6-1 shows this hardware-based method for tell-tale display.

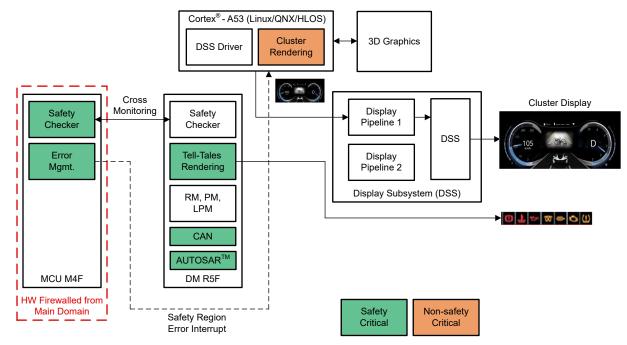


Figure 6-1. Hardware-based Tell-tale Rendering

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The software-based method is to have the tell-tales supported in software with the tell-tales directly overlayed on the main cluster display. Figure 6-2 shows a high-level partitioning of the various functions within a software tell-tale cluster application (without GPU rendering).

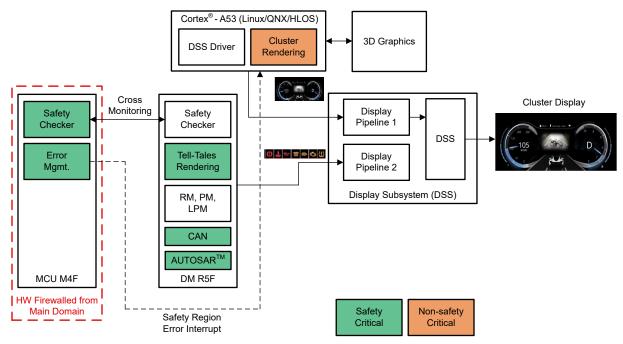


Figure 6-2. Software-based Tell-tale Rendering

The Device Manager (DM) R5F performs tell-tale rendering along with the Display Subsystem (DSS) driver that renders data to an independent display pipeline in the DSS. Primary display cluster data is rendered by the A53 cores through another DSS pipeline. The DM R5 also executes the AUTOSAR[®] and CAN stacks.

The MCU domain, which has Freedom from Interference (FFI) from the rest of the device, executes the safety cross-monitoring of the tell-tale reference signature that is loaded by DM R5F. MCU M4F checks that MISR reference signature is loaded correctly by R5 into the DSS. Additional checks include the MISR reference signature and calculated MISR comparison. Program sequence monitoring of the M4F core and DM R5 core must be performed to protect safety core execution from random faults.

Software diagnostics and hardware diagnostics for each IP within the data flow, provide fault detection and reporting within the required fault-tolerant time interval (FTTI). Fault indications in terms of events or interrupts are routed to the error signal monitor (ESM) on the device, which provides configurable low-priority and high-priority interrupts to the safety core. Software running on MCU M4F can then take necessary action based on these interrupts. Another feature of the ESM is the safety error signal, which is routed to the error pin of the device. This error pin can be used by an external monitoring device to detect if the AM62x is in an unresponsive state and if intervention is required to bring the system to a safe state. For example, resetting the AM62x device or disabling downstream actuators.

FFI features that isolate the MCU domain from the main domain aid in restricting accesses to the MCU domain and performing functions of different safety integrity on the device. Mixed criticalilty can also be further extended to the main domain with the use of firewalls.

6.1 Common Cause Failures

The MCU domain and main domain of the AM62x are powered using a common power source and common clock. The main domain can be reset independently from the MCU domain. An MCU domain reset results in an entire device reset. There are several on-chip diagnostics to aid in detection of common cause failures from clock, power, and reset. Dual clock comparators, on-chip oscillator clock detection, internal Power OK (POK) monitors, and temperature monitors along with thermal sensors are examples of such diagnostics. The safety concept also relies on external monitoring such as a windowed watchdog for detection of common cause failures on the device.



7 TI's Functional Safety Offerings

The AM62x is targeting safety certification with ASIL-B and SIL-2 random fault capability or ASIL-D and SIL-3 systematic capability. The safety manual, FMEDA, and safety analysis reports are available under NDA. The SDL (Software Diagnostic Library) is provided as part of the TI SDK for configuring and using the hardware diagnostic IP on the device.

8 Summary

This application note describes how an entry-level cluster can be implemented on an AM62x processor. The three main features in the AM62 that enable this application are an optimized GPU and corresponding Display Subsystem, support for Functional Safety features, and ARM[®] cores for running HLOS like Linux[®] and QNX[®].

9 References

- Texas Instruments, Enabling Low Power Embedded Systems With AM62x Processors, technical article
- Altia, Altia Code Generation Solutions for Texas Instruments AM62x Sitara™, website
- Rightware, Rightware Releases Kanzi Performance Analyzer, blog

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