## Standards **Protect Your BLDC Motor Drive with Cycle-by-cycle Current Limit Control – Part 2**



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Welcome back! If you missed part 1 of this series, I discussed the necessity of cycle-by-cycle over current protection in BLDC motor drives and how to sense the motor winding current. In part 2, I will discuss on how to implement the cycle-by-cycle over current protection by sensing the DC bus current and using an ultra-low power microcontroller.

TI's ultra-low power MSP430F5132 microcontroller helps to control the motor-winding current on a PWM cycleby-cycle basis without any software interrupt intervention.

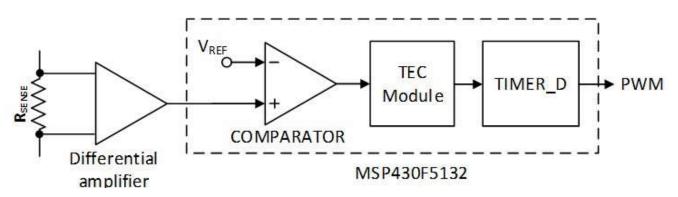


Figure 1-1. Cycle-by-cycle Current-limit Implementation Using a Differential Amplifier and the MSP430F5132 MCU

You can configure the high-bandwidth precision OPA374 as a single-ended differential amplifier to amplify the voltage drop across the sense resistor, R<sub>SENSE</sub>, connected in the DC bus return path

The MSP430F5132 MCU has an integrated comparator and timer event control (TEC) module that you can configure to implement the current limit. The comparator compares the analog voltages at the noninverting (+) and inverting (–) input terminals. If the noninverting terminal is more positive than the inverting terminal, the comparator output, CBOUT, is high.

You can use the output of the comparator with or without internal filtering. When setting the control bit, CBF, in the MCU, the output is filtered with an on-chip resistor-capacitor (RC) filter. You can adjust the delay of the filter in four different steps, which allows you to optimize the comparator's response time. The output filter will suppress noise spikes, which can avoid false switching at the output of the comparator. The output filter can also reduce errors associated with comparator output oscillation when the voltage difference across the input terminals is small. The comparator features a high-precision reference voltage; to obtain different voltage references, configure the CBRSEL bit in the CBCTL2 register. The reference voltages available are 1.5V, 2.0V and 2.5V.

The TEC module is the interface between the timer modules and the external events. The TEC and Timer\_D modules are connected through internal signals. The TEC module contains the control registers to configure the routing between TEC and timer modules. The TEC module also has the enable register bits, interrupt enable and interrupt flags for external event inputs. On receiving the external fault or clear signals, the TEC module controls the timer output and thus the PWM signal.

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The COMPB module and TEC module are used together for cycle-by-cycle current-limit protection. You must externally route the output of the comparator, CBOUT, to the TECxFLT1 external fault event pin of the TEC module, as shown in Figure 1-2, for current-limit protection.

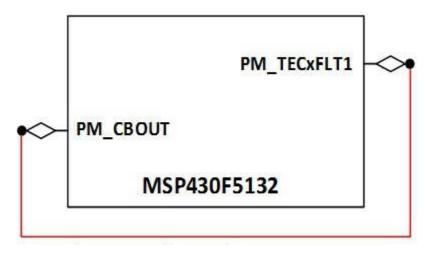


Figure 1-2. CBOUT Routed Externally to the TECxFLT1 External Fault Event Pin

The operation of the TEC module is shown in Figure 1-3. Whenever the current-sense differential amplifier output exceeds the voltage reference of the comparator, the output CBOUT and hence TECxFLT1 goes high, which initiates an event in the TEC module. The TEC module is programmed to disable the Timer\_D output PWM during such an event. The Timer\_D is configured in SET/RESET mode so that during the external event, the Timer\_D resets and causes the PWM output pin to go low. This programmed function means that CBOUT goes high when the motor hits an overcurrent condition and can disable the Timer\_D output (as Figure 1-3 shows) if CBOUT is connected to TECxFLT input pin. Figure 1-3 shows that the PWM turns off immediately when the comparator output goes high. When CBOUT goes low, the Timer\_D output is then allowed to resume normal operation.

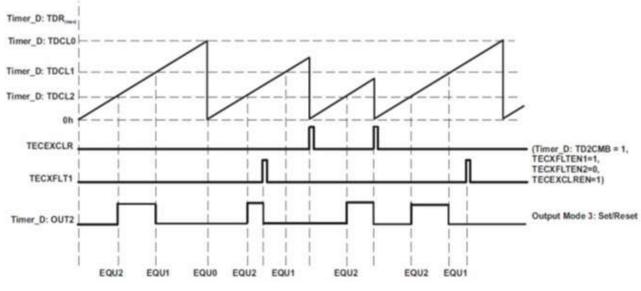


Figure 1-3. External Input Events Resetting Timer\_D Output

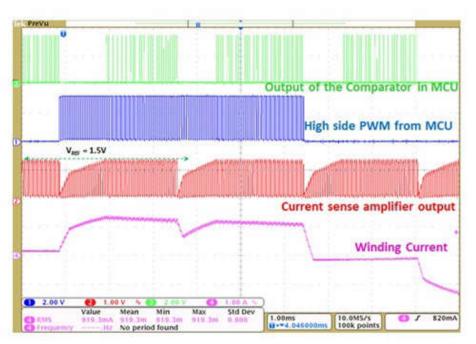
Figure 1-4 shows the current-limit operation when the comparator reference,  $V_{REF}$ , is set at 1.5V, with a 60m $\Omega$  sense resistor ( $R_{SENSE}$ ) and a differential amplifier gain of 20.



The set over current limit ( $I_{OC \ LIMIT}$ ) can be calculated using Equation 1.

Overcurrent limit, I<sub>OC LIMIT</sub> = V<sub>REF</sub>/(R<sub>SENSE</sub>\*amplifier gain)

At V<sub>REF</sub> = 1.5V, I<sub>OC\_LIMIT</sub> = 1.5 / (0.06\*20) = 1.25A

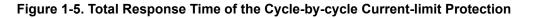


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Figure 1-4. Cycle-by-cycle Current Limit Using the MSP430F5132 MCU Hardware Features

Figure 1-5 shows the response time of the comparator and TEC module with an external trip signal connected to the comparator input. The test results show that the time between the comparator input going more than 1.2V (to ensure the worst case, I considered a lower voltage compared to the 1.5V reference to calculate the response time) and the PWM shutdown is approximately 356ns. Therefore, the total response time of the current-limit action is less than 1µs. Figure 1-6 shows the response time from the comparator output going high to a PWM shutdown event, which is approximately 100ns. The test results show that the hardware features in the MCU ensures a very fast cycle-by-cycle current limit action and hence protects the motor drive.

Comparator threshold voltage, $V_{MST} = 1.5$
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Response time of the fault module in MSP430 ≈ 100m

## Figure 1-6. The Response Time from When the Comparator Goes High to the PWM Shutdown

Thank you for reading this blog series. I hope you found it helpful in understanding necessity of cycle-by-cycle over current protection in BLDC motor drives and how we can implement this method of over current protection using an ultra-low power microcontroller.

## **Additional Resources**

- Check out our TI Designs 230-V, 250-W, High Efficiency BLDC Motor Drive w/DC Bus Voltage Ripple Compensation Reference Design.
- To view more solutions to enable your motor control design, visit www.ti.com/motor.
- Learn more about the MSP430F5132 MCU.
- Read the application report "Sensored 3-Phase BLDC Motor Control Using MSP430" for more advice.

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