

Basic Design Considerations for Backplanes

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ABSTRACT

This application report describes design issues relevant to the parallel backplanes typically used in the wireless, datacom, telecom, and networking markets. Designing a high-performance backplane is extremely complex, because issues such as distributed capacitance, stub lengths, noise margin, rise time (slew rate), flight time, and propagation delay must be defined and optimized to achieve good signal integrity along the transmission line.

This application report uses a GTLP backplane driver to study the effects of these factors in an actual backplane application. Guidelines that enable the design engineer to successfully design a high-performance backplane with GTLP or other single-ended open-drain devices, such as BTL, are provided.

This application report is a revision of the original *Basic Design Considerations for Backplanes*, literature number SZZA016, published June 1999. The theory text was rewritten to make it clearer, and the theory-to-practice section was added, based on work done with the GTLP evaluation module (EVM).

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Introduction

Since the beginning, most equipment makers have used parallel-backplane architectures to deliver large amounts of data across one shared bus. The parallel backplane provides a physical and electrical interconnect between various modules in a system. Each module in the backplane communicates with other modules through the backplane bus. Typically, this bus is driven by a backplane transceiver, primarily as the point-of-contact between backplane cards. The basic backplane is a parallel data-transfer topology used in a multipoint transfer scheme. For example, the TDM bus in a wireless base-station unit operates in a multipoint fashion, with high-speed data communicating between different regions across the backplane.

With the expansion of the internet and wireless/telecom infrastructures, new end-equipment markets have emerged that deliver faster data, integrated voice and data, or a little of both, and need higher performance backplanes. The constant pressure to increase bandwidth requires design engineers to choose between higher performance, more expensive backplane-optimized transceivers to maximize the frequency, increase the bit width using older technology, or a combination of these goals. This application report addresses some of the basic design issues encountered in higher performance backplanes. The effects of distributed capacitance on termination resistance and flight time are examined and the various effects of stubs and connectors are discussed.

Backplane Design Topology – Point-to-Point vs Multipoint

Figure 1 is an example of a simple point-to-point data transfer. A driving device at point A drives a 51-Ω transmission line. A termination resistor (R_{TT}) that matches the line impedance is placed at point B, along with a receiving device. All calculated values for the termination resistance are ideal. The designer must use actual values that best match, or are lower than, calculated values. In this example, the transmitter is an open-drain device that pulls the line low when turned on, but requires the termination resistor to pull the line high when turned off.

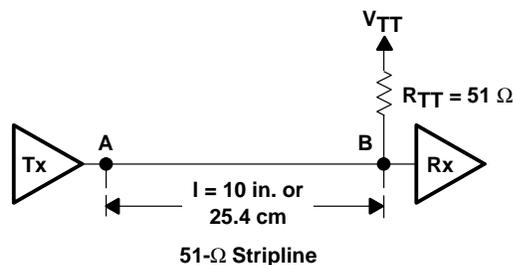


Figure 1. Point-to-Point Application

When the output transistor drives the line low, a constant dc current flows from the termination voltage, V_{TT} , to ground. Too small a termination resistance can damage the driver due to excessive currents. Assuming $V_{TT} = 1.5 \text{ V}$, $V_{OL} = 0.4 \text{ V}$, and $R_{TT} = 51 \Omega$, the constant dc current is about 21.6 mA ($I_{OL(max)} = (V_{TT} - V_{OL})/R_{TT}$). However, this current increases linearly with V_{TT} and should not exceed the recommended current rating of the output driver.

In this, and the following multipoint example, the transmission line is assumed to be a stripline trace that is 10 in. (25.4 cm) long with a natural impedance (Z_0) of 51 Ω, which corresponds to a characteristic capacitance (C_0) of 3.5 pF/in. (138 pF/m).

The propagation delay (t_{pd}) is the time delay through the transmission line per unit length and is a function of the natural impedance and characteristic capacitance.

Use equation 1 to calculate propagation delay (t_{pd}).

$$t_{pd} = Z_o \times C_o \quad (1)$$

In this example, $t_{pd} = 51 \, \Omega \times 3.5 \, \text{pF/in.}$ (138 pF/m) yields 178.5 ps/in. (7038 ps/m or 7.03 ns/m).

The total flight time (t_{flight}) is the time required for the signal to propagate down the transmission line from driver to receiver (time from A to B) and is a function of t_{pd} and length of the line.

Use equation 2 to calculate t_{flight} .

$$\begin{aligned} t_{flight} &= t_{pd} \times \text{length of line} = 178.5 \, \text{ps/in.} \times 10 \, \text{in.} \\ &\quad \text{or } 7.03 \, \text{ns/m} \times 0.254 \, \text{m} \\ &= 1.784 \, \text{ns} \end{aligned} \quad (2)$$

In Figure 2, the point-to-point configuration has been changed to a multipoint layout. Eleven transceivers are placed on the 10-in. transmission line, with 1-in. spacing (d) between each transceiver. One transceiver is configured as a transmitter (Tx); the other ten are configured as receivers (Rx). In a multipoint system, any position can assume the role of transmitter, with the remaining positions acting as receivers, as shown by the transceiver symbol. The 51- Ω stripline transmission line must be terminated at both ends because the transceiver at either end could be the driver. The optimum termination resistance (R_{TT}) for the multipoint system is less than the natural transmission-line impedance of 51 Ω , due to the effects of distributed capacitance. Procedures to calculate the optimum R_{TT} and the effects of mismatched R_{TT} on signal integrity are the main focus of this application report.

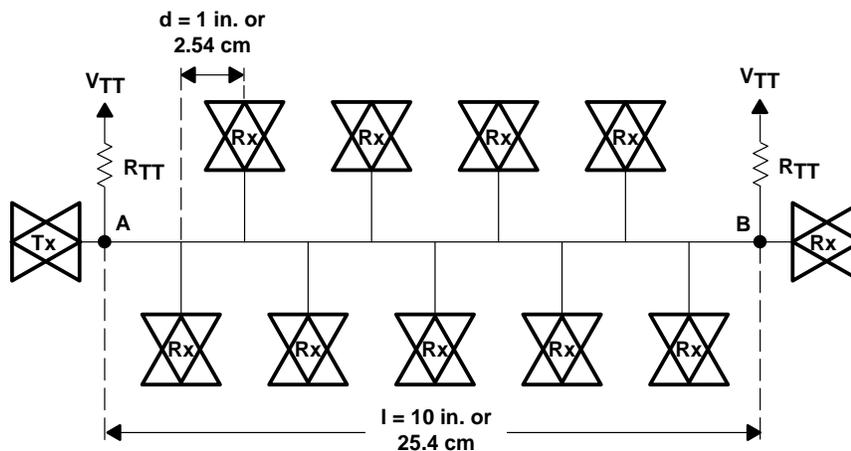


Figure 2. Multipoint Application

Distributed Capacitance

Figure 3 is a simplified version of Figure 2, where an equivalent capacitive load (12-pF capacitor) replaces the receivers. It is assumed that the spacing between card slots is within the rise and fall time of the driver signal, and that all slots are populated with cards.

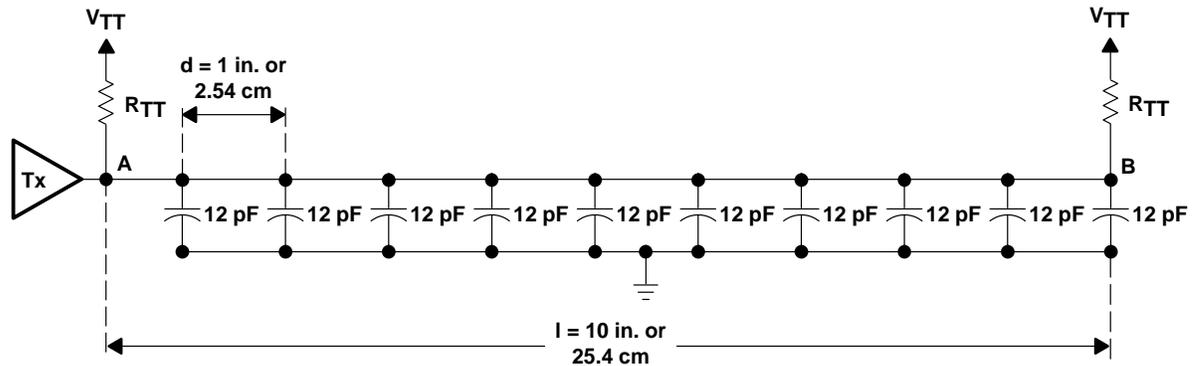


Figure 3. Equivalent Multipoint Application

Total capacitance (C_t) is calculated by summing all the capacitive components associated with the transceiver and the connection to the backplane. Figure 4 shows a typical connection scheme between the backplane stripline and the driving/receiving device on the daughter card. Point C is the connection to the backplane stripline, while point D is the connection to a transceiver integrated circuit. Total capacitance (C_t) at point C is the sum of each of the elements in the connection chain. Total capacitance then can be distributed uniformly across the transmission line at an equivalent rate of capacitance per inch (C_d).

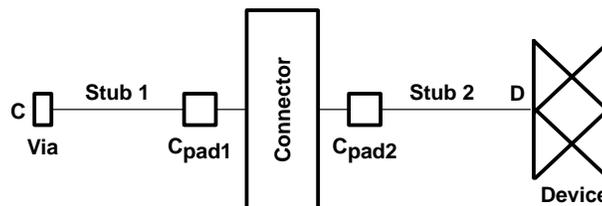


Figure 4. Typical Connection Scheme to Backplane

The stub lines (stub 1 and stub 2) are 51- Ω microstrip construction with a characteristic capacitance of 2.6 pF/in. (102 pF/m). The connection via connects stub 1 to the backplane trace and has an approximate capacitance of 0.5 pF. Stub 1 is 1/16 in. in length and is connected on the other end to the surface-mount pad for the connector (C_{pad1}), which has a capacitance of approximately 0.5 pF.

The HSPICE model for the connector used in this example has a connector capacitance (C_{con}) of 0.74 pF. C_{pad2} has the same value as C_{pad1} and is the surface-mount pad for the connector on the daughter-card side that connects the connector to the daughter-card stub (stub 2). Stub 2 is 1 in. long and is attached to the other end of the transceiver input/output pin, which has a typical capacitance (C_{iO}) of 7 pF.

Two different printed circuit board (PCB) transmission lines are shown in Figure 5. Basically, microstrip resides on the top of the PCB, whereas the stripline is imbedded within the PCB layers. A microstrip is faster due to the less inherent capacitance, but a stripline exhibits better signal integrity because the reference planes shield the conductor from damaging EMI fields. Other performance differences are discussed later in this application report.

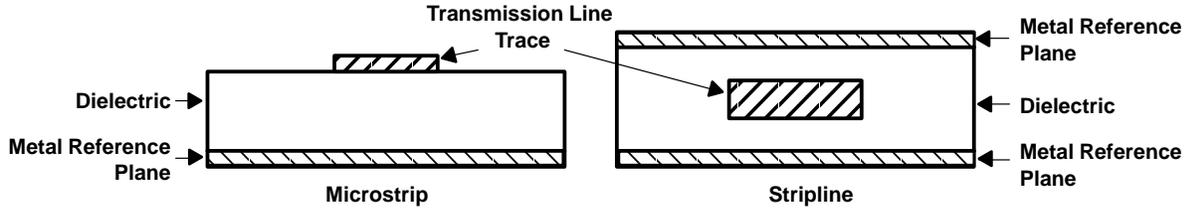


Figure 5. Typical PCB Transmission Lines

The capacitance of the via, pads, and stubs can be calculated based on the dimensions and type of traces. www.ultracad.com provides an excellent capacitance calculator with background information. The C_{io} of the transceiver and the connector capacitance can be obtained from the manufacturer's specification sheet.

The capacitance in this chain is summed as:

$$C_t = C_{via} + C_{stub1} + C_{cpad1} + C_{con} + C_{cpad2} + C_{stub2} + C_{io} \quad (3)$$

$$C_t = 12 \text{ pF}$$

Where:

$$\begin{aligned} C_{via} &= \text{capacitance of via} = 0.5 \text{ pF} \\ C_{stub1} &= \text{capacitance of stub 1} = 0.0625 \times 2.6 = 0.16 \text{ pF} \\ C_{cpad1} &= \text{capacitance of } C_{pad1} = C_{pad2} = 0.5 \text{ pF} \\ C_{cpad2} &= \text{capacitance of } C_{pad2} = C_{pad2} = 0.5 \text{ pF} \\ C_{stub2} &= \text{capacitance of stub 2} = 1 \times 2.6 = 2.6 \text{ pF} \\ C_{con} &= \text{capacitance of connector} = 0.74 \text{ pF} \\ C_{io} &= \text{input/output capacitance of device} = 7 \text{ pF} \end{aligned}$$

The total capacitance (C_t) of 12 pF is placed at point C on the backplane for every transceiver. More than half of C_t is the transceiver typical input/output pin capacitance. This is why backplane designers require low-capacitive ICs to optimize performance in high-frequency backplanes.

With all the slots filled, the 10-in. transmission line has 11 12-pF capacitors distributed at 1-in. intervals. The distributed capacitance (C_d) affects both the propagation delay and the characteristic impedance of the stripline transmission line, which results in a new effective impedance, $Z_{o(\text{eff})}$, and a new effective propagation delay, $t_{pd(\text{eff})}$. The distributed capacitance equals the total capacitance divided by the separation, or $C_d = C_t/d$. In our example, $C_d = 12 \text{ pF}/1 \text{ in.}$ or 12 pF/in. (472 pF/m). The new effective impedance, $Z_{o(\text{eff})}$, and effective propagation delay, $t_{pd(\text{eff})}$, can be calculated using equations 4 and 5.

$$Z_{o(\text{eff})} = \frac{Z_o}{\sqrt{1 + \frac{C_d}{C_o}}} \quad (4)$$

$$t_{pd(\text{eff})} = t_{pd} \sqrt{1 + \frac{C_d}{C_o}} \quad (5)$$

Figures 6 and 7 show the effects of the term $\sqrt{1 + (C_d/C_o)}$ on Z_o and t_{pd} by plotting the normalized effective impedance and t_{pd} in terms of distributed capacitance divided by the characteristic capacitance, C_d/C_o .

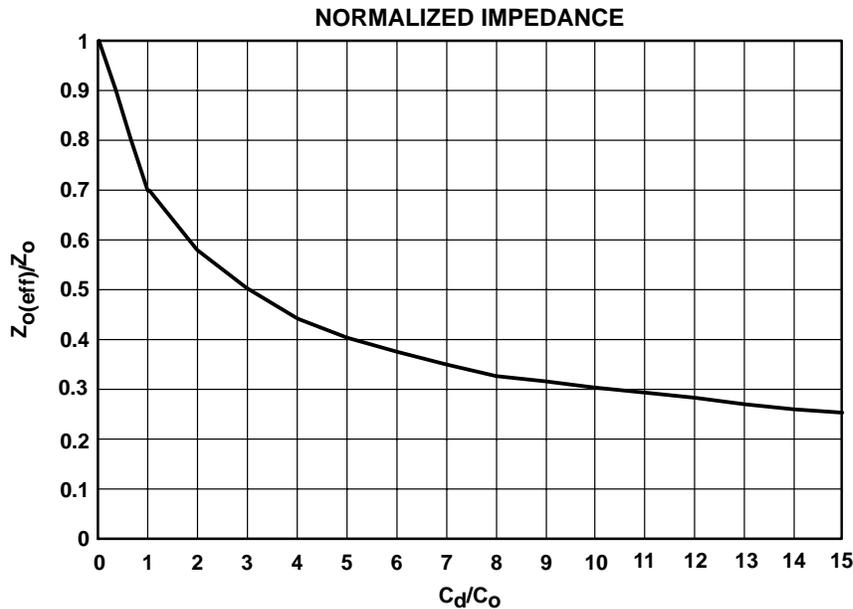


Figure 6. Effective Impedance vs C_d/C_o

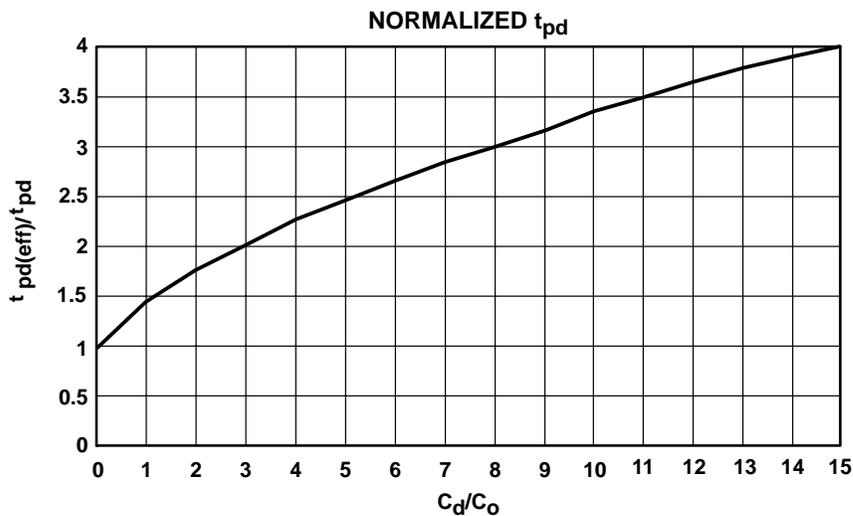


Figure 7. Effective t_{pd} vs C_d/C_o

An easy-to-follow calculation using Figures 6 and 7 is based on a 50- Ω line (Z_o) with a t_{pd} of 180 ps/in. (7.09 ns/m) used in a system where the C_d/C_o ratio is 3. From Figure 6, the C_d/C_o of 3 yields an effective impedance of 0.5 times the characteristic impedance, or $Z_{o(eff)} = 0.5 \times 50 = 25 \Omega$. Figure 7 shows that for the same C_d/C_o ratio of 3, the transmission-line effective propagation delay has doubled and $t_{pd(eff)} = 2 \times 180 = 360$ ps/in. (14.18 ns/m).

In a previous example (capacitors in Figure 3), $C_d = 12$ pF/in. (472 pF/m) and $C_o = 3.5$ pF/in. (138 pF/m) make the C_d/C_o ratio = 3.43 and the term $\sqrt{1 + (C_d/C_o)} = 2.1$. Figures 6 and 7 reflect the changes in the effective values of the transmission line to be 0.48 times the normal impedance and 2.1 times the normal propagation delay.

Another way to calculate the new effective impedance and propagation delay is to use equations 4 and 5 instead of Figures 6 and 7.

The value of the effective impedance is:

$$Z_{o(\text{eff})} = \frac{Z_o}{\sqrt{1 + \frac{C_d}{C_o}}} = \frac{51}{2.1} = 24.2 \Omega \quad (6)$$

The value of the effective t_{pd} is:

$$t_{pd(\text{eff})} = t_{pd} \sqrt{1 + \frac{C_d}{C_o}} = 178.5(2.1) = 375.6 \text{ ps/in.} \quad (7)$$

Using equation 2, the new flight time between points A and B in Figure 3 is:

$$t_{\text{flight}} = t_{pd} \times \text{length of line} = 375.6 \text{ ps/in.} \times 10 \text{ in.} = 3.76 \text{ ns} \quad (8)$$

Note that the propagation delay was 1.785 ns in the point-to-point example.

As discussed previously, the optimum termination resistance is equal to the effective impedance, $Z_{o(\text{eff})}$, of the system so, in this case, the optimum termination resistance, R_{TT} , is the same as $Z_{o(\text{eff})}$ which is 24.2 Ω . The optimum termination resistance ensures incident-wave switching without undershoot or overshoot.

Figure 8 shows the effect on signal integrity in different-terminated conditions. R_{TT} should be less than or equal to $Z_{o(\text{eff})}$ for incident-wave switching, optimum signal integrity, and the best upper noise margin.

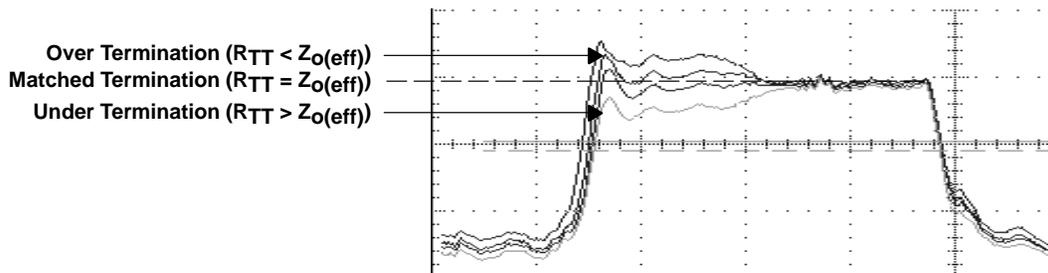


Figure 8. Termination Resistance vs $Z_{o(\text{eff})}$

Equation 9 provides all parameters needed to calculate an optimum termination value:

$$R_{TT} = \frac{Z_o}{\sqrt{1 + \frac{C_d}{C_o}}} = \frac{Z_o}{\sqrt{1 + \frac{C_{\text{via}} + C_{\text{stub1}} + C_{\text{cpad1}} + C_{\text{con}} + C_{\text{cpad2}} + C_{\text{stub2}} + C_{\text{io}}}{dC_o}}} \quad (9)$$

Optimum Termination Simulation

Figure 9 is the result of HSPICE simulation of the circuit in Figure 3, with $51\ \Omega$ used for the pullup terminations (R_{TT}) to 1.5 V. Figure 3 did not show the L-C-R values inherent in transmission lines, but they are included in the HSPICE simulations. The transmitter (driver) is a high-drive GTLP device operating at 50-MHz clock frequency. Because the device is operating in the latched mode, the data signal shown is only one-half clock frequency, or 25 MHz.

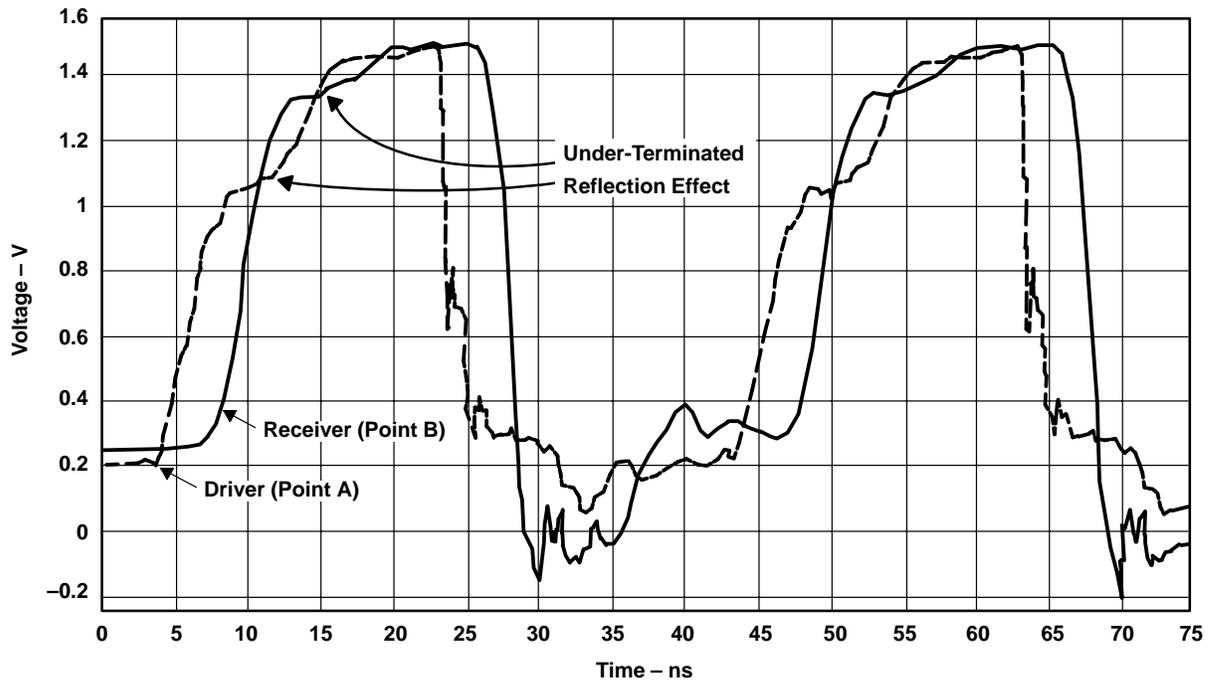


Figure 9. Mismatched Line Termination

One signal in Figure 9 is the driver output at point A of the fully loaded transmission line, and the other signal is the receiver input at point B of the fully loaded transmission line that is farthest from the driver. The effects of the reflections due to termination mismatch can be seen clearly.

Figure 10 shows the same waveforms when the termination resistors are changed to the calculated value of $24.2\ \Omega$. The improvement in signal integrity is due to matching the termination resistors to the loaded impedance of the stripline transmission line. The delay between the two signals is measured at the 1-V threshold level for the GTLP device.

The HSPICE simulation produces the same flight time from point A to point B, as calculated previously.

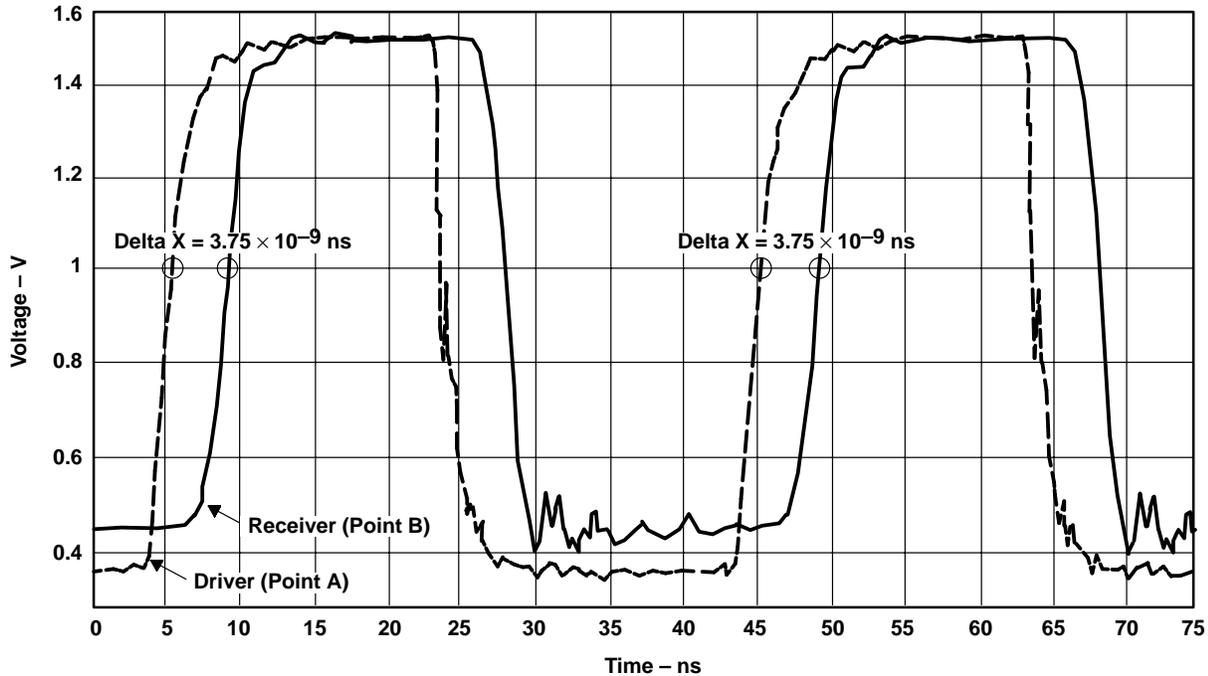


Figure 10. Matched Line Termination

Stripline vs Microstrip Tradeoffs

Table 1 demonstrates the effects of distributed capacitance on various microstrip and stripline transmission lines used in backplane designs. ϵ_r is the dielectric constant and depends on the material used in the multilayer-backplane printed circuit board. For Table 1 discussion purposes, the distributed capacitance is fixed at 12 pF/in. Results in the table differ if the distributed capacitance value is changed. The highlighted stripline Z_0 50- Ω line is closest to the multipoint distributed-capacitance example discussed previously.

Table 1. Comparison of Backplane Lines (Loaded Backplane, $C_D = 12$ pF/in.)

TYPE LINE $\epsilon_r = 4.5$	C_0 (pF/in.)	Z_0 (Ω)	$Z_0(\text{eff})$ (Ω)	t_{pd} (ps/in.)	$t_{pd}(\text{eff})$ (ps/in.)
Microstrip	1	140	38.8	140	505
Microstrip	2	70	26.5	140	370
Microstrip	2.8	50	21.7	140	322
Microstrip	4.67	30	15.9	140	265
Stripline	1.29	140	43.6	180	578
Stripline	2.58	70	29.5	180	428
Stripline	3.6	50	24	180	375
Stripline	6	30	17.3	180	312

Using the same impedance (Z_0) in a loaded backplane, microstrip lines (on the surface of the backplane board) have a faster effective t_{pd} than striplines (embedded in the backplane board), but the microstrips have a lower effective impedance than the stripline. This lower effective impedance requires a lower termination resistance to properly terminate the backplane. The designer must balance the required signal propagation time with the driver capabilities when deciding which type of line to use and what characteristic impedance to choose. In general, it is recommended that stripline be used for the backplane transmission line and microstrip be used for the daughter-card stub lines, because stripline has better signal integrity and does not require a lower termination resistance. The microstrip adds less to the total capacitive load for each card, is faster, and is easier to implement on the daughter card.

Backplane DC Effects

Figure 11 is the dc-equivalent circuit of Figure 2 when the driver is turned on and is in the low state. The driver is replaced by its on resistance (R_{device}), and the transmission line is replaced by its dc resistance (R_{line}). The current (I_3) is the sum of currents I_1 and I_2 . When the output is low at the driver, V_{OL1} is the product of R_{device} and I_3 . The voltage (V_{OL2}) is the low level seen at the receiver farthest from the driver and is equal to $V_{TT} - (R_{TT} \times I_2)$.

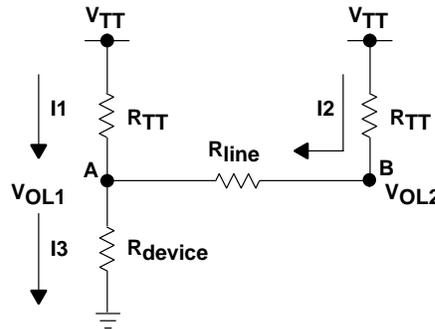


Figure 11. DC Equivalent of Single Backplane Line

In our example, $R_{TT} = 24.2 \Omega$, $R_{line} = 2.2 \Omega$, and $V_{TT} = 1.5 \text{ V}$. The basic equation starts with:

$$I_3 = V_{TT} / [R_{TT} // (R_{TT} + R_{line}) + R_{device}]$$

Where:

$R_{TT} // (R_{TT} + R_{line})$ is the parallel resistance of the upper branch.

From this expression, the following equations can be derived:

$$V_{OL1} = \frac{(V_{TT})(R_{device})(2R_{TT} + R_{line})}{[(R_{TT})(R_{TT} + R_{line}) + (R_{device})(2R_{TT} + R_{line})]} \quad (10)$$

$$V_{OL2} = V_{OL1} + \frac{(R_{line})(V_{TT} - V_{OL1})}{R_{TT} + R_{line}} \quad (11)$$

$$R_{device} = \frac{(R_{TT})(V_{OL1})(R_{TT} + R_{line})}{(V_{TT} - V_{OL1})(2R_{TT} + R_{line})} \quad (12)$$

For the device model in Figure 10, the R_{device} value was estimated to be 4Ω . Using equation 10, $V_{OL1} = 0.361 \text{ V}$ and, using equation 11, $V_{OL2} = 0.456 \text{ V}$, which matches well with the results observed in Figure 10.

The dc analysis can help provide the designer with best-case low-level voltage (V_{OL1}) and worst-case (V_{OL2}) signal levels expected at the receivers on a backplane when the termination resistance has been determined.

The V_{OL} levels affect the noise margins at all receivers as shown in Figure 10. The signal at point B is at the last receiver at the end of a 10-in.-long transmission line. The low level of this signal is higher than that of point A (less lower noise margin). Smaller values of R_{TT} or longer backplanes (higher values of R_{line}) will reduce point-B noise margin even more. The drive capability (characterized by R_{device}) of the transmitter also will affect the waveforms V_{OL} .

Effect of Changing Stub Length on Backplane Signal Characteristics

The effects of changing stub length are most noticeable in the stub associated with the transceiver that drives the signal and, to a lesser extent, on the stubs at the transceivers that are receiving the signal. These effects are in two categories:

- Flight time – The longer the stub, the longer it takes for a signal to propagate through it, and results in increased flight time from the driver to the backplane line (stub delay).
- Rise time [also known as slew rate (V/ns)] – One of the interesting effects of the stub is the faster rise time observed at the driver circuit as stub Z_0 , or stub length, increases.

The inductance of the stub and connector form an L-C-R network between the driver and the load (backplane). Figure 12 shows a simplified equivalent circuit.

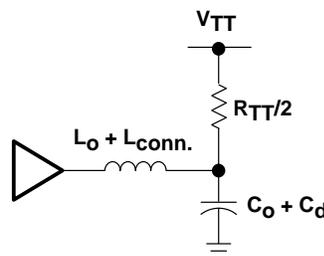


Figure 12. Thevenin Equivalent of Load

The longer the stub length, or the higher the stub Z_0 , the larger is the inductance seen by the driver [the sum of the stub line inductance (L_O) and the connector inductance ($L_{conn.}$)] and, thus, the faster the rise time of the driving waveform. The faster rise time causes increased ringback (increased reflections) and worsens the signal integrity of the system. Therefore, it is best to use a low stub Z_0 and keep the length as short as possible, preferably less than 1 in.

The following analyses are based on HSPICE simulations of the backplane model (see Figure 2). Figure 13 shows the results of simulation data taken on rise time when only the stub Z_0 was changed. The termination resistance used in the calculation was also changed with each new value of stub impedance, because this changes the effective characteristic impedance on the backplane. S1 is the rise time at the driver measured from 20% to 80% steady-state low and high levels. S2 is the rise time measured at the beginning of the backplane. S3 is the measured rise time when the signal leaves the backplane at the last receiver slot. S4 is the measured rise time at the last receiver.

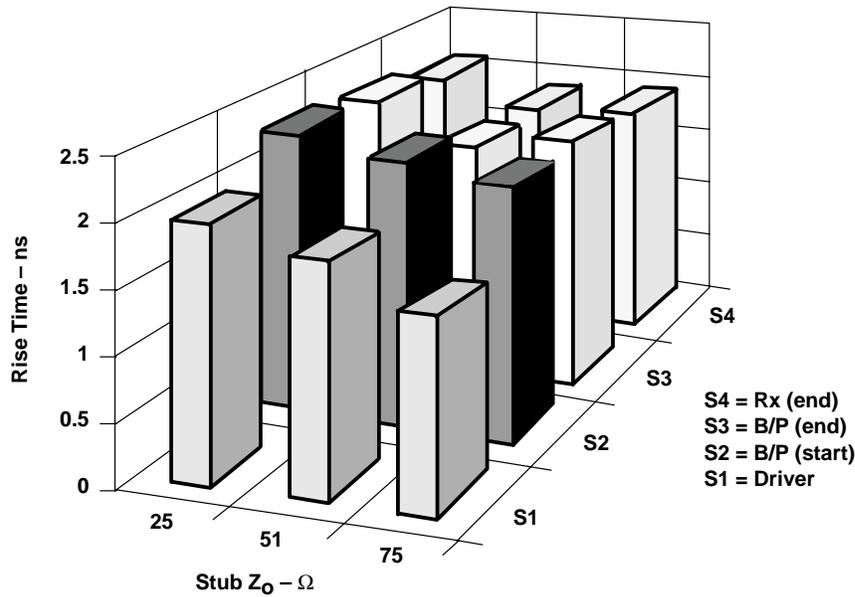


Figure 13. Rise Time vs Stub Z_0 at Various Points on the Backplane

The higher-impedance stubs (higher inductance) produce a faster driver rise time (higher slew rate) and, therefore, faster rise times at all points along the backplane. This shows that system slew rate is dependent on both the device slew rate and the stub impedance. If the system rings, a lower stub Z_0 can alleviate the problem, because it would slow the rise time to a more manageable value. Figure 14 shows the effects of stub length on stub delay and driver rise time. Stub impedance is fixed at 51 Ω , and only stub lengths and R_{TT} were changed.

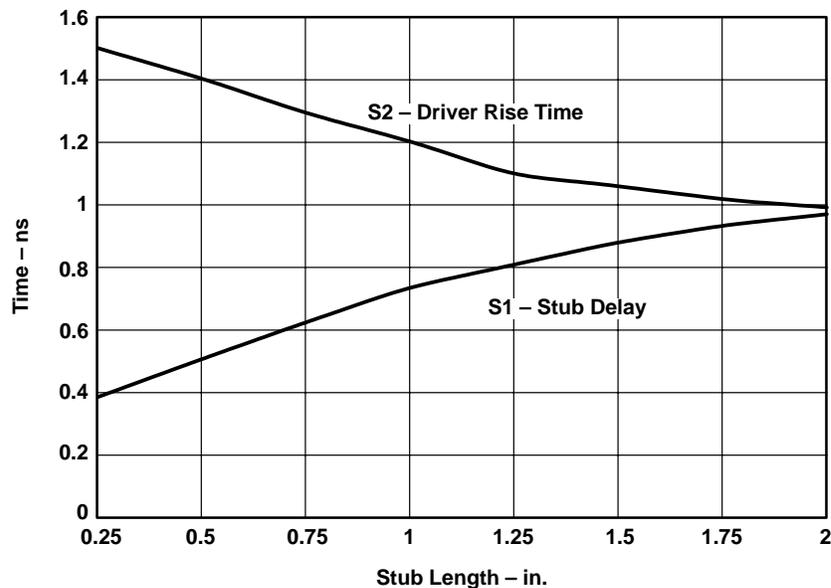


Figure 14. Effects of Stub Length on Stub Delay and Rise Time

The termination was calculated for each stub length, using equation 9. The capacitance of the different stub lengths changed the distributed capacitance on the backplane. Figure 14 shows that as stub length increases, stub delay increases and driver rise time (slew rate) decreases.

Figure 15 shows the effect of stub length on termination resistance, and demonstrates that longer stub lengths result in a lower optimum R_{TT} when everything else is held constant.

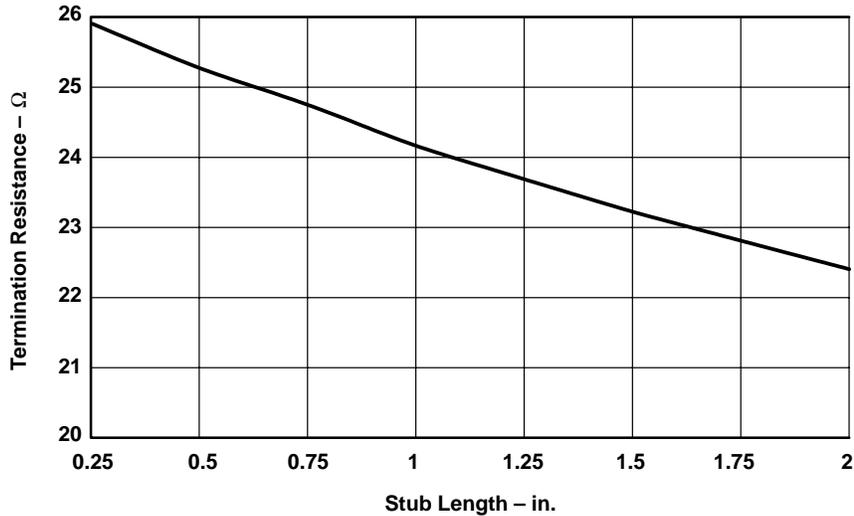


Figure 15. Effect of Stub Length on Termination Resistance at S1

In all three cases, minimum stub lengths are desired because they result in the best stub propagation delay, rise time, and termination resistance. A stub-length design goal is 1 in., or less.

Figure 16 shows the results of simulations of flight time in a backplane. Various stub impedances with fixed stub lengths of 1 in., coupled with a fixed 25- Ω or 50- Ω connector and termination resistors fixed at 24 Ω , or calculated based on stub impedance, were modeled into the system shown in Figure 2. The driver's rise time (20% to 80%) was set to 1.5 ns. The measurements show the delay between the driver and the receiver located at opposite ends of the 10-in. transmission line.

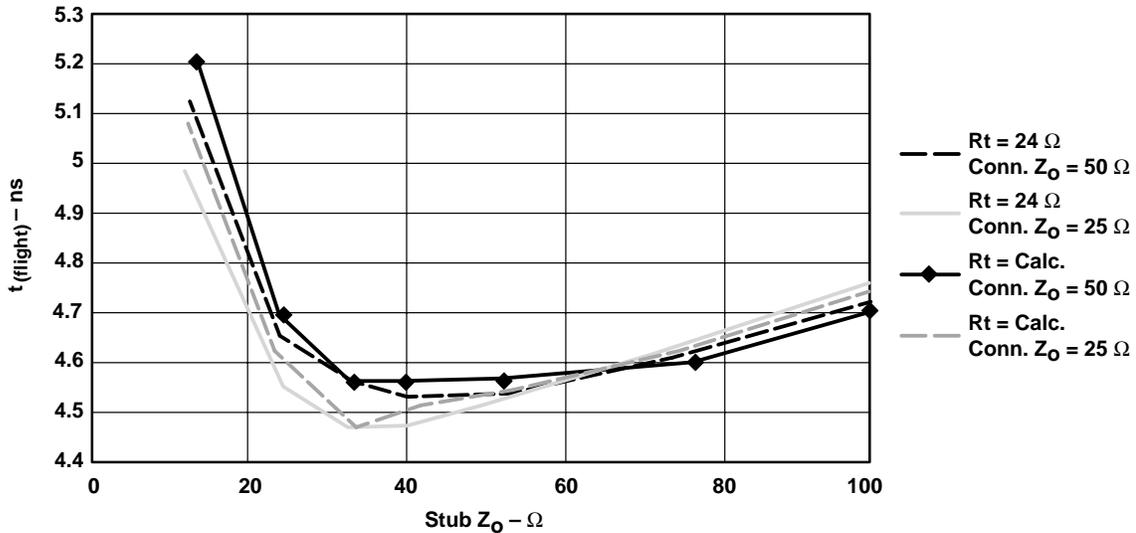


Figure 16. System Flight Time vs Stub Impedance

Figure 16 indicates that a range of stub impedances produces a minimum system flight time. Lowest flight times are observed between 35 Ω and 50 Ω .

Higher-impedance stubs have a larger value of inductance that results in gradually longer stub delays and flight times.

Lower-impedance stubs have larger values of capacitance that result in increased distributed capacitance on the backplane. This increases the effective propagation delay and also increases flight time much more dramatically than the higher-impedance stubs.

A design goal would be to have the stub Z_0 between 35 Ω and 65 Ω for optimum performance.

Distributed Capacitance – Theory to Practice

The effect of distributed capacitance was observed in the GTLP evaluation module (EVM). The EVM is a 17.9-in., 48-bit, 20-slot stripline backplane with slot-to-slot spacing (slot pitch) of 0.94 in. and removable terminations. The backplane is divided into six groups, with each group having eight traces. Group 1 is 20 slots long, while group 6 is only 2 slots long. The other groups are 16, 12, 8, and 4 slots long. Group 1, bit 1 was used for this theory-to-practice evaluation. The natural trace impedance (Z_0) was planned to be 55 Ω for all, but two traces in group 1, including the trace used for this experiment, were higher due to missing reference planes between them. Available termination-resistor values are 25 Ω , 33 Ω , 38 Ω , and 50 Ω . Data was taken at 23-MHz, 50-MHz, and 87-MHz clock frequencies. The SN74GTLP1655 high-drive transceiver was used for this experiment and was operated in the latched mode where data frequency is one-half of clock frequency. The data waveforms are shown. The driver in all cases is in slot 1; the waveforms shown were obtained directly from the backplane connector pin of the receiver slot under test.

Fully Loaded Backplane

Figure 17 clearly shows the effect of the different termination resistors on signal integrity in the fully loaded EVM. All waveforms show incident-wave switching, with upper noise margin gained with lower termination-resistor values. The 50- Ω termination value is unacceptable. The 43.5-MHz and 11.5-MHz data waveforms are included for comparison.

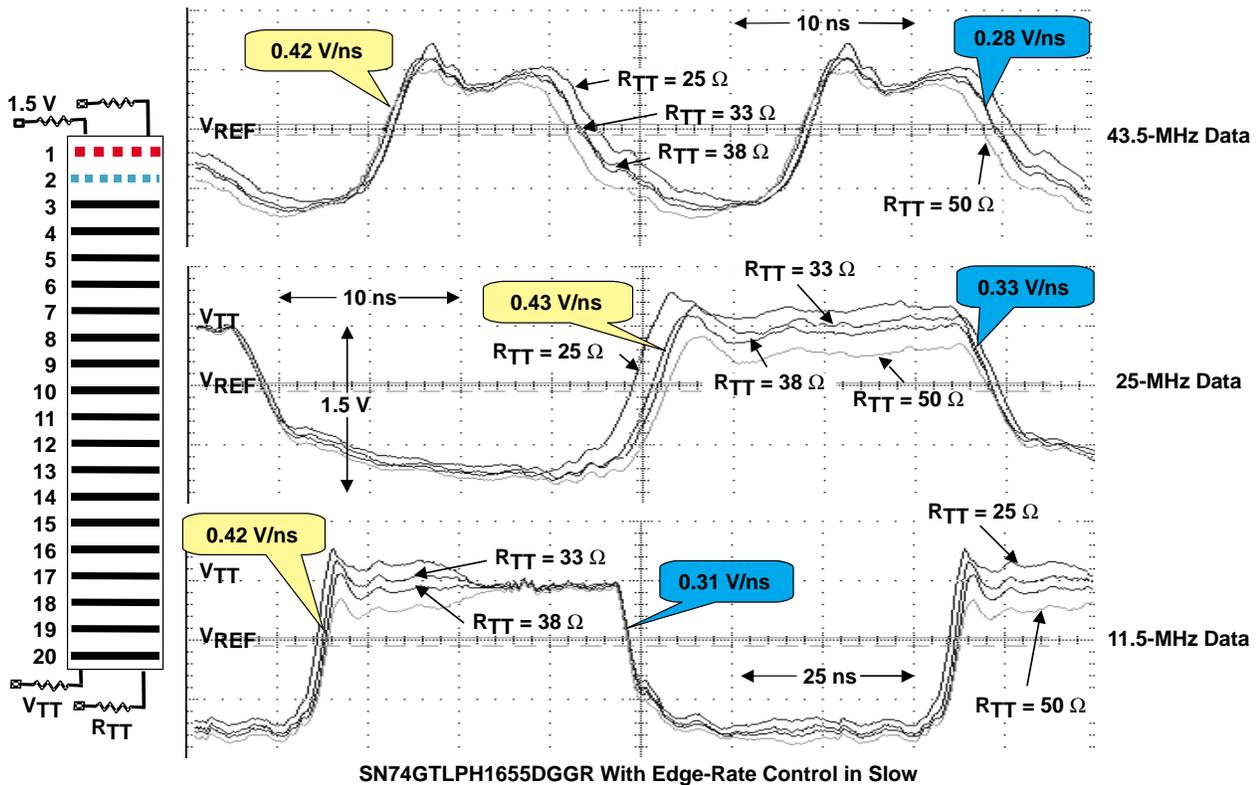


Figure 17. Fully Loaded Backplane vs R_{TT} (Driver in Slot 1, Receiver in Slot 2)

The V_{OH} voltages at both 25-MHz and 43.5-MHz data rates never converge to the termination voltage of 1.5 V as with 11.5-MHz data. The reason is that the reflections have not had enough time to settle, which typically takes one round trip on the bus.

Additionally, slew rates of the optimum termination line are included for the rising and falling edges. Typical TTL slew rates in lumped loads are from 1 V/ns to 1.4 V/ns, depending on the capacitive load. The significantly slower GTLP edge rates result in a larger device t_{pd} , but allow for higher system frequencies because limited ringing improves signal integrity. The observed slew rate should increase as the load is reduced.

C_t can be calculated using the information known about the EVM and the observed $Z_{o(\text{eff})}$. Assuming stripline construction with $Z_o = 95 \Omega$ and $C_o = 2.40 \text{ pF/in.}$, solve for C_d using equation 9 and assuming that the optimum $R_{TT} = Z_{o(\text{eff})} = 35 \Omega$. An interpolated R_{TT} value of 35Ω was chosen because it produces the best incident-wave switching performance. Then, solve for C_t by multiplying C_d by the separation between two transceivers which, in this case, is 0.94 in.

$$C_d = \left(\frac{Z_o^2}{R_{TT}^2} - 1 \right) \times C_o = \left(\frac{95^2}{35^2} - 1 \right) \times 2.40 \text{ pF/in.} = 15.28 \text{ pF/in.} \quad (13)$$

$$C_t = C_d \times d = 15.28 \text{ pF/in.} \times 0.94 \text{ in.} = 14.36 \text{ pF} \quad (14)$$

Using C_d and C_o , the effective t_{pd} and flight time can be calculated.

t_{pd} for our EVM transmission line with a Z_o of $95 \Omega = 230 \text{ ps/in.}$

$$t_{pd(\text{eff})} = t_{pd} \times \sqrt{1 + (C_d/C_o)} = 230 \text{ ps/in.} \times 2.71 = 624.3 \text{ ps/in.}$$

The total distance traveled from slot 2 to the termination load is:

$$18 \text{ slots} \times 0.94 \text{ in.} + \text{termination stub length of } 1 \text{ in.} = 17.92 \text{ in.}$$

Therefore, flight time is $17.92 \text{ in.} \times 624.3 \text{ ps/in.}$, or 11.2 ns.

Round-trip flight time from slot 2 to the load, and back, is 22.4 ns.

The observed settling time is 20.8 ns.

Lightly Loaded Backplane

Figure 18 clearly shows the effect of the different termination resistors on signal integrity when every other card is removed from the EVM and the distributed capacitive load is reduced by a factor of two. There is still some capacitive loading (about 0.7 pF) at the empty slot position, but the majority is removed with the female connector, stub, and device C_{i0} .

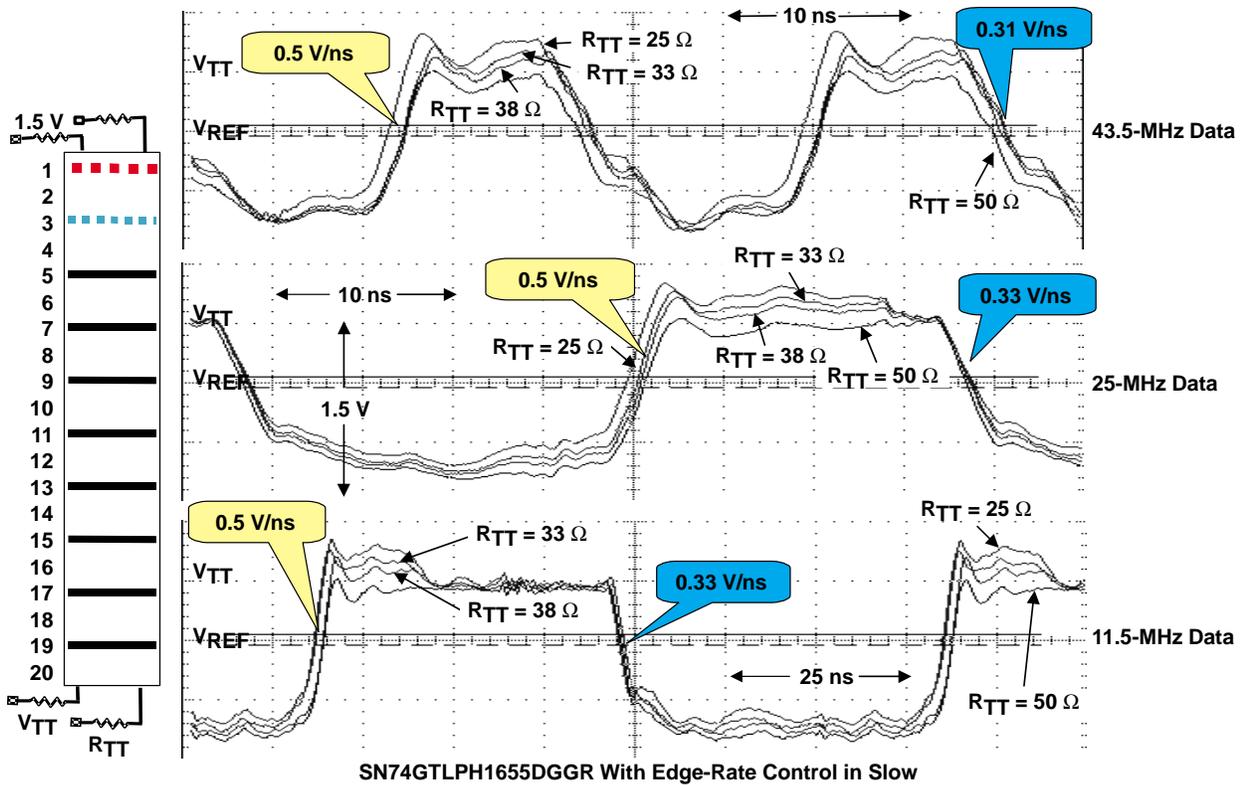


Figure 18. Lightly Loaded Backplane vs R_{TT} (Driver in Slot 1, Receiver in Slot 3)

All termination resistances again show incident-wave switching, with noise margin gained as the termination-resistor value is reduced, but all resistances are within acceptable noise-margin limits. This shows a very important point; reducing C_t by increasing slot spacing, reducing stub length, using devices with a lower C_{i0} , or a combination of all three reduces the loaded backplane capacitance, allowing a higher termination-resistor value to be used.

C_t can be calculated again, and should be the same value as obtained for the fully loaded case. Optimum R_{TT} , in this case, is 46 Ω (interpolated from Figure 18).

$$C_d = \left(\frac{Z_o^2}{R_{TT}^2} - 1 \right) \times C_o = \left(\frac{95^2}{46^2} - 1 \right) \times 2.40 \text{ pF/in.} = 7.84 \text{ pF/in.} \tag{15}$$

$$C_t = C_d \times d = 7.84 \text{ pF/in.} \times 1.88 \text{ in.} = 14.73 \text{ pF} \tag{16}$$

The fully loaded and lightly loaded C_t values agree closely, as expected.

$$t_{pd(eff)} = t_{pd} \times \sqrt{1 + (C_d/C_o)} = 230 \text{ ps/in.} \times 2.07 = 475.1 \text{ ps/in.}$$

Therefore, flight time is 16.98 in. (17 slots \times 0.94 in. + 1 in.) \times 475.1 ps/in. or 8.1 ns.

Round-trip flight time from slot 3 to the load, and back, is 16.2 ns.

The observed settling time is 15.5 ns.

Very Lightly Loaded Backplane

Figure 19 clearly shows the effect of the different termination resistors on signal integrity when every other three cards are removed from the EVM and the distributed capacitive load is reduced by a factor of four.

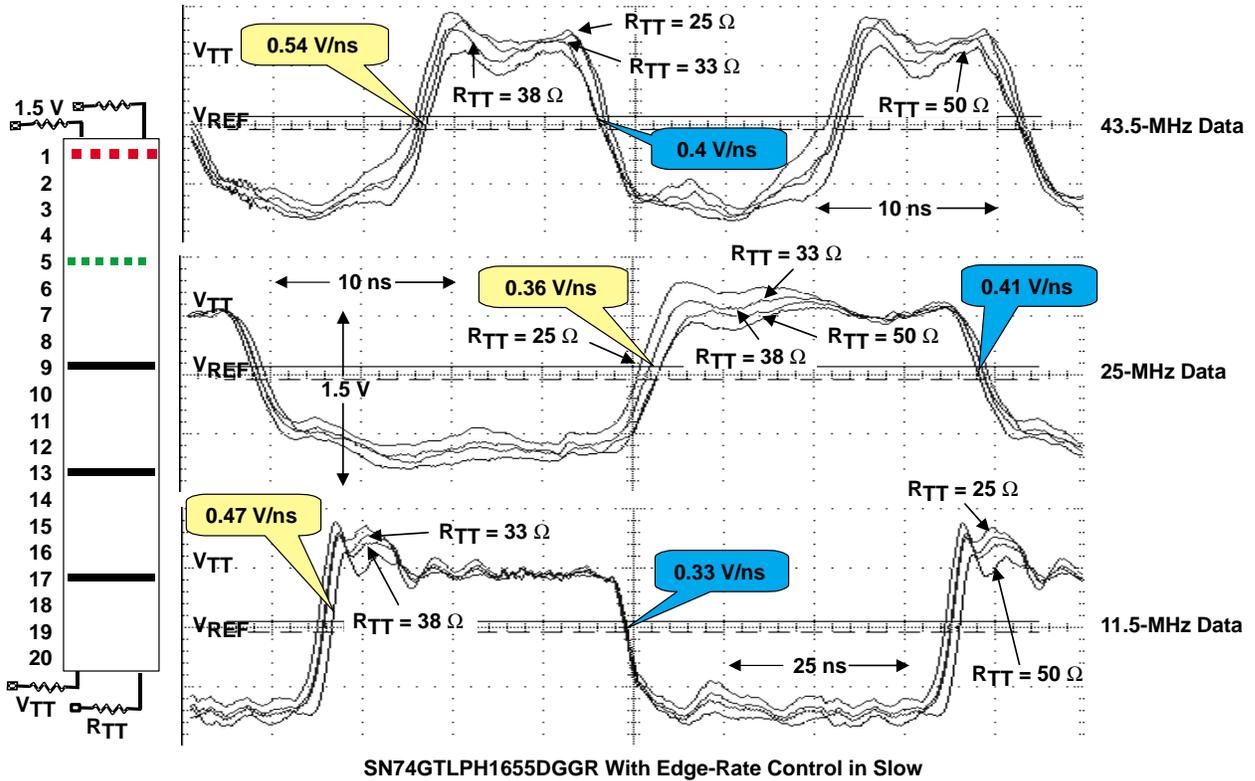


Figure 19. Very Lightly Loaded Backplane vs R_{TT} (Driver in Slot 1, Receiver in Slot 5)

C_t can be calculated and should be the same values as obtained in the other cases. Optimum R_{TT}, in this case, is 60 Ω (extrapolated from Figure 19).

$$C_d = \left(\frac{Z_o^2}{R_{TT}^2} - 1 \right) \times C_o = \left(\frac{95^2}{60^2} - 1 \right) \times 2.40 \text{ pF/in.} = 3.62 \text{ pF/in.} \quad (17)$$

$$C_t = C_d \times d = 3.62 \text{ pF/in.} \times 3.76 \text{ in.} = 13.6 \text{ pF} \quad (18)$$

In all cases, the C_t values agree closely (within ±5%).

$$t_{pd(\text{eff})} = t_{pd} \times \sqrt{1 + (C_d/C_o)} = 230 \text{ ps/in.} \times 1.58 = 364.3 \text{ ps/in.}$$

Therefore, flight time is 15.1 in. (15 slots × 0.94 in. + 1 in.) × 364.3 ps/in. or 5.5 ns.

Round-trip flight time from slot 5 to the load, and back, is 11.0 ns.

The observed settling time is about 10 ns. Some oscillations are evident to about 25 ns.

In all cases (i.e., fully, lightly, and very lightly loaded) observed vs calculated flight times are within 10%.

The total capacitance in all the above cases was calculated to be about 14 pF, based on the observed optimum R_{TT} . Analyzing each component in the capacitance chain on the daughter card is summed below, with the results close to observed and measured. The daughter-card construction use for the GTLP EVM is different from the original assumptions. The via and stub 1 add no capacitance to the line. Through-hole connectors, instead of surface mount, were used for increased reliability, but at the expense of additional capacitance. C_{cpad3} was added and is required to connect the device to stub 2.

$$C_t = C_{via} + C_{stub1} + C_{cpad1} + C_{con} + C_{cpad2} + C_{stub2} + C_{cpad3} + C_{io} \tag{19}$$

$$= 0 + 0 + 0.5 + 2.0 + 0.5 + 3.3 + 0.5 + 7 = 14.5 \text{ pF}$$

Where:

- C_{via} = capacitance of via = 0 pF
- C_{stub1} = capacitance of stub 1 = 0 pF
- C_{cpad1} = capacitance of C_{pad1} = 0.5 pF
- C_{cpad2} = capacitance of C_{pad2} = 0.5 pF
- C_{stub2} = capacitance of stub 2 = 1 in. \times 3.3 pF/in. = 3.3 pF
- C_{con} = capacitance of connector = 2.0 pF
- C_{cpad3} = capacitance of C_{pad3} = 0.3 pF
- C_{io} = typical input/output capacitance of device (SN74GTL1655) = 7 pF

The procedure to determine the actual backplane natural trace impedance (Z_o) was to measure the daughter-card C_t directly (13.8 pF). Then, flight time, with only slot 1 occupied, was measured and divided by backplane length to determine that t_{pd} unloaded was 230 ps/in. The same procedure was used in a fully loaded condition, and the resulting t_{pd} was 616 ps/in. Using the backplane calculator set to the new C_t , Z_o was adjusted to match the measured t_{pd} . The new Z_o was 96 Ω , $C_o = 2.4$ pF/in., and $Z_o(\text{eff}) = 36 \Omega$.

Table 2 provides the results of additional investigation using different equipment (i.e., TDR) on each of the eight traces in the 20-slot group (group 1) on the GTLP EVM. Z_o is calculated and is our best estimate. The backplane trace impedance with only the connector pins attached (i.e., all cards removed) (Z_o') and the backplane trace impedance in a fully loaded backplane (i.e., 20 cards inserted) (Z_o'') are measured. Group 1, bit 1, Z_o is closer to 91 Ω and, in the fully loaded case, the t_{pd} is 564 ps/in. vs our assumption of 624.3 ps/in. This makes round-trip flight time 20.2 ns, which is much closer to the observed time of 20.8 ns.

Table 2. GTLP EVM Group 1 Trace Impedance

GROUP 1 TRACE	D1	D2	D3	D4	D5	D6	D7	D8
Natural Trace Impedance								
Z_o (Ω)	91	47.5	47	47	48	47.5	83	47.5
t_{pd} (ps/in.)	165	140	138	139	141	148	147	142
C_o (pf/in.)	1.81	2.95	2.94	2.96	2.94	3.12	1.77	2.99
Trace Impedance With Only Connectors								
Z_o' (Ω)	62.7	37.5	37	36.3	37.1	37.9	58.5	36.8
t_{pd}' (ps/in.)	240	177	175	180	183	185	208	183
Trace Impedance Under Full Load								
Z_o'' (Ω)	26.6	17.7	17.9	17.5	17.9	18	24.8	17.7
t_{pd}'' (ps/in.)	564	377	362	373	377	390	493	382

Note the difference in the fully loaded trace impedance between trace D1/D7 and the other traces. Using the lower natural trace impedance offers the advantage of a smaller t_{pd} and shorter time of flight, but at the expense of terminating with a lower-value termination resistor and the subsequent increase in power consumption. Texas Instruments offers both medium-drive (50 mA) and high-drive (100 mA) GTLP devices to allow the designer to match the device with backplane loading. The termination resistor (R_{TT}) should match the fully loaded trace impedance (i.e., Z_0'') of the backplane for optimal signal integrity.

Table 3 provides the stackup used on the GTLP EVM backplane. Additional information on the GTLP EVM can be found in the *GTLP EVM User's Guide* (SCEA023).

Table 3. GTLP EVM Backplane Stackup

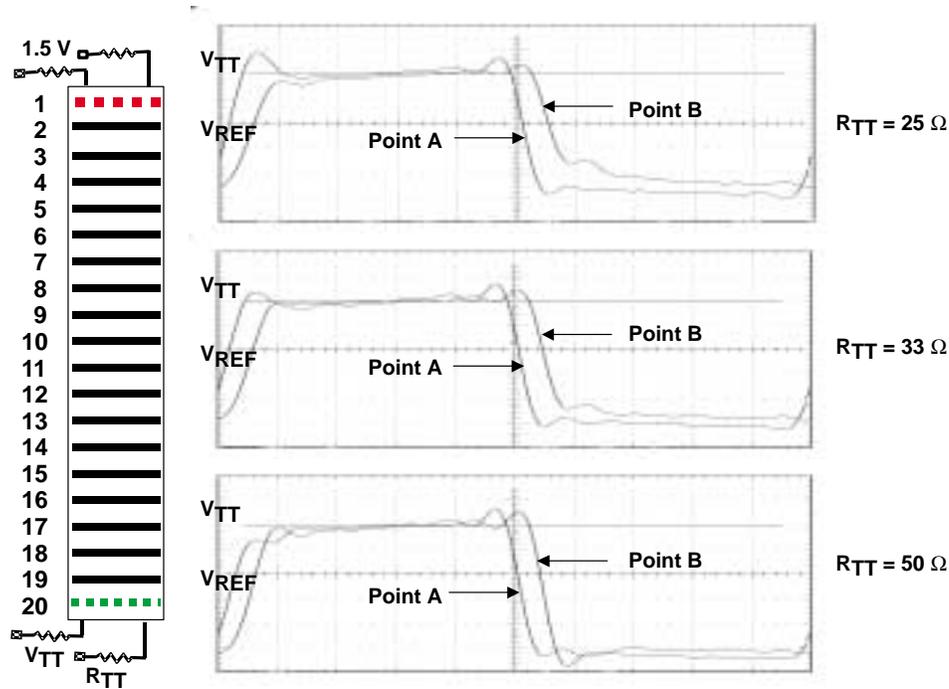
TRACE NAME	USE	LAYER	COPPER WEIGHT (oz)	PHYSICAL REPRESENTATION	DIELECTRIC HEIGHT (in.)	DIELECTRIC NAME
Top	Regulator power/ bypass capacitor/termination	1	0.5			
					0.004	B stage
Internal signal 2	Clock distribution/signal	2	1			
					0.004	Core
Ground plane	Ground plane	3	1			
					0.004	B stage
Internal signal 3	Data signal	4	1			
					0.058	Core
Internal signal 4	Data signal	5	1			
					0.004	B stage
VCC	VCC	6	1			
					0.004	Core
Internal signal 5	Data signal	7	1			
					0.004	B stage
Bottom	Termination	8	0.5			

High-drive (100 mA) devices, such as the SN74GTLP1655, can drive the transmission line down to $R_{TT} \approx 22 \Omega$, without exceeding the recommended maximum I_{OL} , while medium-drive (50 mA) GTLP devices can drive the transmission line down to $R_{TT} \approx 38 \Omega$. Both drives can be used with higher values of R_{TT} (i.e., 60Ω), if required. Medium-drive GTLP devices cost less, have a smaller pin count (fewer GND and V_{CC} pins), and have slightly less maximum B-port C_{iO} (medium drive is 9.5 pF vs 10.5 pF for high drive), so the designer must balance and optimize backplane construction with device capability to ensure optimum system signal integrity.

The driver card on the GTLP EVM used initial engineering samples of the SN74GTLP1655. All receiver cards used production SN74GTL1655 devices because they were more readily available and were operated only in the receive mode. The newer GTLP devices were designed specifically to drive transmission lines and have slower backplane-optimized slew rates for better signal integrity. GTL devices have faster edge rates and are better for point-to-point applications.

Backplane DC Effects – Theory to Practice

Figure 20 shows the dc effects previously described in the *Backplane DC Effects* section on a fully loaded backplane with waveforms plotted at different terminations. V_{OL} information is taken with an 8-MHz clock frequency (4-MHz data), which is the slowest crystal oscillator we had on hand, in order to eliminate as much ac switching effects from the V_{OL} measurement as possible. Each set of waveforms represents measurements taken at each end of the GTLP EVM (or points A and B as described in Figure 11). As expected, V_{OL} decreases as the termination voltage increases because the GTLP driver is able to drive the line lower with a higher resistance load.



SN74GTLPH1655 With Edge-Rate Control in Fast and Frequency = 100 MHz

Figure 20. Fully Loaded Backplane vs R_{TT} (Driver in Slot 1, Receiver in Slot 20)

Assuming the line resistance from one end of the GTLP EVM to the other (slot 2 to slot 20) to be about 2.7Ω , an on resistance of the SN74GTLPH1655 output driver to be 2.75Ω (measured value), and $V_{TT} = 1.5 \text{ V}$, and using equations 10 and 11, theoretical values vs actual test measurements were obtained (see Table 4). V_{TT} voltage source cause V_{OL} (and V_{OH}) to fluctuate; the difference in the two levels was plotted (not shown) and measured. This voltage difference was then compared to the calculated values, and the data shows that a very good correlation exists. Thus, validity of equations 10 and 11 is verified.

Table 4. Theoretical vs Actual V_{OL} Measurements

R_{TT} (Ω)	THEORETICAL VALUES			ACTUAL VALUES
	V_{OL} SLOT 2 (V)	V_{OL} SLOT 20 (V)	DIFFERENCE (mV)	DIFFERENCE (mV)
25	0.260	0.380	121	120
33	0.207	0.305	98	96
38	0.184	0.271	87	
50	0.145	0.215	69	72

Data from Table 4 also implies that there is a theoretical maximum length of a backplane. As the length increases, the V_{OL} difference increases and reaches a point where the highest V_{OL} value is within the predetermined noise margin allotted to the system by the designer.

Conclusion

Good backplane designs should follow the design rules in this application report and account for the capacitive loading effects on a backplane transmission line to obtain better signal integrity and achieve incident-wave switching. Minimizing the distributed capacitance on the backplane transmission line is desirable and can be accomplished by using transceiver devices with low C_{iO} , selecting connectors with low capacitance, using higher natural trace impedance (balanced against backplane time of flight), and by keeping stub lengths short.

The backplane integrated-circuit drive strength must be selected based on the fully loaded characteristic impedance of the backplane and should be able to maintain the minimum required V_{OL} levels along the entire length of the backplane without exceeding the recommended maximum low-level output current limitations.

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Glossary

C_{i0}	Input/output capacitance of the transceiver
C_o	Characteristic capacitance – capacitance per unit length of a transmission line in free space
GTL	Gunning transceiver logic– operates at signal levels of $V_{TT} = 1.2$ V, $V_{REF} = 0.8$ V, and $V_{OL} = 0.4$ V. GTL+ is a derivative of GTL that operates at higher noise-margin signal levels of $V_{TT} = 1.5$ V, $V_{REF} = 1$ V, and $V_{OL} = 0.55$ V, and moves V_{REF} from the normal ground-bounce area.
GTLP	Gunning transceiver logic plus – normally associated with slower edge-rate devices optimized for distributed loads that allow higher-frequency operation in heavily loaded backplane applications
L_o	Characteristic inductance – inductance per unit length of a transmission line in free space
R_{TT}	Termination resistance – resistance used to match the effective impedance of a transmission line in order to minimize reflections. $R_{TT} = Z_{o(eff)}$
$t_{(flight)}$	Flight time – time it takes a signal to propagate between two points on a transmission line. $t_{(flight)} = \text{length} \times t_{pd}$
t_{pd}	Propagation delay – delay per unit length of a signal traveling down a transmission line, expressed by the formula $t_{pd} = Z_o \times C_o$
Z_o	Characteristic impedance – impedance of a transmission line, as defined by $Z_o = \sqrt{L_o/C_o}$
$Z_{o(eff)}$	Effective impedance – impedance of a transmission line when external capacitance is added at fixed intervals along the line. $Z_{o(eff)} = \sqrt{L_o/(C_o + C_d)}$

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