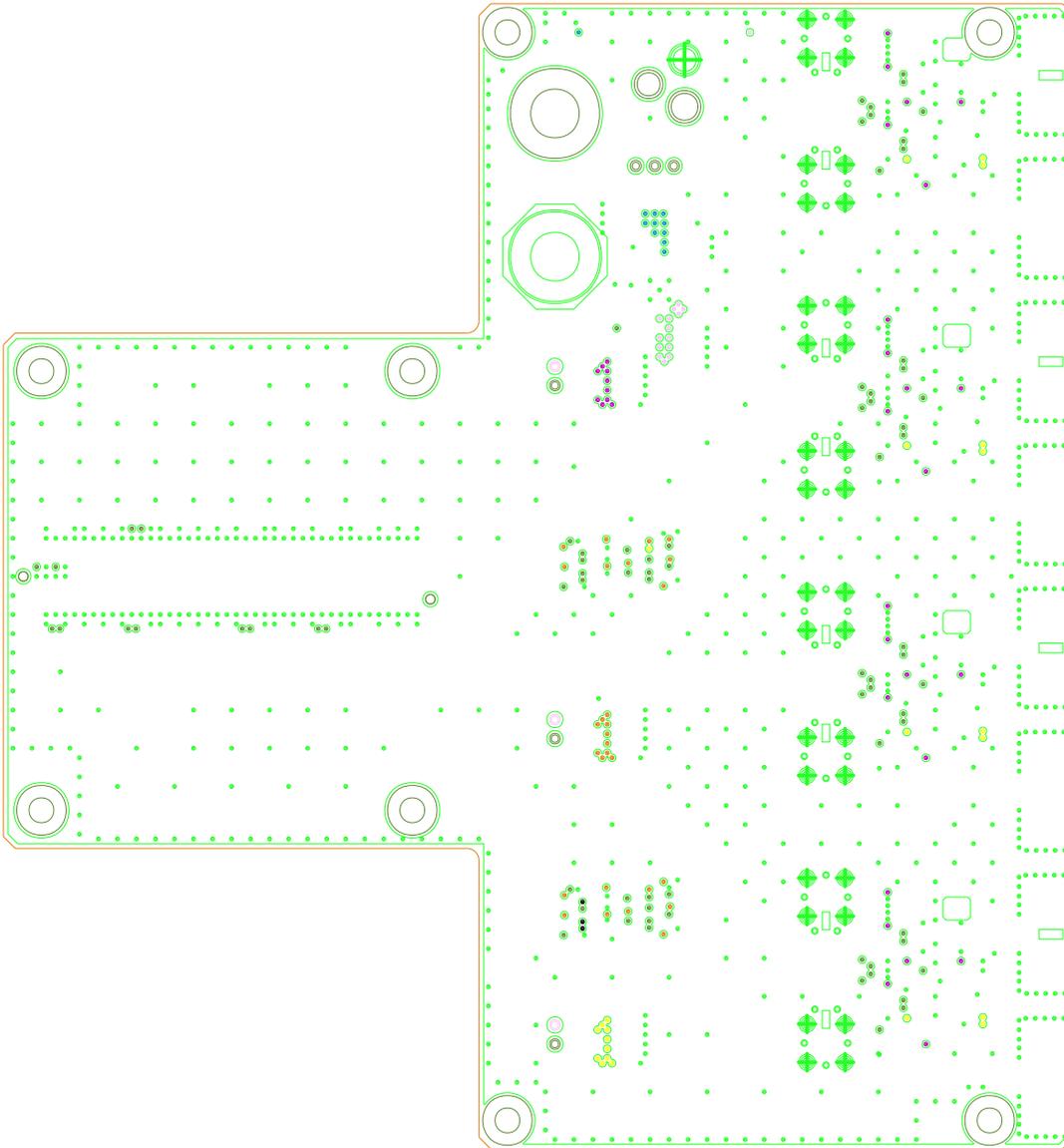


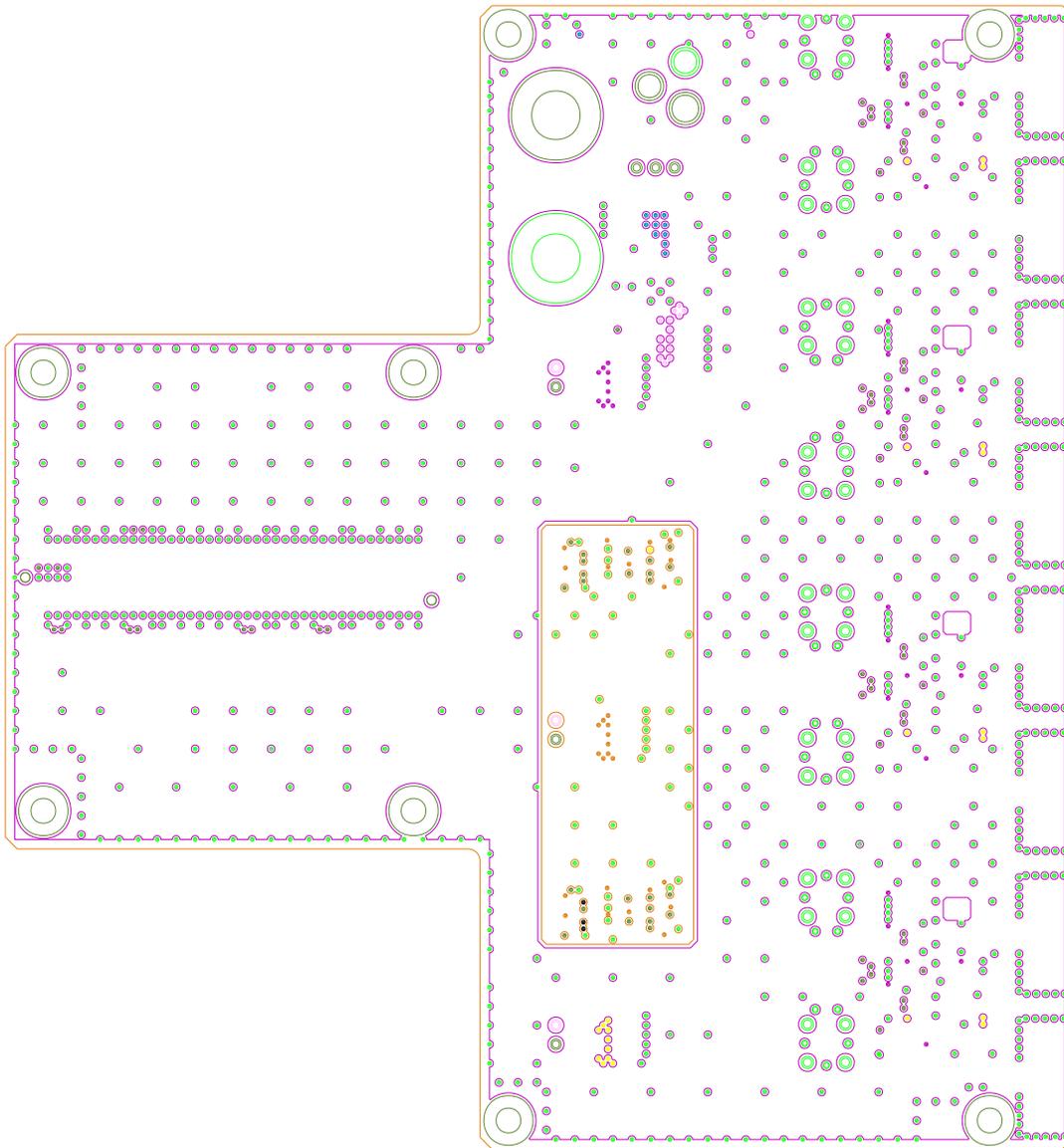
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	CUSTOMER: TEXAS INSTRUMENTS		KSID: 15254	JOB NUMBER: 123933
	BOARD NAME: TLK10XXX HD-SDI DAUGHTER BOARD		LAYER DESCRIPTION: TOP, LAYER 1	
ENGINEER: J. NERGER	PCB DESIGNER: M. THREET	BOARD REV: 1.0	RELEASE DATE: 08/15/2014	SHEET NUMBER: 1 of 13



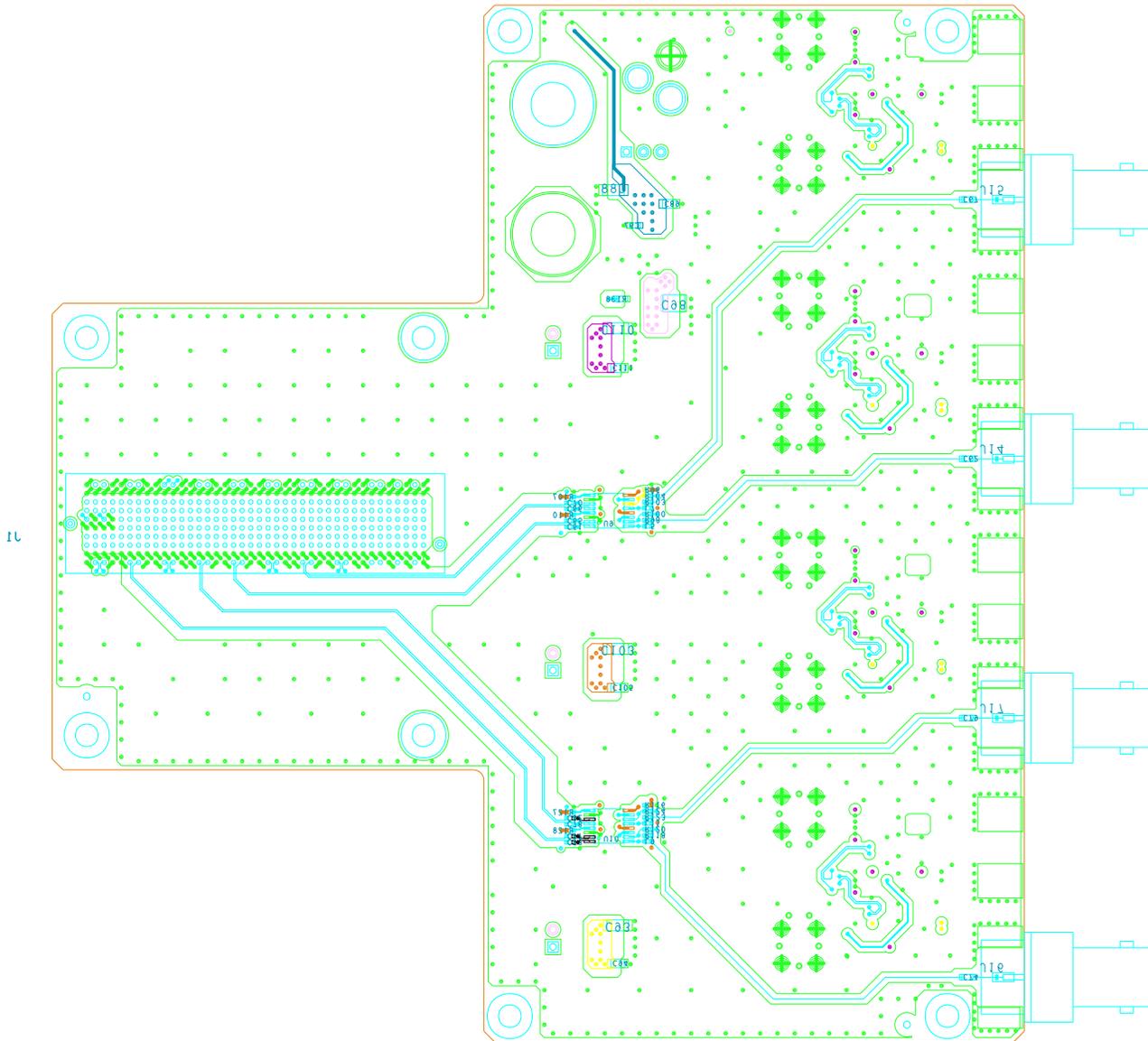
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	CUSTOMER: TEXAS INSTRUMENTS		KSID: 15254	JOB NUMBER: 123933
	BOARD NAME: TLK10XXX HD-SDI DAUGHTER BOARD		LAYER DESCRIPTION: GND1, LAYER 2	
	ENGINEER: J. NERGER	PCB DESIGNER: M. THREET	BOARD REV: 1.0	RELEASE DATE: 08/15/2014



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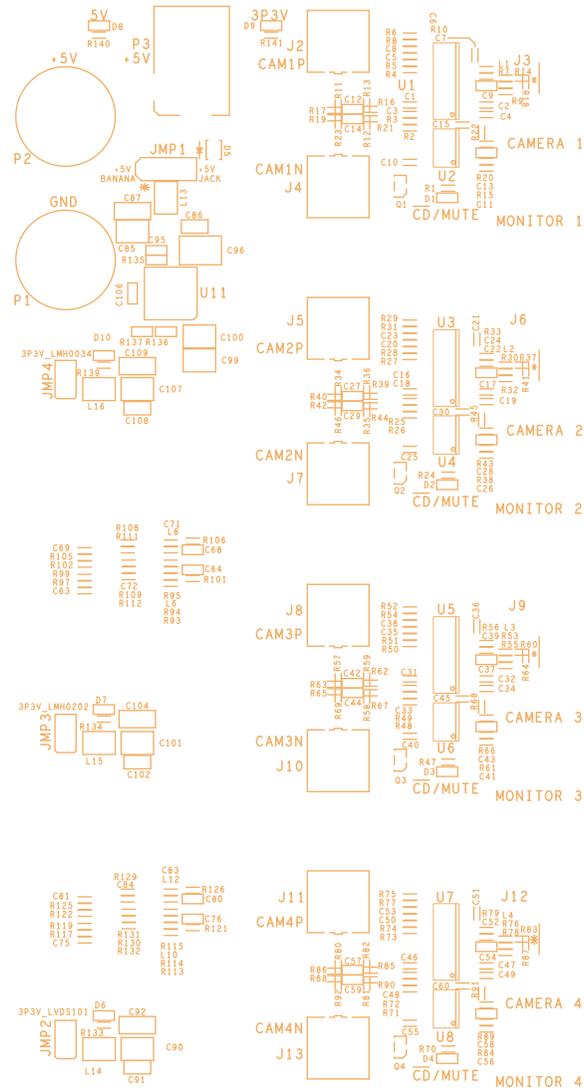
	CUSTOMER: TEXAS INSTRUMENTS		KSID: 15254	JOB NUMBER: 123933
	BOARD NAME: TLK10XXX HD-SDI DAUGHTER BOARD		LAYER DESCRIPTION: GND2, LAYER 3	
	ENGINEER: J. NERGER	PCB DESIGNER: M. THREET	BOARD REV: 1.0	RELEASE DATE: 08/15/2014



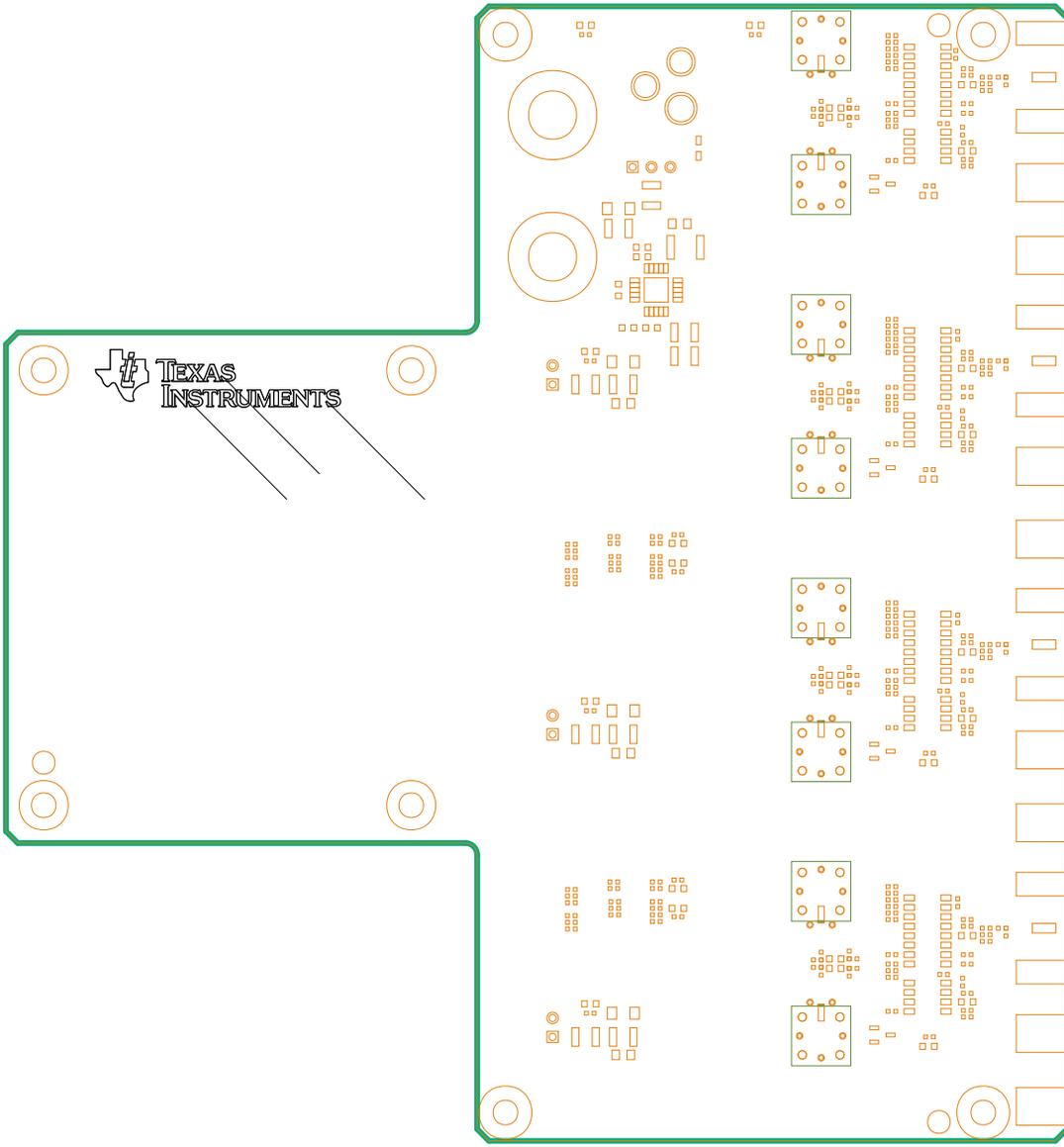
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	CUSTOMER: TEXAS INSTRUMENTS		KSID: 15254	JOB NUMBER: 123933	
	BOARD NAME: TLK10XXX HD-SDI DAUGHTER BOARD		LAYER DESCRIPTION: BOTTOM, LAYER 6		
	ENGINEER: J. NERGER	PCB DESIGNER: M. THREET	BOARD REV: 1.0	RELEASE DATE: 08/15/2014	SHEET NUMBER: 6 of 13

TLK10XXX HD-SDI
INTERFACE BOARD
6583088

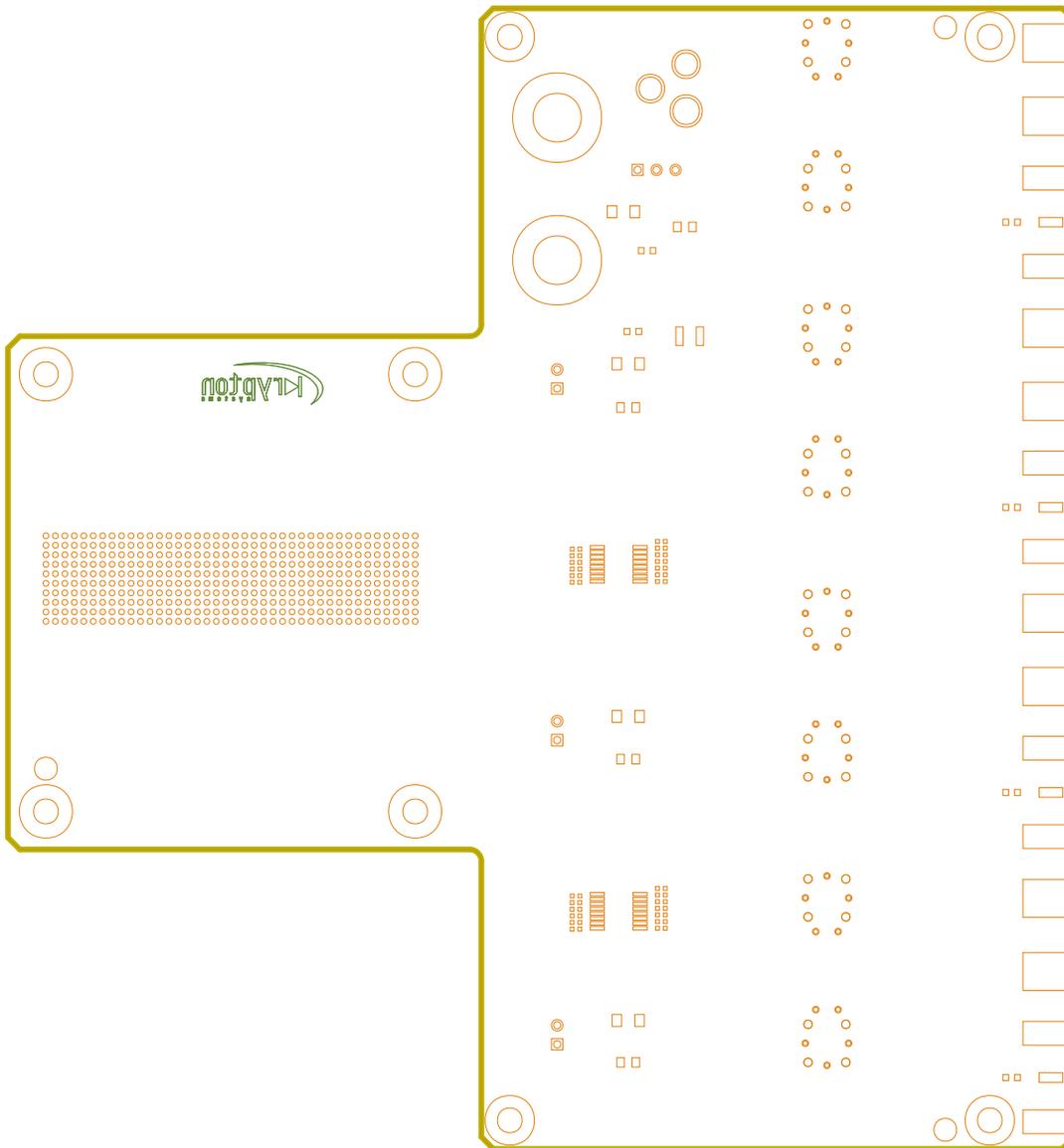


	CUSTOMER: TEXAS INSTRUMENTS		KSID: 15254	JOB NUMBER: 123933
	BOARD NAME: TLK10XXX HD-SDI DAUGHTER BOARD		LAYER DESCRIPTION: SILKSCREEN TOP	
ENGINEER: J. NERGER	PCB DESIGNER: M. THRETT	BOARD REV: 1.0	RELEASE DATE: 08/15/2014	SHEET NUMBER: 9 of 13



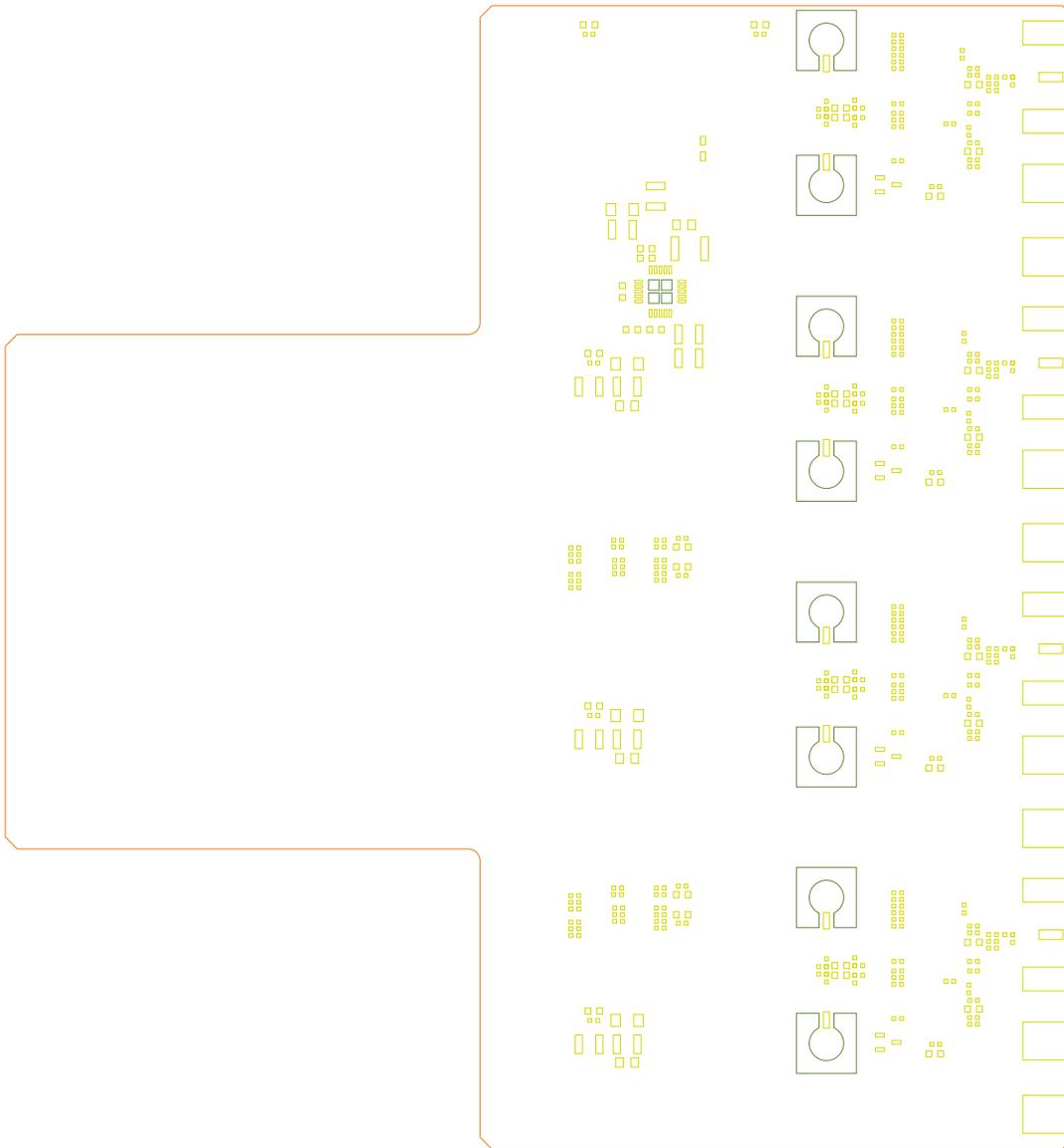
TEXAS INSTRUMENTS

	CUSTOMER: TEXAS INSTRUMENTS		KSID: 15254	JOB NUMBER: 123933
	BOARD NAME: TLK10XXX HD-SDI DAUGHTER BOARD		LAYER DESCRIPTION: SOLDERMASK TOP	
	ENGINEER: J. NERGER	PCB DESIGNER: M. THREET	BOARD REV: 1.0	RELEASE DATE: 08/15/2014

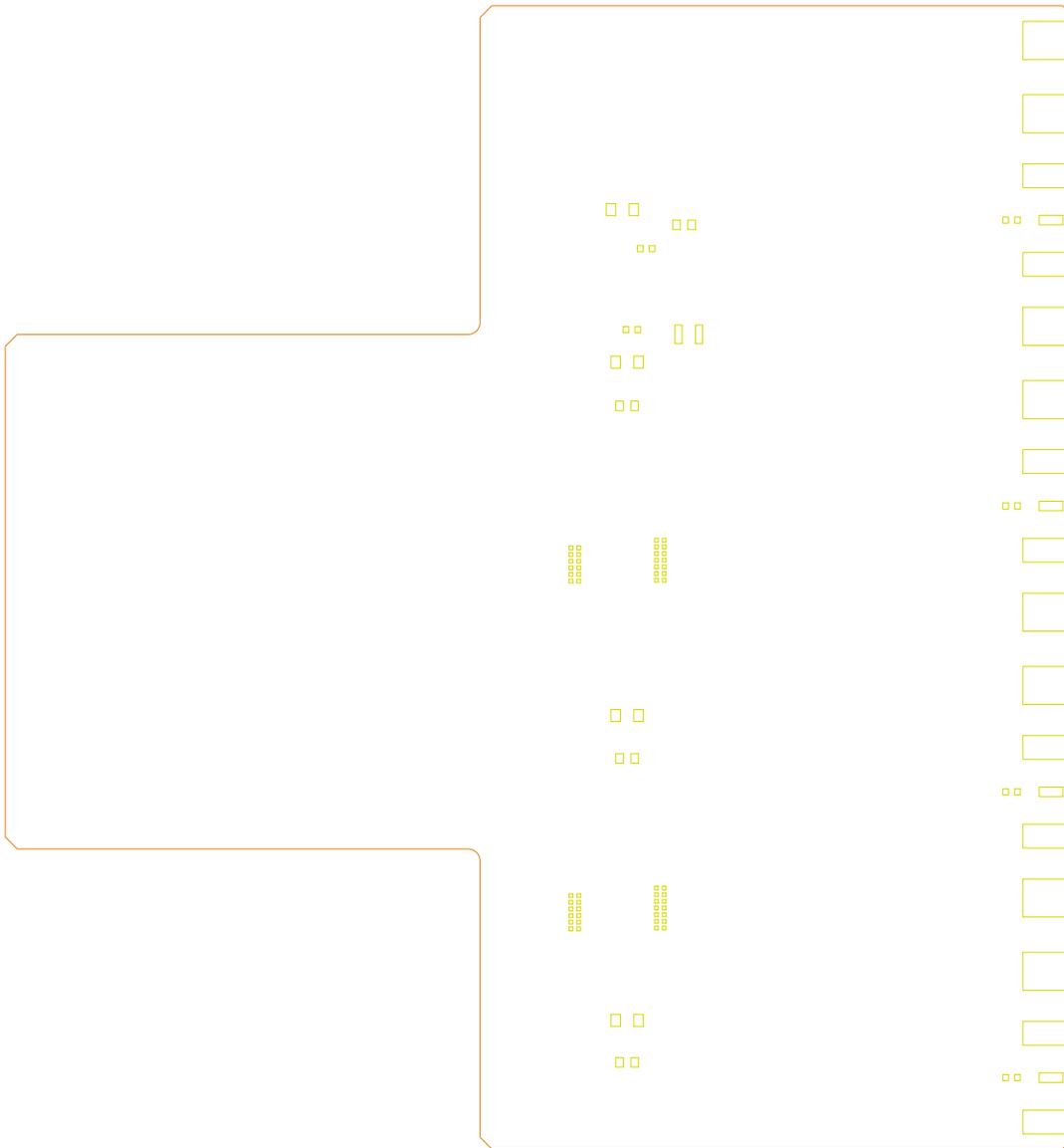


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	CUSTOMER: TEXAS INSTRUMENTS		KSID: 15254	JOB NUMBER: 123933
	BOARD NAME: TLK10XXX HD-SDI DAUGHTER BOARD		LAYER DESCRIPTION: SOLDERMASK BOTTOM	
	ENGINEER: J. NERGER	PCB DESIGNER: M. THREET	BOARD REV: 1.0	RELEASE DATE: 08/15/2014

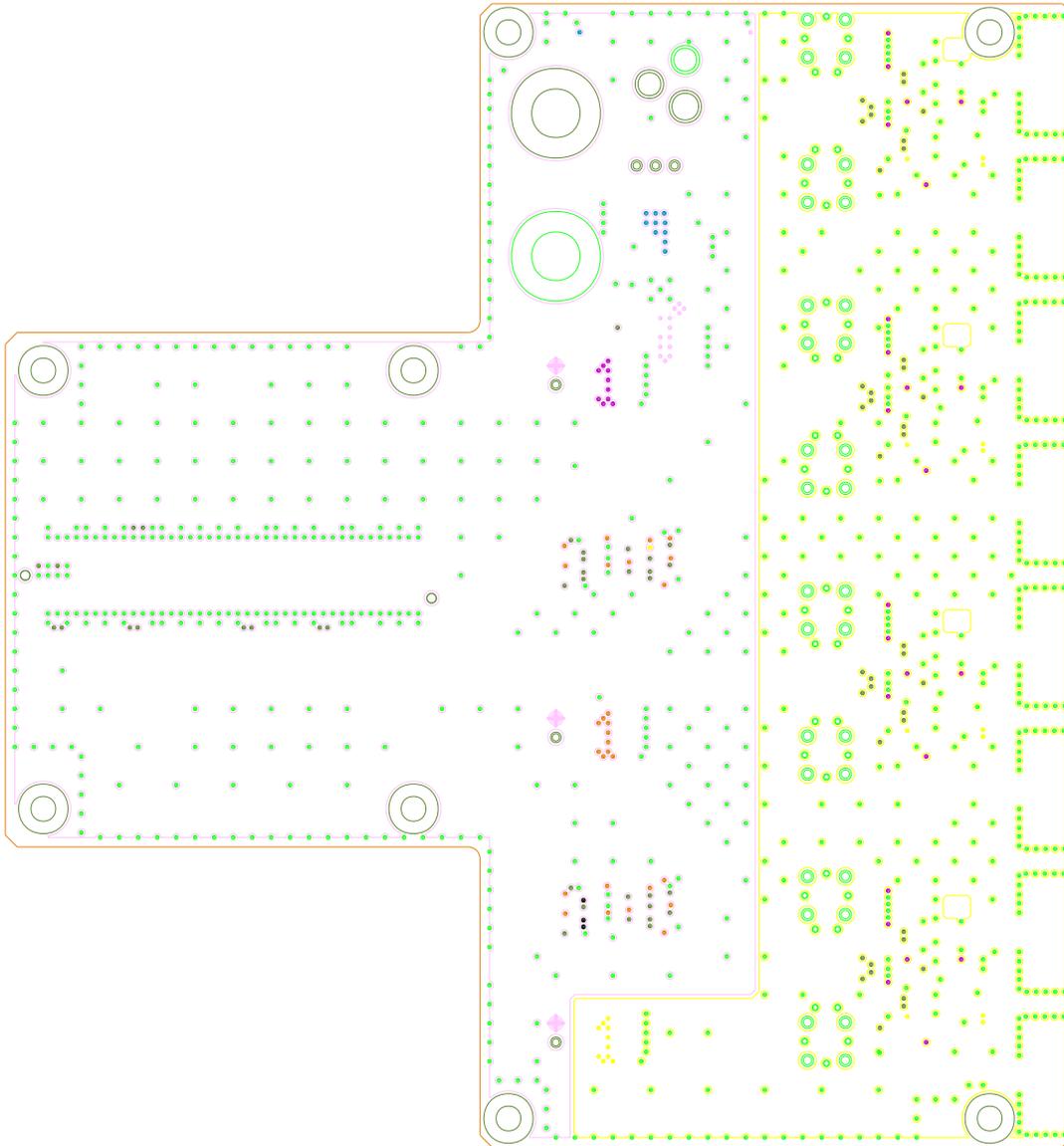


	CUSTOMER: TEXAS INSTRUMENTS		KSID: 15254	JOB NUMBER: 123933	
	BOARD NAME: TLK10XXX HD-SDI DAUGHTER BOARD		LAYER DESCRIPTION: SOLDERPASTE TOP		
	ENGINEER: J. NERGER	PCB DESIGNER: M. THREEET	BOARD REV: 1.0	RELEASE DATE: 08/15/2014	SHEET NUMBER: 11 of 13



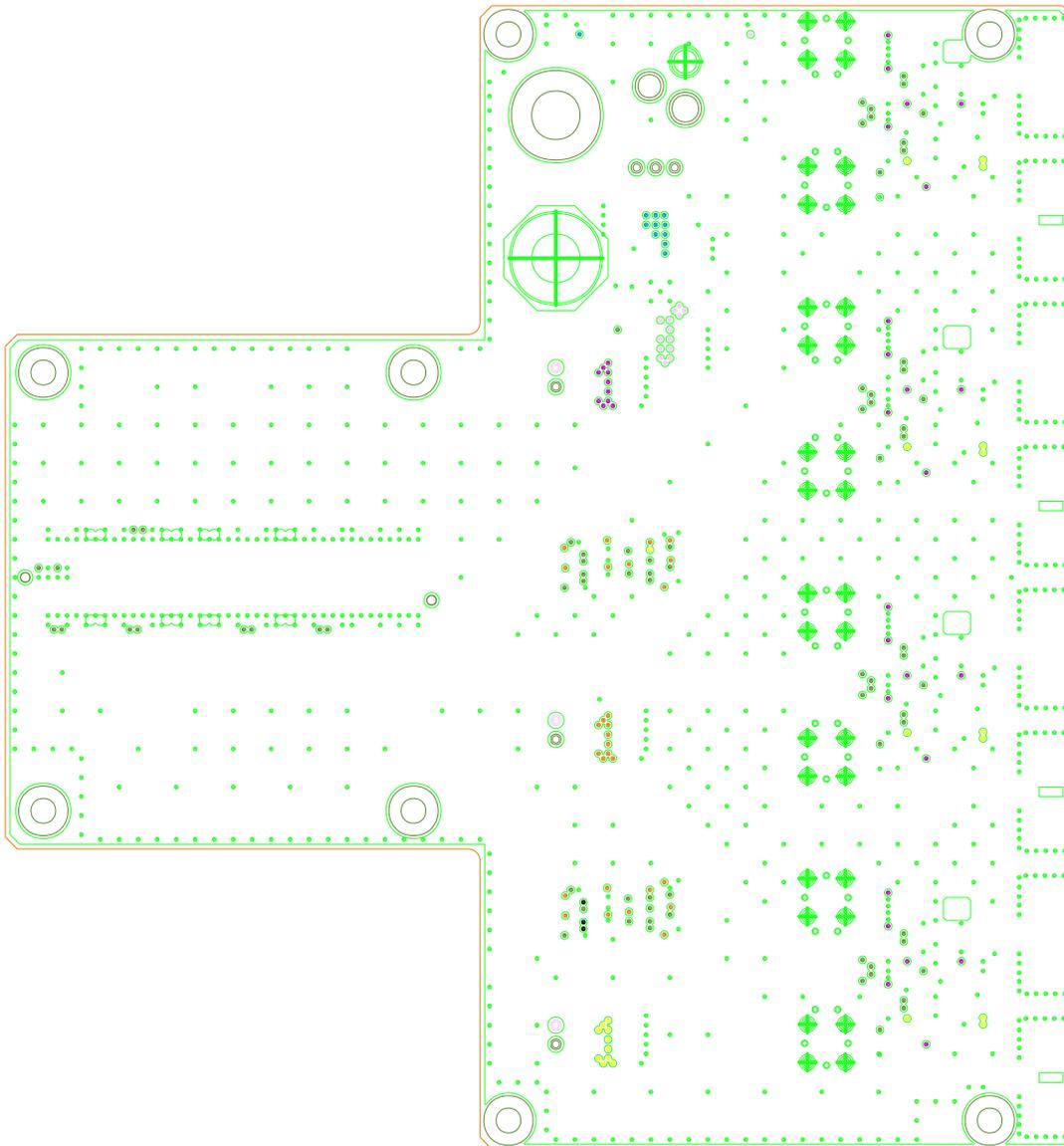
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	CUSTOMER: TEXAS INSTRUMENTS		KSID: 15254	JOB NUMBER: 123933	
	BOARD NAME: TLK10XXX HD-SDI DAUGHTER BOARD		LAYER DESCRIPTION: SOLDERPASTE BOTTOM		
	ENGINEER: J. NERGER	PCB DESIGNER: M. THREEET	BOARD REV: 1.0	RELEASE DATE: 08/15/2014	SHEET NUMBER: 12 of 13



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	CUSTOMER: TEXAS INSTRUMENTS		KSID: 15254	JOB NUMBER: 123933
	BOARD NAME: TLK10XXX HD-SDI DAUGHTER BOARD		LAYER DESCRIPTION: GND3, LAYER 4	
	ENGINEER: J. NERGER	PCB DESIGNER: M. THREET	BOARD REV: 1.0	RELEASE DATE: 08/15/2014



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	CUSTOMER: TEXAS INSTRUMENTS		KSID: 15254	JOB NUMBER: 123933
	BOARD NAME: TLK10XXX HD-SDI DAUGHTER BOARD		LAYER DESCRIPTION: GND4, LAYER 5	
	ENGINEER: J. NERGER	PCB DESIGNER: M. THREET	BOARD REV: 1.0	RELEASE DATE: 08/15/2014

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

FABRICATION NOTE (DIMENSIONS ARE IN INCHES AND [mm])

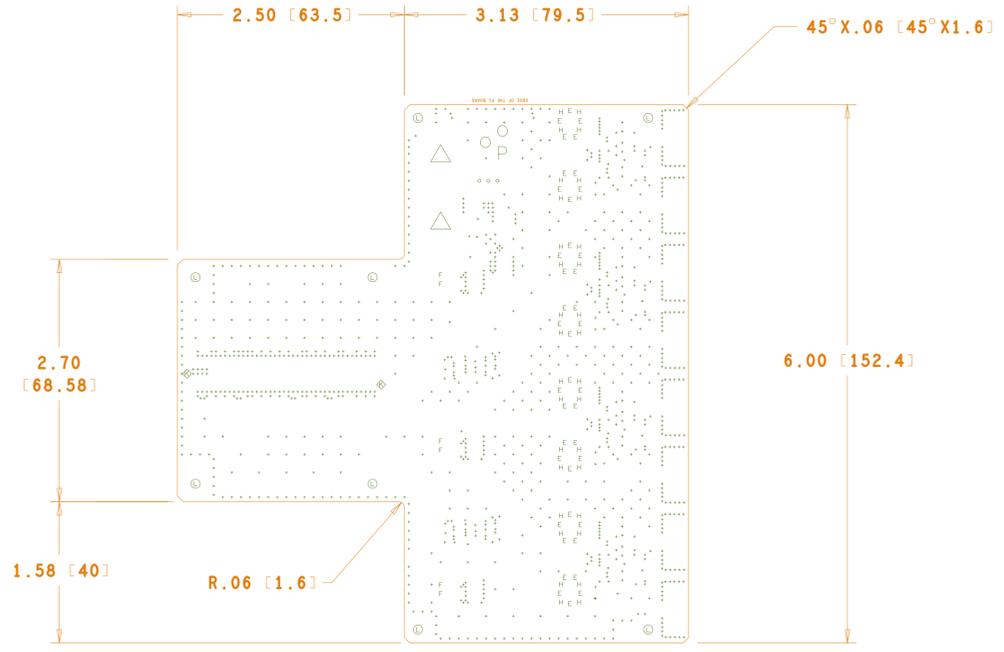
- 1: ALL FABRICATION ITEMS MUST MEET OR EXCEED BEST INDUSTRY PRACTICE IPC-A-600C (COMMERCIAL STANDARD).
- 2: LAMINATE MATERIAL: COPPER CLAD FR4 370 HR or EQUIVALENT.
- 3: COPPER WEIGHT: 1.0 OZ MIN OUTER LAYERS / 1.0 OZ INNER LAYERS.
- 4: FINISH BOARD THICKNESS: 0.064 +/- .010 INCH.
- 5: POSITION ACCURACY: +/- .0015 INCH.
- 6: WARP AND TWIST NOT TO EXCEED .020/ INCH.
- 7: CONTROLLED IMPEDANCE LAYERS: SEE TABLE 1
- 8: LAYER COUNT: 6
- 9: VIA PADS FOR ALL UNUSED INTERNAL SIGNAL LAYERS MAY BE REMOVED DURING BOARD MANUFACTURING.

PROCESS NOTES:

- 1: COPPER PLATING TO BE 0.001 INCH MINIMUM IN ALL PLATED THROUGH HOLES.
- 2: CIRCUITRY ON OUTER LAYERS TO BE ELECTROLESS NICKEL IMMERSION GOLD AND MEET OR EXCEED IPC-4552. 2 uIN MIN OF IMMERSION GOLD APPLIED OVER 120 - 240 uIN OF ELECTROLESS NICKEL.
- 3: SOLDERMASK BOTH SIDES, COLOR: BLUE.
- 4: APPLY WHITE LPI SILKSCREEN TO TOP AND BOTTOM SIDE OF BOARD USING SEPARATE ARTWORK.
- 5: THIS BOARD MUST BE RoHS COMPLIANT.
- 6: SAMPLE CROSS SECTION MUST BE PROVIDED BY VENDOR.
- 7: ALL 10 MIL HOLE VIA PADS SHALL BE TENTED (COVERED WITH SOLDER RESIST).

TRACE WIDTHS AND ROUTING:

- 1: TRACE WIDTH CALCULATIONS ARE STARTING VALUES. BOARD SHOP MAY ADJUST TRACE WIDTHS TO COMPENSATE FOR PROCESS.
- 2: DIELECTRIC CONSTANT: POLYCLAD 370 HR OR EQUIVALENT.



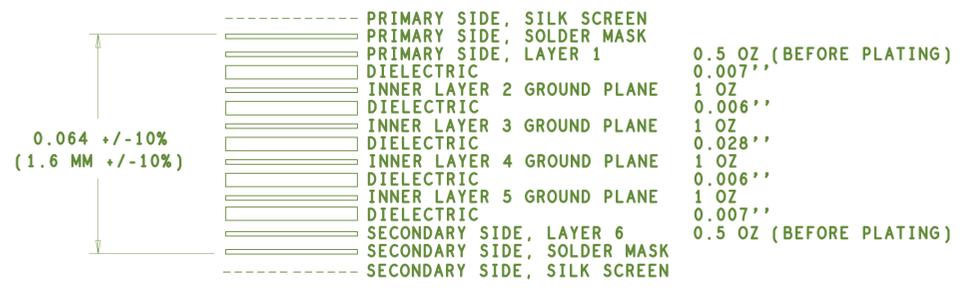
DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
.	10.0	+2.0/-2.0	PLATED	1057
e	24.0	+3.0/-3.0	PLATED	40
f	38.0	+3.0/-3.0	PLATED	6
o	38.0	+3.0/-3.0	PLATED	3
h	44.0	+3.0/-3.0	PLATED	32
o	120.0	+2.0/-2.0	PLATED	2
P	140.0	+0.0/-0.0	PLATED	1
△	255.0	+3.0/-3.0	PLATED	2
◇	50.0	+2.0/-2.0	NON-PLATED	2
⊙	130.0	+2.0/-2.0	NON-PLATED	8

TABLE 1: DIMENSIONS: INCHES

LAYER NO.	DIFFERENTIAL PAIR IMPEDANCE (OHMS)	SINGLE ENDED TRACE WIDTH	DIFF TRACE WIDTH	DIFF TRACE SPACING
L1(TOP) L6(BOT)	100 +/- 10%		0.0055	0.006
L1(TOP) L6(BOT)	75 +/- 10%	0.004		
L1(TOP) L6(BOT)	50 +/- 10%	0.011		

	CUSTOMER:	TEXAS INSTRUMENTS	KSID:	15254	JOB NUMBER:	123933
	BOARD NAME:	TLK10XXX HD-SDI DAUGHTER BOARD	LAYER DESCRIPTION:	FABRICATION		
	ENGINEER:	J. NERGER	PCB DESIGNER:	M. THREET	BOARD REV:	1.0
			RELEASE DATE:	08/15/2014	SHEET NUMBER:	13 of 13

LAYER STACK-UP



SIGNATURES		DATE	TEXAS INSTRUMENTS		
DRAWN			FABRICATION DRAWING		
CHECKED			TLK10XXX HD-SDI DAUGHTER BD		
ENGRG			SIZE	FSCM NO	DWG NO
ISSUED					
			SCALE	NONE	SHEET 1 of 1

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