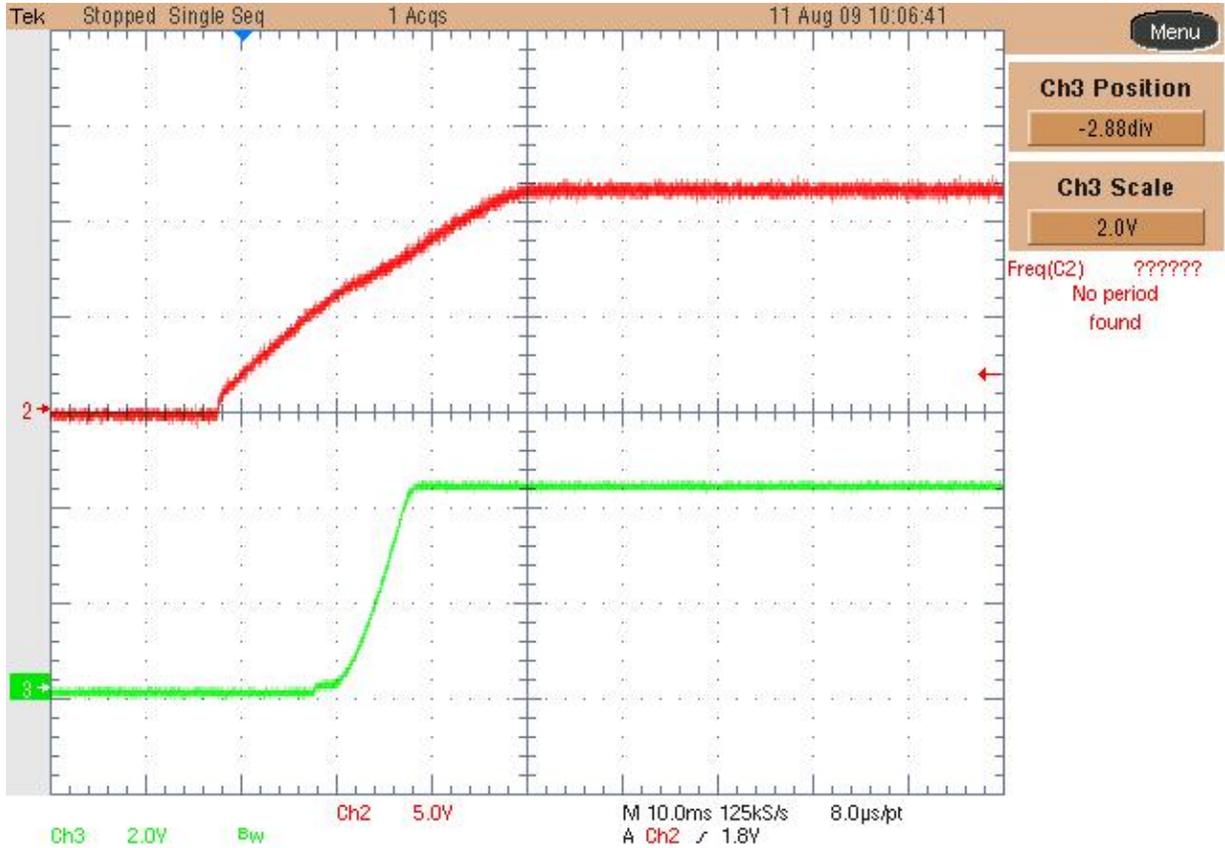


1 Startup

The output voltage at startup is shown in the image below. Input voltage was set to 12Vdc. The output was loaded with a 5A constant current.

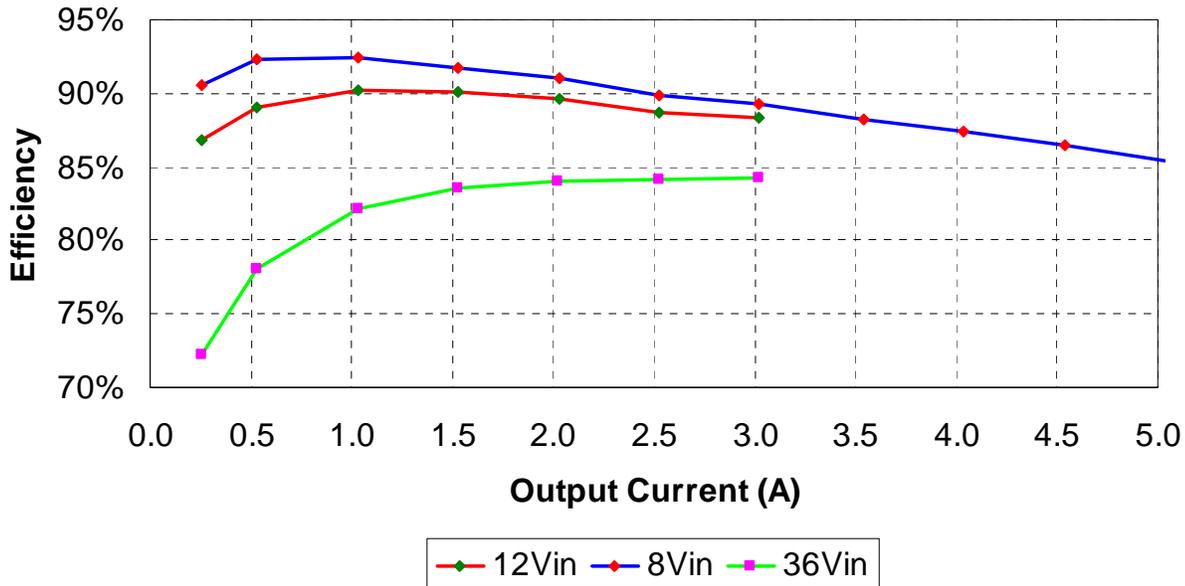
Channel 2 shows the input voltage ramp up (5 V/div, 10ms/div).

Channel 3 shows the output voltage (2 V/div).



2 Efficiency

The efficiency data is shown in the tables and graph below.



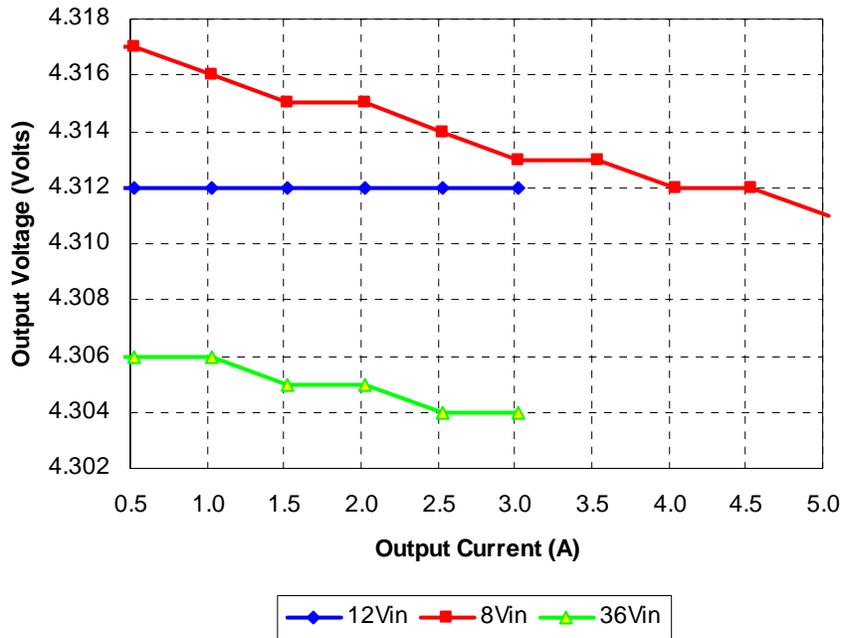
Iout (A)	Vout (V)	Pout (W)	Iin (A)	Vin (V)	Pin (W)	Ploss (W)	Eff
0.2585	4.312	1.11	0.1066	12.05	1.28	0.17	86.8%
0.5319	4.312	2.29	0.2137	12.06	2.58	0.28	89.0%
1.0308	4.312	4.44	0.4100	12.01	4.92	0.48	90.3%
1.5280	4.312	6.59	0.6059	12.07	7.31	0.72	90.1%
2.0270	4.312	8.74	0.8115	12.02	9.75	1.01	89.6%
2.5250	4.312	10.89	1.0157	12.08	12.27	1.38	88.7%
3.0230	4.312	13.04	1.2220	12.08	14.76	1.73	88.3%

Iout (A)	Vout (V)	Pout (W)	Iin (A)	Vin (V)	Pin (W)	Ploss (W)	Eff
0.2584	4.317	1.12	0.1536	8.016	1.23	0.12	90.6%
0.5320	4.317	2.30	0.3099	8.024	2.49	0.19	92.4%
1.0308	4.316	4.45	0.6014	8.001	4.81	0.36	92.5%
1.5280	4.315	6.59	0.8932	8.048	7.19	0.60	91.7%
2.0270	4.315	8.75	1.1960	8.032	9.61	0.86	91.0%
2.5250	4.314	10.89	1.5050	8.056	12.12	1.23	89.8%
3.0230	4.313	13.04	1.8180	8.032	14.60	1.56	89.3%
3.5380	4.313	15.26	2.1580	8.013	17.29	2.03	88.2%
4.0370	4.312	17.41	2.4730	8.058	19.93	2.52	87.4%
4.5370	4.312	19.56	2.8030	8.073	22.63	3.07	86.5%
5.0330	4.311	21.70	3.1380	8.095	25.40	3.70	85.4%

Iout (A)	Vout (V)	Pout (W)	Iin (A)	Vin (V)	Pin (W)	Ploss (W)	Eff
0.2582	4.306	1.11	0.0427	36.03	1.54	0.43	72.3%
0.5311	4.306	2.29	0.0813	36.02	2.93	0.64	78.1%
1.0298	4.306	4.43	0.1499	36.00	5.40	0.96	82.2%
1.5270	4.305	6.57	0.2184	36.04	7.87	1.30	83.5%
2.0260	4.305	8.72	0.2880	36.03	10.38	1.65	84.1%
2.5240	4.304	10.86	0.3584	36.01	12.91	2.04	84.2%
3.0220	4.304	13.01	0.4285	36.01	15.43	2.42	84.3%

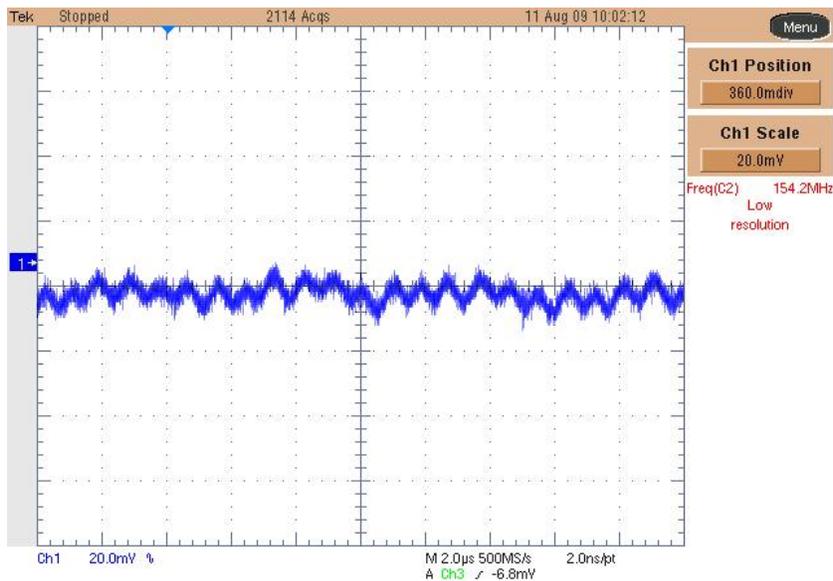
3 Output Voltage Regulation

The output voltage versus load current is plotted below.



4 Output Ripple Voltage

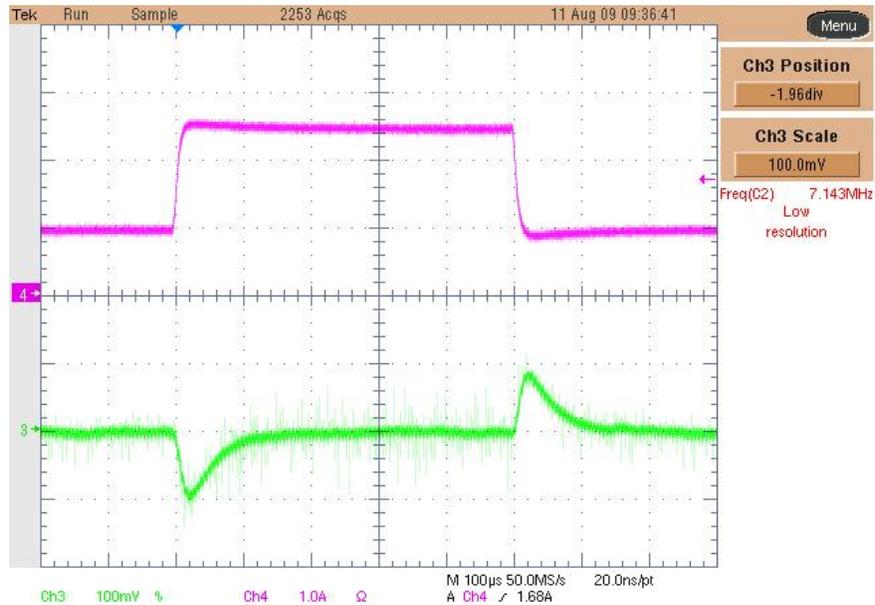
The output ripple voltage is shown in the plot below. The input was set to 12V and the load was set to 3A. Channel 1: output voltage (ac coupled, full bandwidth 20 mV/div, 2us/div).



5 Load Transient

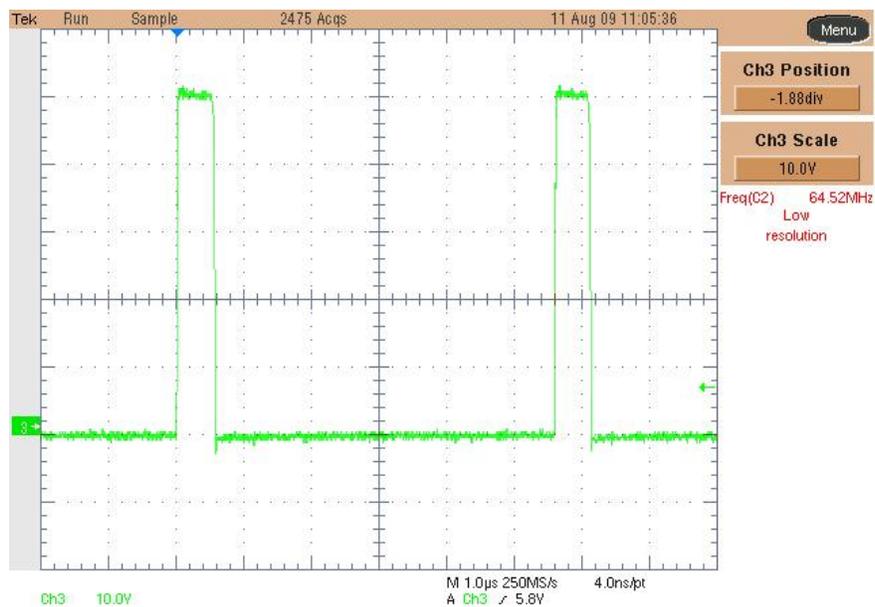
The image below shows the response to 1A to 2.5A load transient on the output voltage. The input voltage was set to 16V.

Channel 3: Vout (ac coupled) 100mV/div, Channel 4: Iout 1A/div, 100us/div.



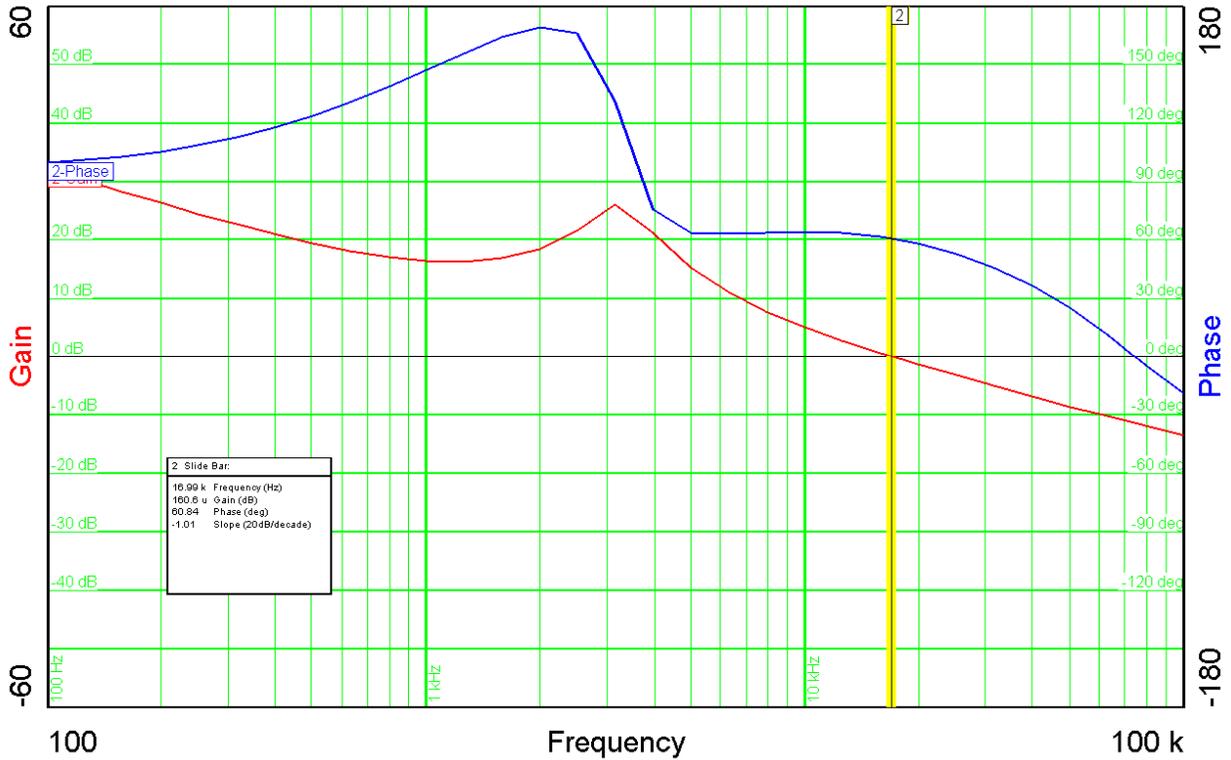
6 Switch-node

The image below shows the switch-node waveform. The input voltage was set to 50V during a 3A load condition. Channel 3: Vds(TP4), 10V/div, 1us/div, full bandwidth.



7 Loop Response

The image below shows the loop response of the converter measured with a 12V input, and 3A load. Phase margin is 60.84 deg. and crossover frequency is 16.99 KHz.



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