

# TI Designs: TIDA-01423

## 3-V to 4.5-V Input, 400-mA, -12-V Inverting Buck-Boost Reference Design



### Description

The TIDA-01423 TI Design demonstrates an inverting buck-boost converter (voltage inverter) to generate a -12-V rail at 400 mA of current from a 3-V to 4.5-V input voltage. Such a negative voltage is required for many communications equipment systems as well as industrial equipment, such as test and measurement. Using the TPS62136 buck converter enables a very-simple negative voltage inverter (inverting buck-boost) design to create a 12-V negative output voltage at 400-mA currents.

### Resources

[TIDA-01423](#)  
[TPS62136](#)

Design Folder  
 Product Folder

### Features

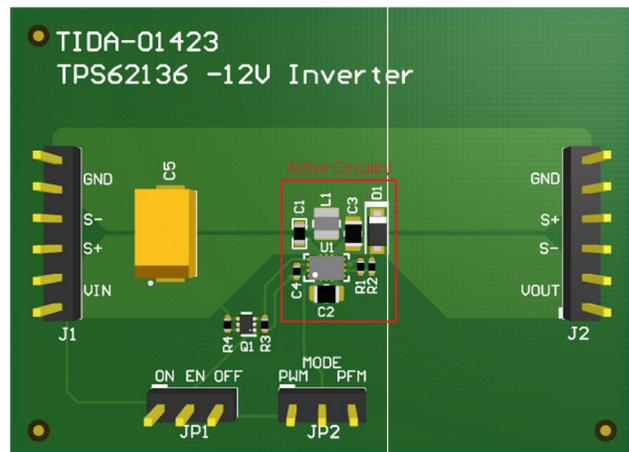
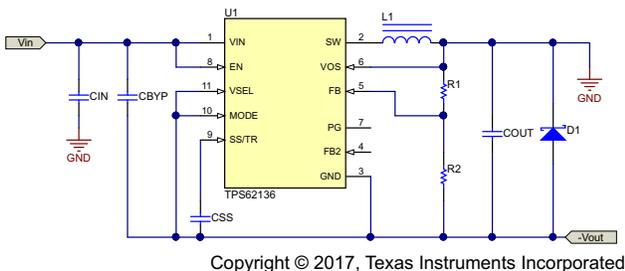
- High Negative Output Voltage of -12 V
- Total Solution Size Less Than 65 mm<sup>2</sup>
- High Output Current of 400 mA
- Low Output Voltage Ripple (<0.5 %)
- Input Voltage Range of 3 V to 4.5 V

### Applications

- [Telecom Infrastructure](#)
- [Wireless Infrastructure](#)
- [Optical Modules](#)
- [Optical Networking: EPON](#)
- [Remote Radio Unit \(RRU\)](#)



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## 1 System Description

A negative voltage in the range of -5 V to -12 V is frequently required in high-performance communications equipment systems, such as optical modules and remote radio units.

In an optical module, the negative voltage is required to supply modulators like the electroabsorption modulator (EAM) or Mach-Zehnder modulator (MZM). The high efficiency (low temperature rise) and small size is very important in such systems.

Such high negative voltages are also required for the new Gallium Nitride (GaN) technology (field-effect transistor (FET) and RF power amplifier) used in antenna systems and remote radio units.

The wide-output voltage range supports many of the different voltages required in such systems, which enables the same design to be reused for different systems that have different negative voltage rails.

### 1.1 Key System Specifications

**Table 1. Key System Specifications**

PARAMETERS	SPECIFICATIONS	DETAILS
Input voltage range ( $V_{IN}$ )	3 V to 4.5 V	—
Output voltage ( $V_{OUT}$ )	-12 V	—
Output current	0.4 A	<a href="#">Figure 4</a>

## 2 System Overview

### 2.1 Highlighted Products

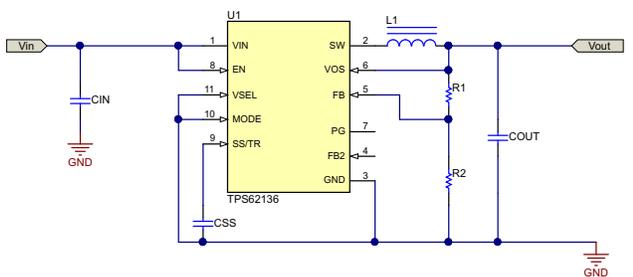
#### 2.1.1 TPS62136

The TPS62136 is a 4-A, step-down converter in a 2x3-mm QFN package based on a distributed control system (DCS). The device accepts up to a 17-V input voltage and supports up to 12 V on its output. This wide-input voltage range is ideally suited for an inverting converter, which, at a minimum, requires a voltage rating of the input voltage plus the output voltage.

### 2.2 Design Considerations

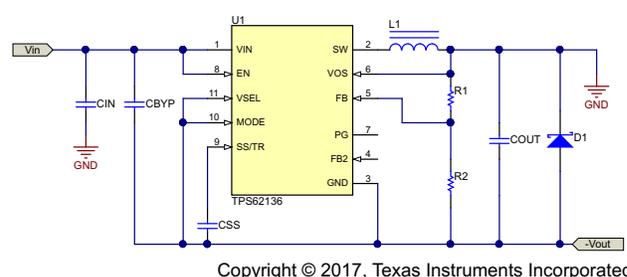
#### 2.2.1 Inverting Buck-Boost Topology Concept

The inverting buck-boost topology is very similar to the buck topology. In the buck configuration that [Figure 1](#) shows: the positive connection ( $V_{OUT}$ ) is connected to the inductor and the return connection is connected to the ground (GND) pin of the integrated circuit (IC). However, in the inverting buck-boost configuration that [Figure 2](#) shows, the IC ground is used as the negative output voltage pin (labeled as  $-V_{OUT}$ ). The former positive output in the buck configuration is used as the ground. This inverting topology allows the output voltage to be inverted and always lower than the ground.



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Figure 1. TPS62136 Buck Topology



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Figure 2. TPS62136 Inverting Buck-Boost Topology

The circuit operation is different in the inverting buck-boost topology than in the buck topology. [Figure 3 \(a\)](#) shows that the output voltage terminals are reversed, though the components are wired the same as a buck converter. As [Figure 3 \(b\)](#) shows, during the ON-time of the control MOSFET, the inductor is charged with current while the output capacitor supplies the load current. The inductor does not provide current to the load during this time. During the OFF-time of the control MOSFET and the ON-time of the synchronous MOSFET shown in [Figure 3 \(c\)](#), the inductor provides current to the load and the output capacitor. These changes affect many parameters, which the following subsections describe in further detail.

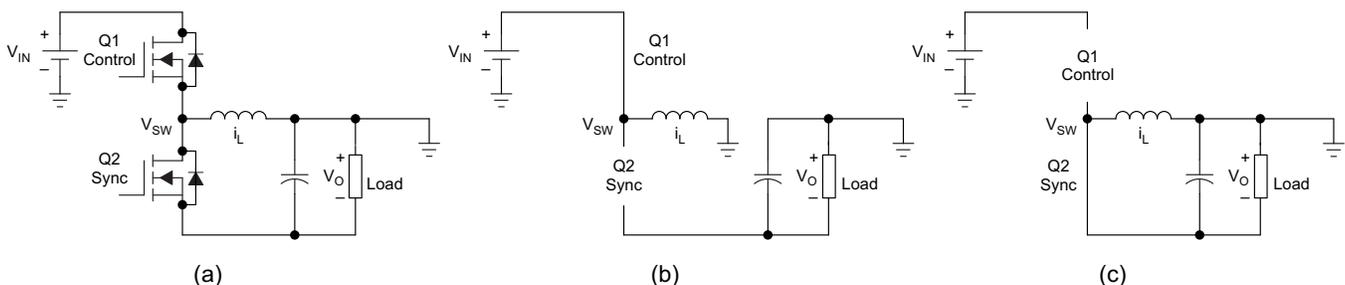


Figure 3. Inverting Buck-Boost Configuration

The average inductor current is affected in this topology. In the buck configuration, the average inductor current is equal to the average output current because the inductor always supplies current to the load during both the ON- and OFF-times of the control MOSFET. However, in the inverting buck-boost configuration, only the output capacitor supplies the load with current, while the load is completely disconnected from the inductor during the ON-time of the control MOSFET. During the OFF-time, the inductor connects to both the output capacitor and the load (see [Figure 3](#)). Because the OFF-time is  $1 - D$  of the switching period, the average inductor current in [Equation 1](#) is calculated as:

$$I_{L(Avg)} = \left| \frac{I_{OUT}}{(1-D)} \right| \quad (1)$$

The duty cycle for the typical buck converter is simply  $V_{OUT} / V_{IN}$ , but the calculation of the ideal duty cycle in [Equation 2](#) for an inverting buck-boost converter becomes:

$$D = \frac{V_{OUT}}{(V_{OUT} - V_{IN})} \quad (2)$$

[Equation 3](#) provides the peak-to-peak inductor ripple current:

$$\Delta I_L = \frac{V_{IN} D}{f_s L} \quad (3)$$

where,

- $\Delta I_L$  (A): Peak-to-peak inductor ripple current
- D: Duty cycle
- $f_s$  (MHz): Switching frequency
- L ( $\mu$ H): Inductor value
- $V_{IN}$  (V): Input voltage with respect to ground, not with respect to the device ground or  $V_{OUT}$ .

[Equation 4](#) calculates the maximum inductor current:

$$I_L = I_{L(avg)} + \frac{\Delta I_L}{2} \quad (4)$$

### 2.2.2 $V_{IN}$ and $V_{OUT}$ Range

The input voltage that can be applied to an integrated circuit (IC) operating in the inverting buck-boost topology is less than the input voltage for the same IC operating in the buck topology. The reason for this difference is because the ground pin of the IC is connected to the (negative) output voltage. Therefore, the input voltage across the device is  $V_{IN}$  to  $V_{OUT}$ , not  $V_{IN}$  to ground. Thus, the input voltage range of the TPS62136 is 3 V to  $17 \text{ V} + V_{OUT}$ , where  $V_{OUT}$  is a negative value.

The output voltage range is the same as when configured as a buck converter, but negative. The output voltage for the inverting buck-boost topology must be set between  $-0.8 \text{ V}$  and  $-12 \text{ V}$ . The output voltage is set in the same way as the buck configuration, with two resistors connected to the FB pin. The TIDA-01423 design sets the output voltage at  $-12 \text{ V}$ , which gives an input voltage range of 3 V to 5 V. However, TI does not recommend to use a 5-V input voltage because voltage tolerances on the input supply can violate the recommended operating range of TPS62136.

### 2.2.3 Capacitor Selection

An input capacitor,  $C_{IN}$ , is required to provide a low-impedance input voltage source to the inverter. A low equivalent series resistance (ESR) X5R or X7R ceramic capacitor is best for input voltage filtering and minimizing interference with other circuits. For most applications, a  $10\text{-}\mu\text{F}$  ceramic capacitor is recommended from  $V_{IN}$  to ground (system ground, not  $-V_{OUT}$ ). The  $C_{IN}$  capacitor value can be increased without any limit for better input voltage filtering.

On the output, the TIDA-01423 design uses a  $22\text{-}\mu\text{F}$  output capacitor, which has an effective capacitance of about  $10 \mu\text{F}$  at the  $-12\text{-V}$  output voltage. For maximum output current, a second output capacitor can help to increase the phase margin.

For the inverting buck-boost configuration of the TPS62136, installing a bypass capacitor, CBYP, to provide a low impedance source for the internal gate drivers is important. This capacitor is connected from  $V_{IN}$  to  $-V_{OUT}$ ; therefore, it requires the highest voltage rating. For most applications, a 22- $\mu$ F ceramic capacitor is recommended. The bypass capacitor provides an AC path from  $V_{IN}$  to  $-V_{OUT}$ . When  $V_{IN}$  is applied to the circuit, this  $dV/dt$  across a capacitor from  $V_{IN}$  to  $-V_{OUT}$  creates a current that must return to ground (the return of the input supply) to complete its loop. This current may flow through the body diode of the internal low-side MOSFET and the inductor to return to ground. Flowing through the body diode pulls the  $V_{OUT}$  pin below IC ground, which violates its absolute maximum rating. Such a condition may damage the TPS62136 device and is not recommended. For protective measure, a Schottky diode must be installed on the output, as the schematic in [Figure 2](#) shows.

To avoid excessive inrush current, a soft-start capacitor is installed on the SS/TR pin.

## 2.2.4 Maximum Output Current

In the inverting buck-boost topology, the maximum output current is reduced as compared to the buck topology. This reduction is a result of the peak inductor current being higher, as calculated in [Equation 4](#).

For example, for an output voltage of  $-12$  V, 1.5- $\mu$ H inductor, and input voltage of 3.3 V, the following calculations produce the maximum allowable output current that can be ensured based on the TPS62136 minimum current limit value of 4.8 A. Due to increased duty cycles when operating at high load current, the duty cycle used for the following maximum output current calculation in [Equation 5](#) must be increased by 5% for these conditions, which provides a more accurate maximum output current calculation.

$$D = \frac{V_{OUT}}{V_{OUT} - V_{IN}} \times 1.05 = \frac{-12}{-12 - 1.33} \times 1.05 = 0.82 \quad (5)$$

The switching frequency at maximum load is based on [Figure 9](#). Based on the inductor data sheet, the effective inductance value is approximately 1.1  $\mu$ H at 3-A current (see [Equation 6](#)).

$$\Delta I_L = \frac{V_{IN} \times D}{f_S \times L} = \frac{3.3 \times 0.82}{0.55 \text{ MHz} \times 1.1 \mu\text{H}} = 4.5 \text{ A} \quad (6)$$

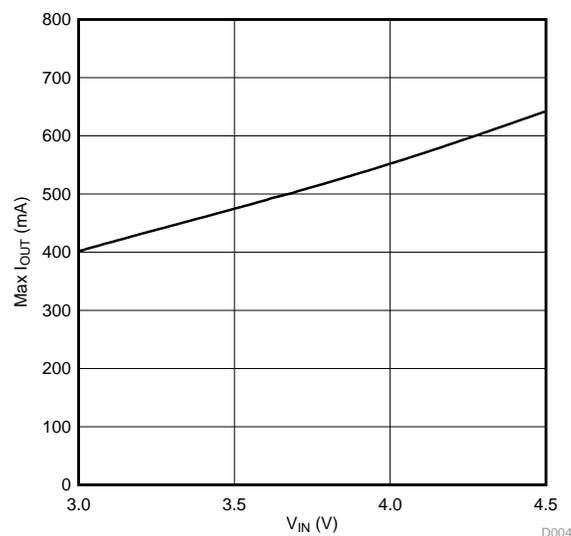
Rearranging [Equation 4](#) and setting  $I_{L(max)}$  equal to the minimum value of  $I_{LIMF}$ , as specified in the data sheet, results in [Equation 7](#):

$$I_{L(avg)} = I_{L(max)} - \frac{\Delta I_L}{2} = 4.8 - \frac{4.5}{2} = 2.5 \text{ A} \quad (7)$$

This result is then used in [Equation 1](#) to calculate the maximum achievable output current in [Equation 8](#):

$$I_{OUT} = I_{L(avg)} \times (1 - D) = 2.5 \text{ A} \times (1 - 0.82) = 450 \text{ mA} \quad (8)$$

[Figure 4](#) shows the maximum output current for the TIDA-01423 design.



**Figure 4. Maximum Output Current ( $V_{OUT} = -12$  V)**

### 2.2.5 Thermal Limits

With different conditions, thermal limits may become an issue as a result of the small size of the converter itself. As the output current increases, the absolute power loss (in mW) in the TPS62136 device also increases, which causes a higher temperature rise across the thermal impedance of the TPS62136 device.

The maximum allowed IC junction temperature is 125°C as stated in the TPS62136 data sheet. To calculate the IC temperature for different conditions, multiply the power loss of the TPS62136 device by the  $\theta_{JA}$ , which is approximately 40°C/W for the TIDA-01423 printed-circuit board (PCB), and add this value to the ambient temperature.

To calculate the maximum output current at any ambient temperature, simply subtract the maximum ambient temperature from 125°C to obtain the allowable temperature rise. Divide the  $\theta_{JA}$  of the PCB by this temperature rise to obtain the allowable IC power loss. Find this IC power loss for an input voltage of 3.3 V in Figure 8 to determine the maximum output current under specific conditions. See Equation 9 for the calculation.

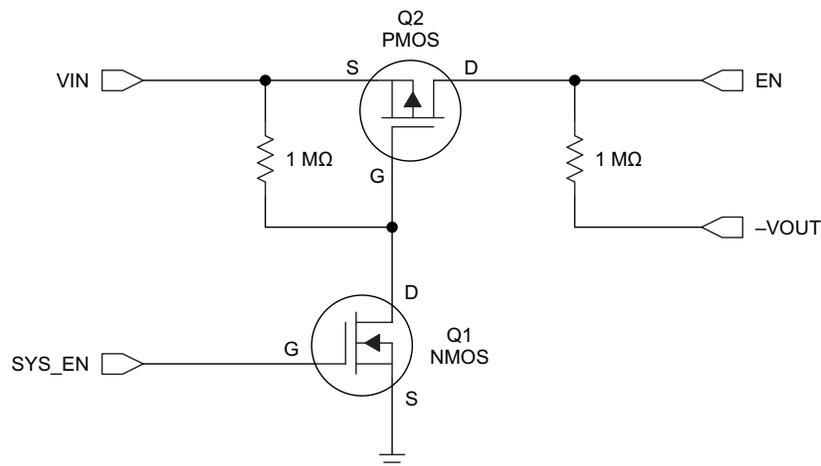
$$I_{C\_LOSS} \leq \frac{125 - T_{A\_MAX}}{\theta_{JA}} \tag{9}$$

### 2.2.6 Enable Pin Configuration

The device is enabled when the voltage at the EN pin trips its threshold and the input voltage is above the undervoltage lockout (UVLO) threshold. The TPS62136 device stops operation when the voltage on the EN pin falls below its threshold or the input voltage falls below the UVLO threshold.

Because  $V_{OUT}$  is the IC ground in this configuration, the EN pin must be referenced to  $V_{OUT}$  instead of ground. In the buck configuration, 0.83 V is considered as high and less than 0.67 V is considered as low. However, in the inverting buck-boost configuration, the  $V_{OUT}$  voltage is the reference; therefore, the high threshold is 0.83 V +  $V_{OUT}$  and the low threshold is 0.67 V +  $V_{OUT}$ . For example, if  $V_{OUT} = -12$  V, then  $V_{EN}$  is considered at a high level for voltages above -11.17 V and a low level for voltages below -11.24 V.

This behavior can cause difficulties when enabling or disabling the part because, in some applications, the IC that provides the EN signal may not be able to produce negative voltages. The level-shifter circuit that Figure 5 shows alleviates any difficulties associated with the offset EN threshold voltages by eliminating the requirement for negative EN signals. If disabling the TPS62136 is not desired, the EN pin may be directly connected to  $V_{IN}$  without this circuit.



NOTE:  $V_{OUT}$  is the negative output voltage of the inverting buck-boost converter.

**Figure 5. EN Pin Level Shifter**

The positive signal that originally drives EN is instead tied to the gate of Q1 (SYS\_EN). When Q1 is OFF (SYS\_EN grounded), Q2 has 0 V across its  $V_{GS}$  and also remains OFF. In this state, the EN pin is at -12 V, which is below the low-level threshold, and disables the device.

When SYS\_EN provides enough positive voltage to turn Q1 ON ( $V_{GS}$  threshold as specified in the MOSFET data sheet), the gate of Q2 is at ground potential through Q1. This action drives the  $V_{GS}$  of Q2 negative and turns Q2 ON. Then  $V_{IN}$  ties to EN through Q2 and the pin is above the high-level threshold, which turns the device ON. Be careful to ensure that the  $V_{GD}$  and  $V_{GS}$  of Q2 remain within the MOSFET ratings during both the enabled and disabled states. Failing to adhere to this constraint can result in damaged MOSFETs.

Figure 16 shows the enable sequence where the SYS\_EN signal activates the enable circuit. This circuit has been tested with a 3.3-V SYS\_EN signal and dual N/PFET Si1029X. The EN signal is the output of the circuit and goes from  $V_{IN}$  to  $V_{OUT}$  to properly enable and disable the device.

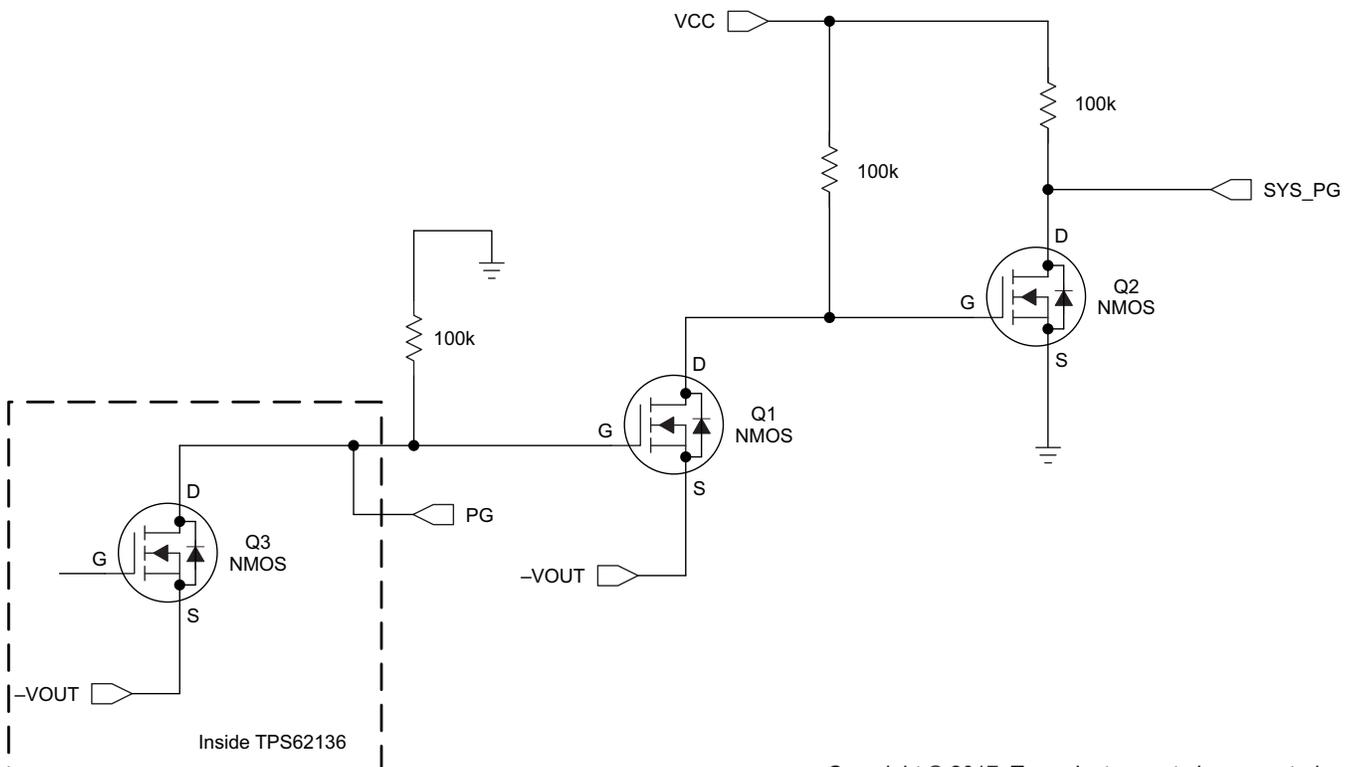
### 2.2.7 Mode Pin Configuration

The operation mode can be selected with the mode pin of the TPS62136. The device runs in automatic PFM or PWM mode when this pin is pulled low (IC ground which is  $-V_{OUT}$ ), which results in a higher efficiency at a light load. When the pin is pulled high ( $V_{IN}$ ), the device runs in forced PWM mode (for a constant frequency at a light load).

### 2.2.8 Power Good Pin Configuration

The TPS62136 has a built-in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG pin is an open-drain output that requires a pullup resistor. Because  $V_{OUT}$  is the IC ground in this configuration, the PG pin is referenced to  $V_{OUT}$  instead of ground, which means that the TPS62136 device pulls PG to  $V_{OUT}$  when it is low.

This behavior can cause difficulties in reading the state of the PG pin because, in some applications, the IC that detects the voltage level of the PG pin may not be able to withstand negative voltages. The level-shifter circuit shown in Figure 6 alleviates any difficulties associated with the offset PG pin voltages by eliminating the negative output signals of the PG pin. If the PG pin functionality is not required, it may be left floating or connected to  $V_{OUT}$  without this circuit.



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Figure 6. PG Pin Level Shifter

Inside the TPS62136, the PG pin is connected to an N-channel MOSFET (Q3). By tying the PG pin to the gate of Q1, when the PG pin is pulled low, Q1 is OFF and Q2 is ON because the  $V_{GS}$  of Q2 is at  $V_{CC}$ . SYS\_PG is then pulled to ground.

When Q3 turns OFF, the gate of Q1 is pulled to ground potential, which turns Q1 ON. This sequence of events pulls the gate of Q2 below ground, which turns it OFF. SYS\_PG is then pulled up to the  $V_{CC}$  voltage. Note that the  $V_{CC}$  voltage must be at an appropriate logic level for the circuitry connected to the SYS\_PG net.

### 3 Getting Started Hardware

To test this TI Design, simply apply an input voltage on the J1 connector and the load to J2 connector. Then, connect a jumper between ON and EN on JP1. Set JP2 to the desired operating mode, PFM (for higher efficiency at light load) or PWM (for constant frequency at light load).

### 4 Testing and Results

All data in this section has been recorded using a 3.3-V  $V_{IN}$ , -12-V  $V_{OUT}$  unless otherwise noted.

#### 4.1 Test Results

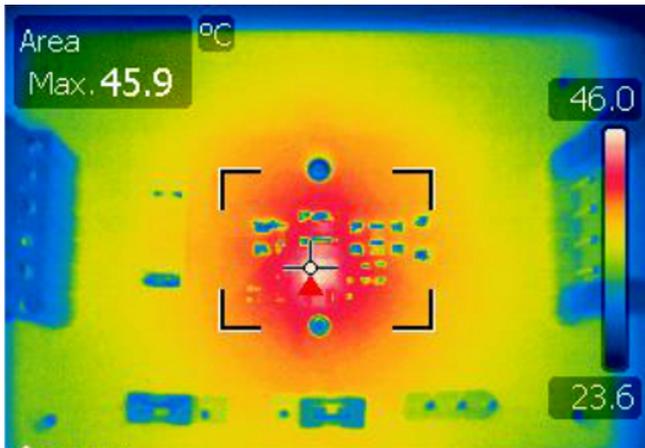


Figure 7. Thermal Performance (250-mA Load)

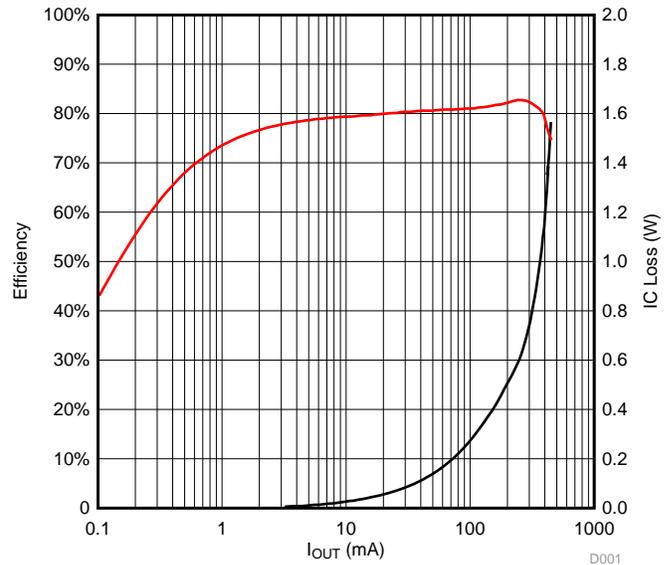


Figure 8. Efficiency Over Load (Mode = PFM)

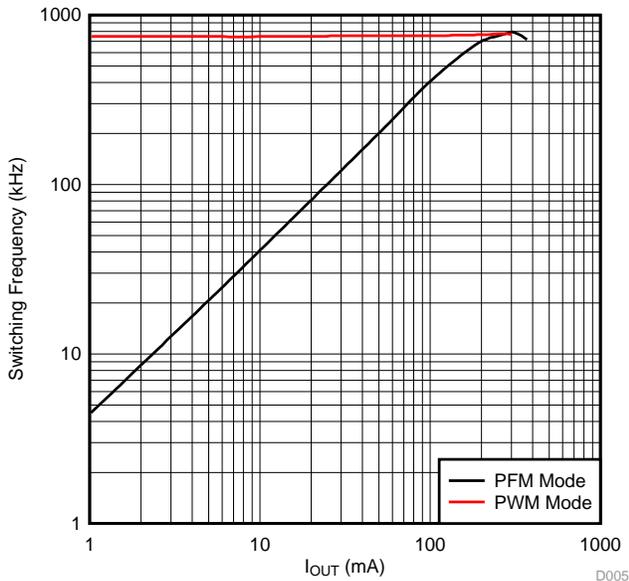


Figure 9. Switching Frequency Over Load

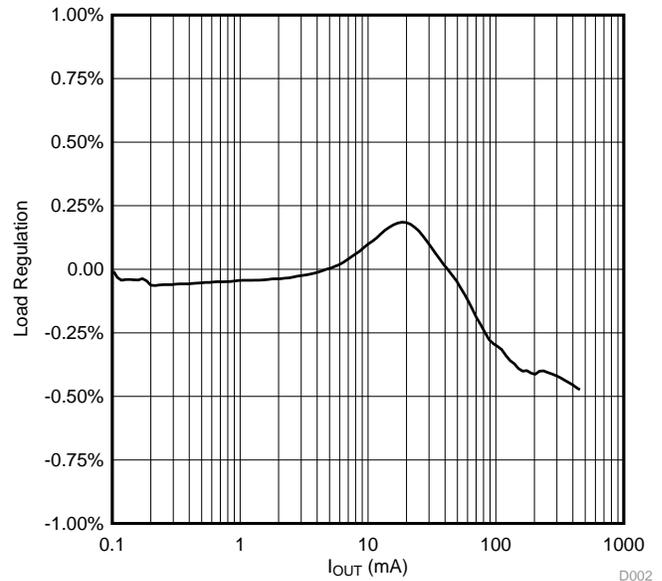


Figure 10. Load Regulation (Mode = PFM)

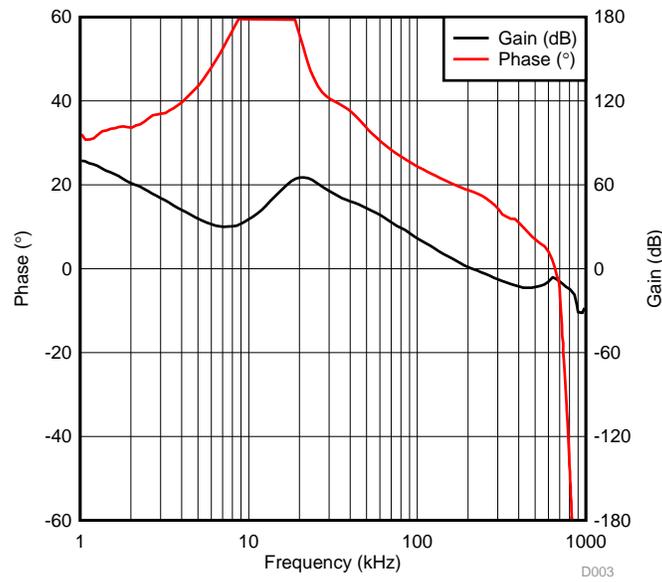


Figure 11. Loop Gain (300 mA)

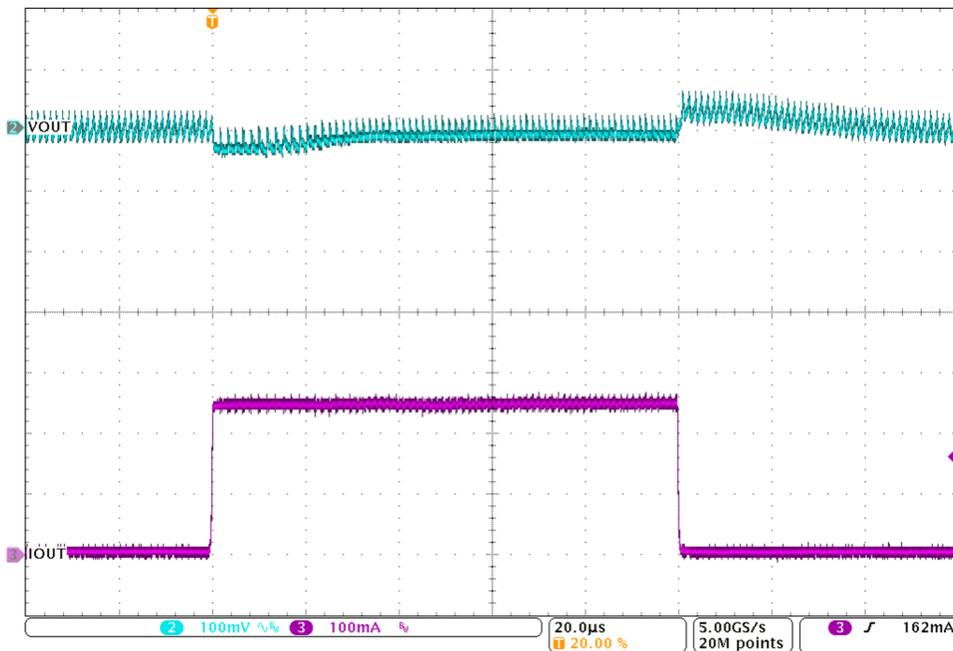


Figure 12. Transient Response (0-A to 250-mA Load Step, Mode = PWM)

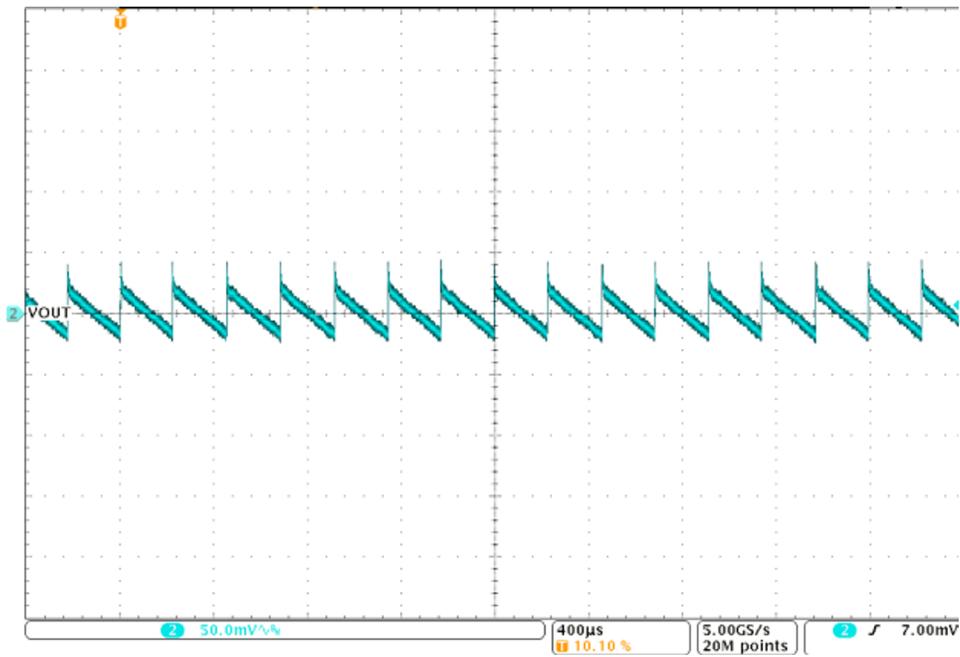


Figure 13. Output Voltage Ripple (1-mA Load, Mode = PFM)

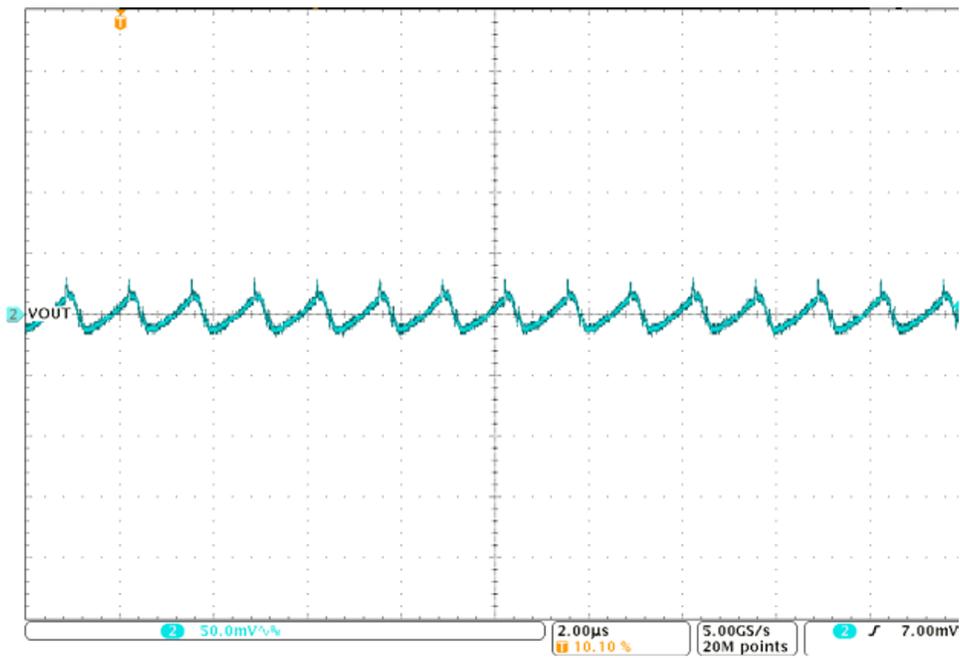


Figure 14. Output Voltage Ripple (1-mA Load, Mode = PWM)

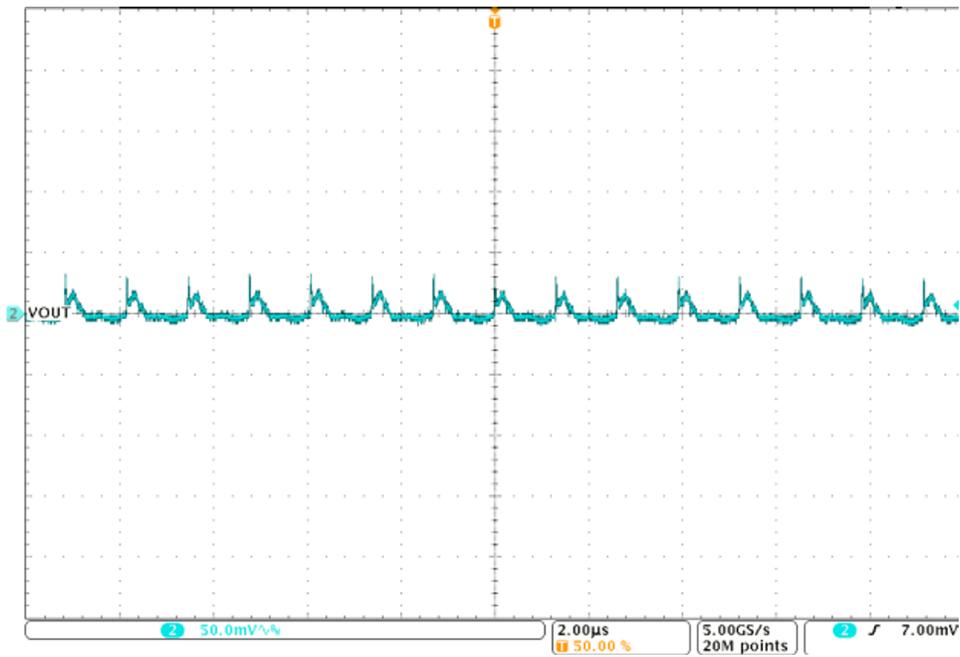


Figure 15. Output Voltage Ripple (250-mA Load)

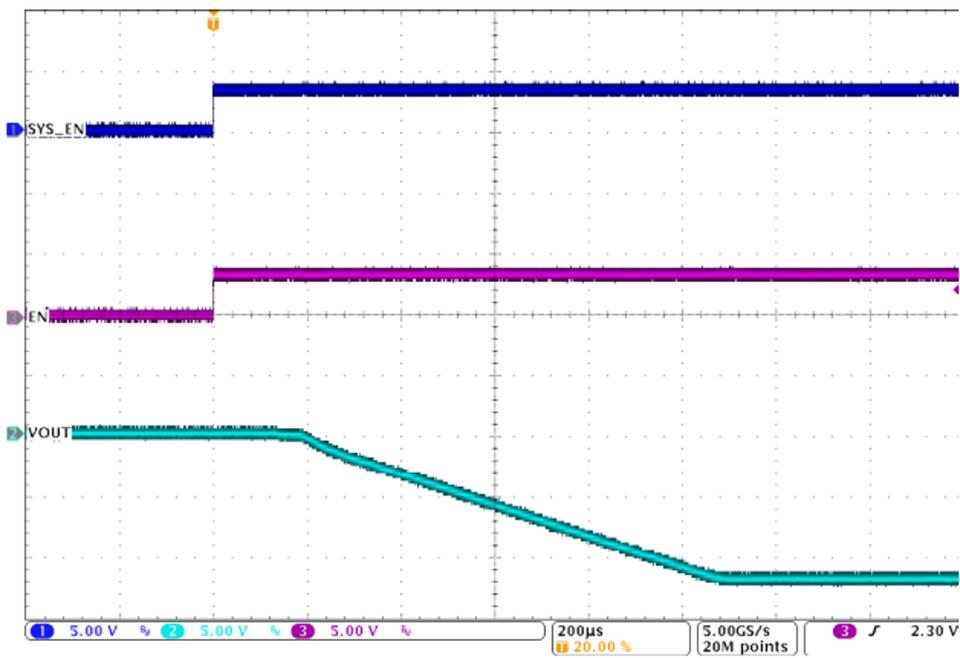


Figure 16. Start-Up on EN (No Load)

## 5 Design Files

### 5.1 Schematics

To download the schematics, see the design files at [TIDA-01423](#).

### 5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-01423](#).

### 5.3 PCB Layout Recommendations

#### 5.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-01423](#).

### 5.4 Gerber Files

To download the Gerber files, see the design files at [TIDA-01423](#).

### 5.5 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-01423](#).

## 6 Related Documentation

1. Texas Instruments, [Simplifying Stability Checks](#), Application Report (SLVA381)
2. Texas Instruments, [Using the TPS62125 in an Inverting Buck-Boost Topology](#), TPS62125 Application Report (SLVA514)
3. Texas Instruments, [TPS62136 1-MHz High Accuracy 3-V to 17-V 4-A Step-Down Converter](#), TPS62136 Data Sheet (SLVSDV2)

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