*User's Guide*

*SLVU185–September 2006*

# *TPS5410EVM-203 1-A, Regulator Evaluation Module*

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# 1 Introduction

This user's guide contains background information for the TPS5410 as well as support documentation for the TPS5410EVM-203 evaluation module (HPA203) . Also included are the performance specifications, the schematic, and the bill of materials for the TPS5410EVM-203.

## 1.1 Background

The TPS5410 dc/dc converter is designed to provide up to a 1-A output from an input voltage source of 5.5 V to 36 V. The TPS5410EVM-203 is designed using 2 independent circuits providing output voltages of 12 V and 5 V. Rated input voltage and output current range for the evaluation module is given in Table 1. This evaluation module is configured to demonstrate the flexibility of the TPS5410 regulators. The switching frequency is internally set at a nominal 500 kHz. The high-side MOSFET is incorporated inside the TPS5410 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS5410 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are provided internal to the integrated circuit (IC), whereas an external divider allows for an adjustable output voltage. Additionally, the TPS5430/31 provides an enable input. The absolute maximum input voltage is 40 V for the TPS5410EVM-203.

**Table 1. Input Voltage and Output Current Summary**

| OUTPUT VOLTAGE | INPUT VOLTAGE RANGE | OUTPUT CURRENT RANGE |
|---|---|---|
| 12 V | VIN = 14.5 V to 36 V | 0 A to 1 A |
| 5 V | VIN = 7 V to 36 V | 0 A to 1 A |

## 1.2 Performance Specification Summary

A summary of the TPS5410EVM-203 performance specifications is provided in Table 2. Specifications are given for an input voltage of VIN = 25 V and an output voltage of 12 V or 5 V, unless otherwise specified. The TPS5410EVM-203 is designed and tested for VIN = 14.5 V to 36 V for the 12 V circuit and VIN = 7 V to 36 V for the 5 V circuit. The ambient temperature is 25°C for all measurements, unless otherwise noted.

**Table 2. TPS5410EVM-203 Performance Specification Summary**

| SPECIFICATION | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| VIN voltage range | 12 V output | | | 14.5 | | 36 | V |
| | 5 V output | | | 7 | | 36 | |
| Output voltage set point | 12 V output | | | | 12.0 | | V |
| | 5 V output | | | | 5.0 | | |
| Output current range (both circuits) | | | | 0 | | 1 | A |
| Line regulation | 12 V output | $I_O$ = 0.5 A, VIN = 14.5 V – 36 V | | | ±0.05% | | |
| | 5 V output | $I_O$ = 0.5 A, VIN = 3 V – 36 V | | | ±0.09% | | |
| Load regulation | 12 V output | VIN = 25 V, $I_O$ = 0 A to 1 A | | | ±0.03% | | |
| | 5 V output | | | | ±0.03% | | |
| Load transient response | 12 V output | $I_O$ = 0.25 A to 0.75 A | Voltage change | | –110 | | mV |
| | | | Recovery time | | 150 | | µs |
| | 5 V output | | Voltage change | | –70 | | mV |
| | | | Recovery time | | 200 | | µs |
| | 12 V output | $I_O$ = 0.25 A to 0.75 A | Voltage change | | 110 | | mV |
| | | | Recovery time | | 150 | | µs |
| | 5 V output | | Voltage change | | 70 | | mV |
| | | | Recovery time | | 200 | | µs |
| Loop bandwidth | 12 V output | VIN = 25 V, $I_O$ = 0.5 A | | | 10 | | kHz |
| | 5 V output | VIN = 25 V, $I_O$ = 0.5 A | | | 17 | | |

**Table 2. TPS5410EVM-203 Performance Specification Summary (continued)**

| SPECIFICATION | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Phase margin | 12 V output | VIN = 25 V , $I_O$ = 0.5 A | | 60 | | ° |
| | 5 V output | VIN = 25 V, $I_O$ = 0.5 A | | 71 | | |
| Input ripple voltage | 12 V output | $I_O$ = 1 A | | 180 | | mVpp |
| | 5 V output | | | 50 | | |
| Output ripple voltage | 12 V output | $I_O$ = 1 A | | 15 | | mVpp |
| | 5 V output | | | 8 | | |
| Output rise time | | | | 8 | | ms |
| Operating frequency | | | | 500 | | kHz |
| Max efficiency | 12 V output | VIN = 14.5 V, $V_O$ = 12 V, $I_O$ = 0.8 A | | 96.3% | | |
| | 5 V output | VIN = 7 V, $V_O$ = 5 V, $I_O$ = 0.4 A | | 94.3% | | |

## 1.3 Modifications

These evaluation modules are designed to demonstrate the small size that can be attained when designing with the TPS5410. A few changes can be made to this module.

### 1.3.1 Output Voltage Set Point

To change the output voltage of the EVM, it is necessary to change the value of resistor R3 (12 V circuit) or R4 (5 V circuit). Changing the value of these resistors can change the output voltage above 1.25 V. The value of R for a specific output voltage can be calculated using Equation 1.

$$R2 = 10\ k\Omega \times \frac{1.221\ V}{V_O - 1.221\ V} \tag{1}$$

Table 3 lists the R values for some common output voltages. Note that VIN must be in a range so that the minimum on-time is greater than 200 ns, and the maximum duty cycle is less than 87%. The values given in Table 3 are standard values, not the exact value calculated using Equation 1.

**Table 3. Output Voltages Available**

| Output Voltage (V) | $R_2$ Value (kΩ) |
|---|---|
| 1.8 | 21.5 |
| 2.5 | 9.53 |
| 3.3 | 5.90 |
| 5 | 3.24 |

### 1.3.2 External Compensation

The TPS5410 utilizes an internally synthesized type 3 compensation network. As this compensation network is fixed, it is ideally suited for a limited range of output filter components. Both the 12 V and 5 V circuits contain additional component locations that allow the overall loop characteristics of the circuits to be modified so that output filter capacitors that would normally not be useable can be accommodated. These components are C6, C9, C12 and R1 for the 12 V circuit and C5, C10, C13 and R2 for the 5 V circuit. These components can be used to place two additional pole / zero pairs into the feedback loop. Also present are 0 Ω resistors, R5 and R7, in the feedback path of each circuit. These maybe removed to break the loop to verify the loop response if modifications are made.

The 12 V circuit on the EVM is designed using as standard type of output filter that works well with the internal compensation. The external compensation components C6, C9, C12 and R1 are left open. The 5 V circuit is designed to use ceramic output capacitors. The external compensation components are required for this design and are populated as shown in the schematic of Figure 20. For additional information on designing with ceramic or aluminum electrolytic capacitors using the TPS5410 or other wide voltage range devices, see SLVA237 *Using TPS5410/20/30/31 With Aluminum/Ceramic Output Capacitors.* It should be noted that for this design the value of the output capacitors was derated by 70 percent to account for the reduced capacitance of ceramic capacitors that have a bias voltage applied. Also, C5 is added to the circuit to improve load regulation performance. If the circuit is modified for different pole / zero locations, C5 should be chosen to be less than 1/10 the value of C13.

## 2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS5410EVM-203 evaluation module. The section also includes test results typical for the evaluation modules and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and startup.

### *2.1 Input / Output Connections*

The TPS5410EVM-203 is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 1 A should be connected to J1 and J2 for the 12 V circuit or J3 and J4 for the 5 V circuit. If both circuits are powered from the same supply, make sure that the supply is capable of supplying the full current for both circuits. The load should be connected to J5 and J6 for the 12 V output, and J7 and J8 for the 5 V output. Connections should be made using short lengths of 20 AWG wires or better to avoid losses. The maximum load current capability should be 1 A for each circuit. Each of the input and output connectors provides two pins, one for the intended connection and one provides Kelvin connection point to monitor the input and output voltages.

**Table 4. EVM Connectors and Test Points**

| Reference Designator | Function |
|---|---|
| J1 | VIN for 12 V circuit (see Table 1 for Vin range) |
| J2 | GND return for 12 V circuit VIN |
| J3 | VIN for 5 V circuit (see Table 1 for Vin range) |
| J4 | GND return for 5 V circuit VIN |
| J5 | 12 V output |
| J6 | GND return for 12 V output |
| J7 | 5 V output |
| J8 | GND return for 5 V output |
| JP1 | 2-pin header for enable of 5 V output. Connect EN to ground to disable, open to enable. |
| JP2 | 2-pin header for enable of 12 V output. Connect EN to ground to disable, open to enable. |
| TP1 | PH node of 5 V circuit |
| TP2 | PH node of 12 V circuit |
| TP3 | VSENSE node of 12 V output |
| TP4 | VSENSE node of 5 V output |
| TP5 | Test point between voltage divider network and R5. Used for loop response measurements of 12 V circuit. |
| TP6 | Test point between voltage divider network and R7. Used for loop response measurements of 5 V circuit. |

## 2.2 Efficiency

The efficiency for both EVM output voltages peak at a load current of about 0.75 A, and then decrease as the load current increases towards full load. Figure 1 shows the efficiency for the 12 V output at an ambient temperature of 25°C.

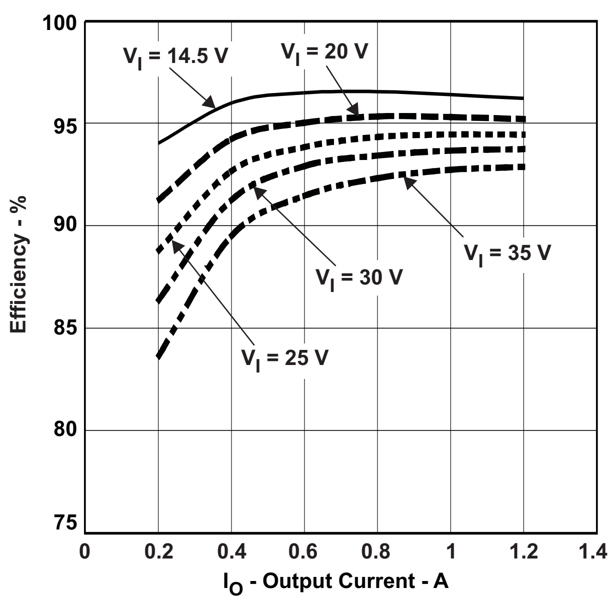



**Figure 1. TPS5410 12 V Output Efficiency**

Figure 2 shows the efficiency for the 5 V output at an ambient temperature of 25°C.

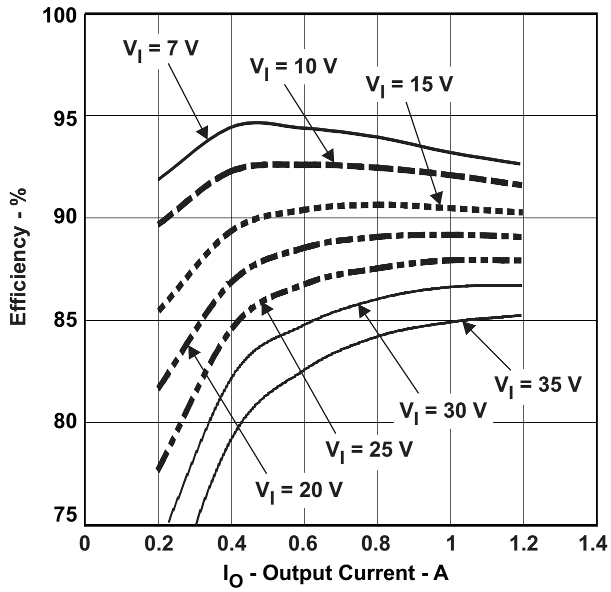



**Figure 2. TPS5410 5 V Output Efficiency**

The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs.

## 2.3 Output Voltage Load Regulation

The load regulation for the 12 V and 5 V outputs are shown in Figure 3 and Figure 4.

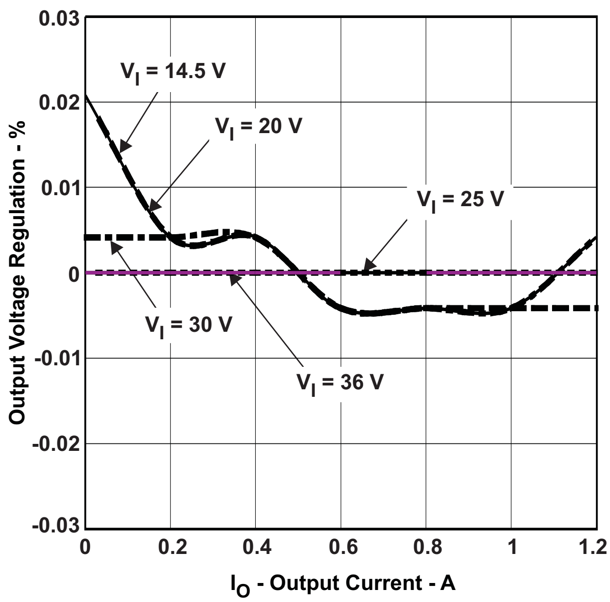



**Figure 3. TPS5410 12 V Output Load Regulation**

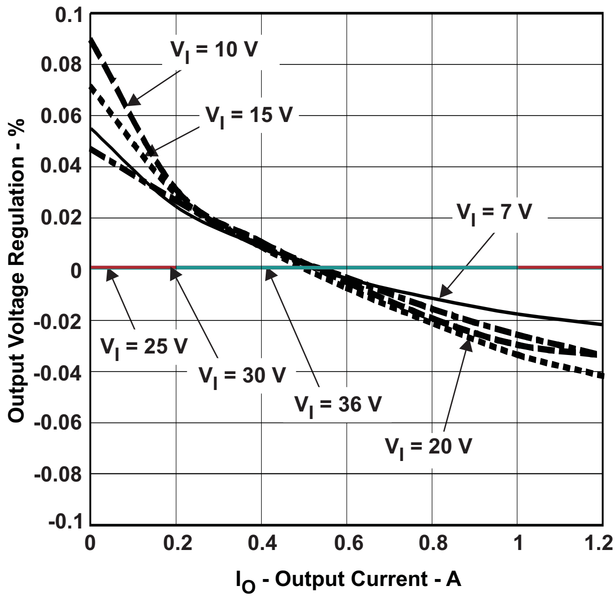



**Figure 4. TPS5410 5 V Output Load Regulation**

Measurements are given for an ambient temperature of 25°C.

## 2.4 Output voltage Line Regulation

The line regulation for the 12 V and 5 V outputs are shown in Figure 5 and Figure 6.

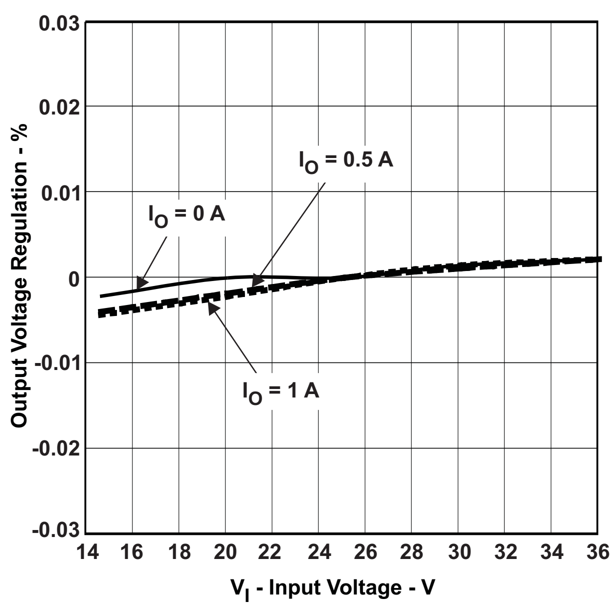



**Figure 5. TPS5410 12 V Output Line Regulation**

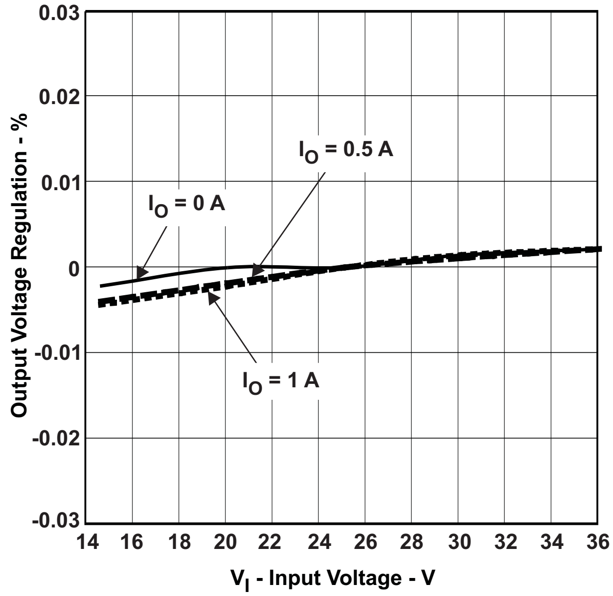



**Figure 6. TPS5410 5 V Output Line Regulation**

## 2.5 Load Transients

The 12 V and 5 V circuit response to load transients is shown in Figure 7 and Figure 8. The current step is from 25% to 75% of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

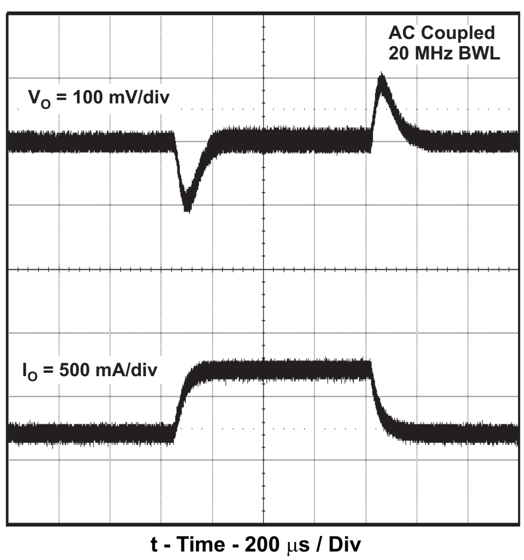



**Figure 7. TPS5410 12 V Output Transient Response**

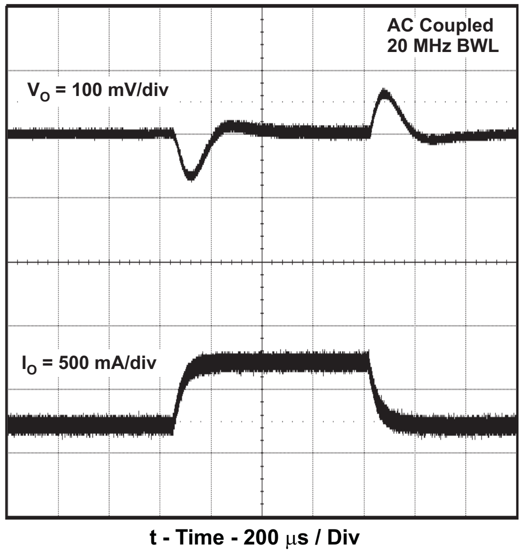



**Figure 8. TPS5410 5 V Output Transient Response**

## 2.6 Loop Characteristics

The 12 V and 5 V output loop-response characteristics are shown in Figure 9 and Figure 10. Gain and phase plots are shown for VIN voltage of 25 V. Load current for both measurements is 0.5 A.

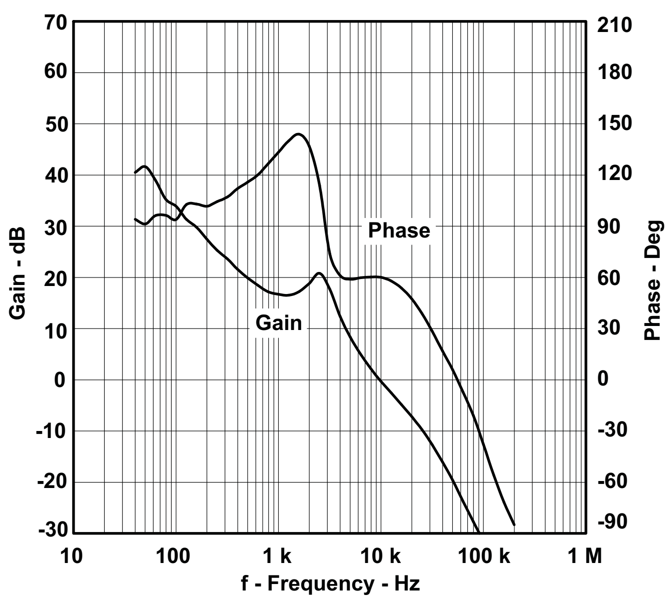



**Figure 9. TPS5410 12 V Output Loop Response**

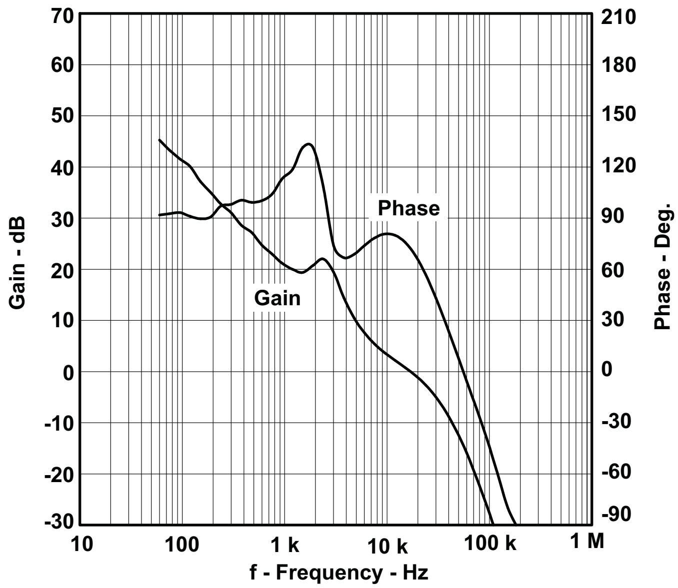



**Figure 10. TPS5410 5 V Output Loop Response**

## 2.7 *Output Voltage Ripple*

The 12 V and 5 V output voltage ripple is shown in Figure 11 and Figure 12 . The output current is the rated full load of 1 A. Voltage is measured directly across output capacitors.

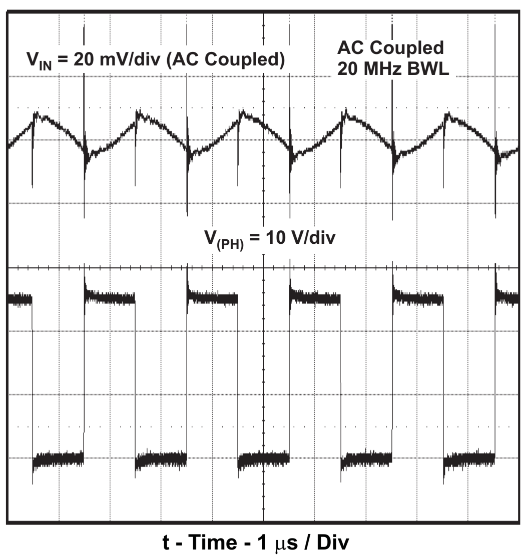



**Figure 11. TPS5410 12 V Output Ripple**

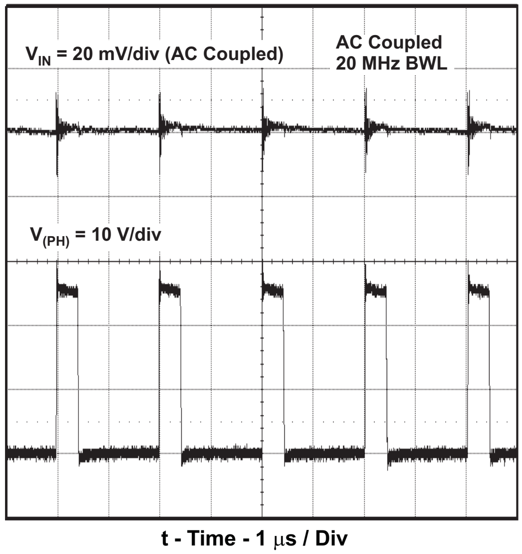



**Figure 12. TPS5410 5 V Output Ripple**

## 2.8 Input Voltage Ripple

The 12 V and 5 V input voltage ripple is shown in Figure 13 and Figure 14. The output current for each device is at full rated load of 1 A.

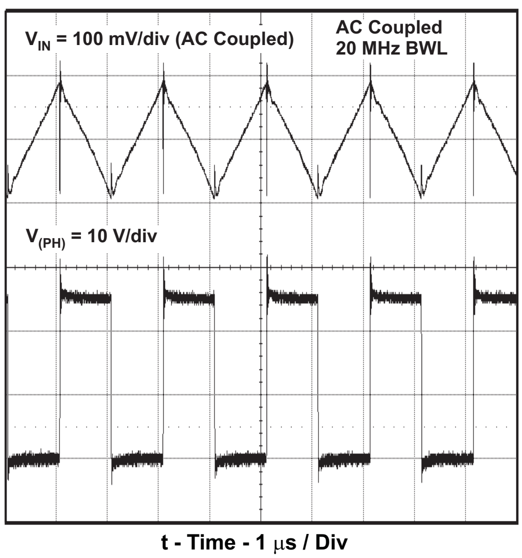



**Figure 13. TPS5410 12 V Input Ripple**

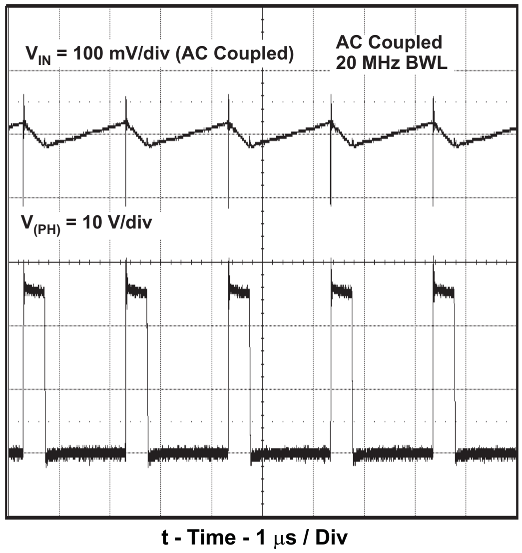



**Figure 14. TPS5410 5 V Input Ripple**

## 2.9 Powering Up

The start-up waveforms are shown in Figure 15 and Figure 16. In Figure 15, the top trace shows ENA, and the bottom trace shows Vout for the 12 V circuit. Initially, the output is inhibited by using a jumper at JP2 to tie ENA to GND. When the jumper is removed, ENA is released. When the ENA voltage reaches the enable-threshold voltage of 1.06 V, the start-up sequence begins and the internal reference voltage begins to ramp up at the internally set rate towards 1.221 V and the output voltage ramps up to the externally set value of 12 V. Figure 16 shows the start-up waveform relative to the input voltage. With the ENA pin open, the input voltage is applied to the circuit. When the UVLO threshold is reached, the start up sequence begins and the internal reference voltage begins to ramp up at the internally set rate towards 1.221 V and the output voltage ramps up to the externally set value of 12 V. The start up waveforms are similar for the 5 V circuit.

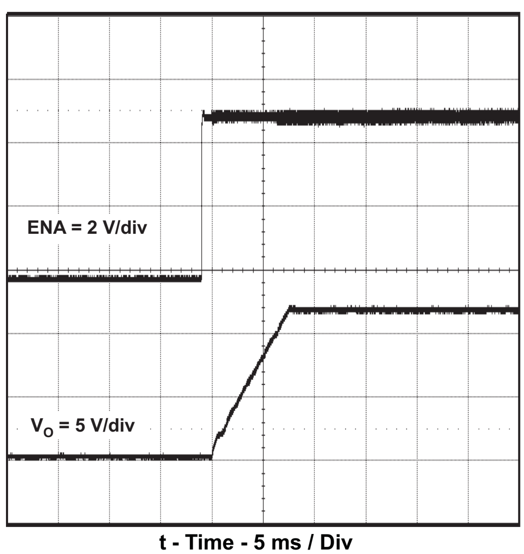



**Figure 15. TPS5410 Start-Up, ENA and $V_O$**

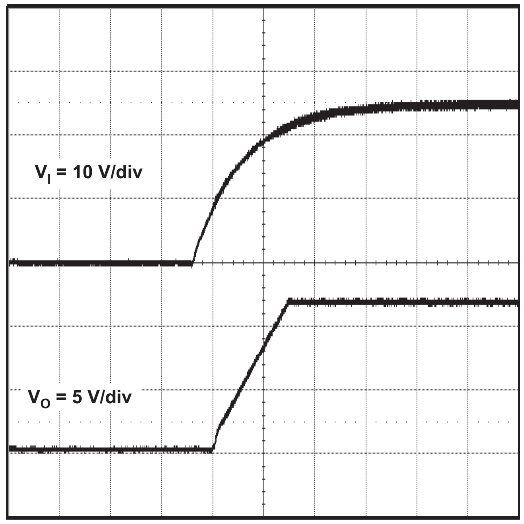



**Figure 16. Startup Waveform, $V_I$ and $V_O$**

## 3 Board Layout

This section provides a description of the TPS5410EVM-203 board layout and layer illustrations.

### 3.1 Layout

The board layout for the TPS5410EVM-203 is shown in Figure 17 through Figure 19. The topside layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz. copper.

The top layer contains the main power traces for VOUT, and VPH for both circuits. Also on the top layer are connections for the remaining pins of each TPS5410 and a large ground traces. The bottom layer contains the input voltage traces, routes for the ENA feature and VSENSE traces for both circuits. Although the two circuits are independent, the ground traces are connected together with a trace on the top side.

The input decoupling capacitors (C1 and C2) and bootstrap capacitors (C3 and C4) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper Vout trace at the output connector.

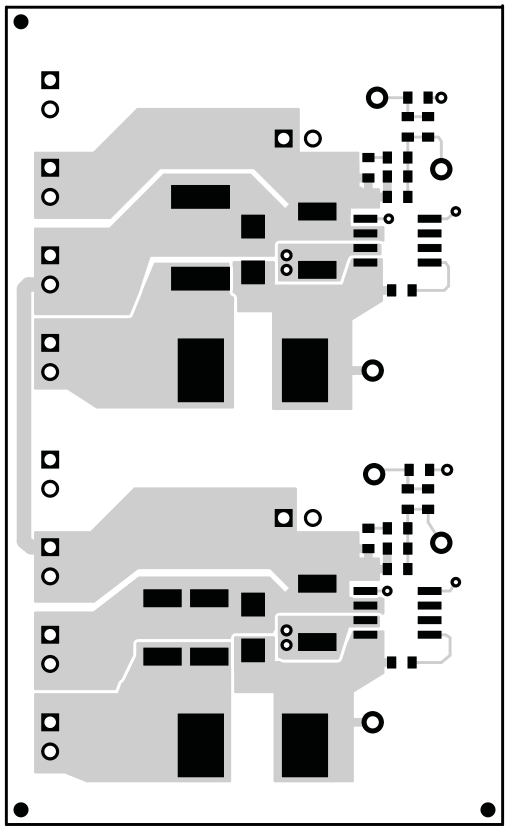


**Figure 17. Top-Side Layout**

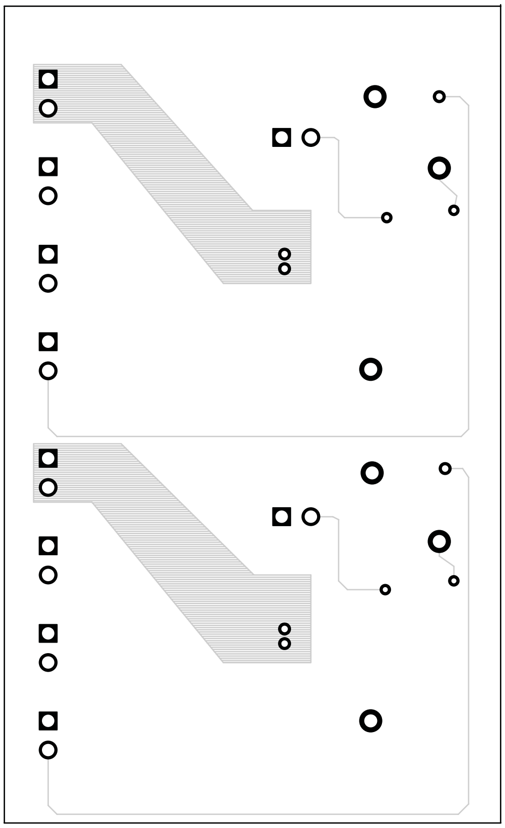


Figure 18. Bottom-Side Layout (Looking From Top Side)

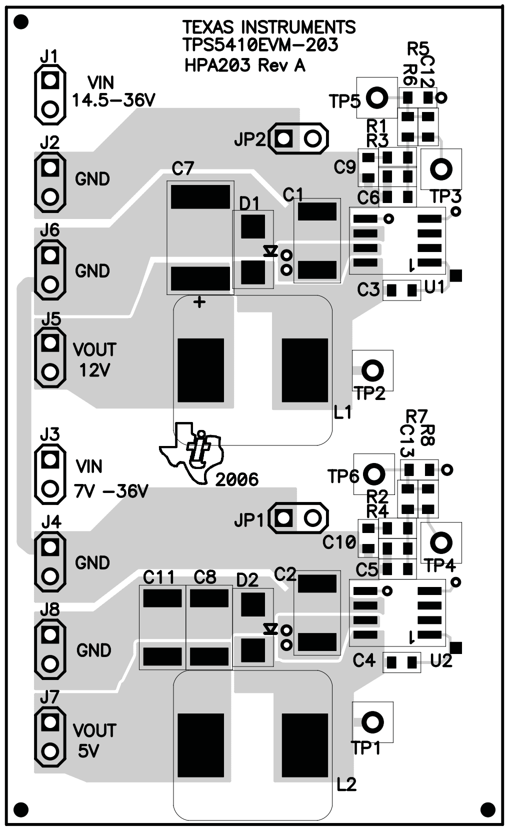


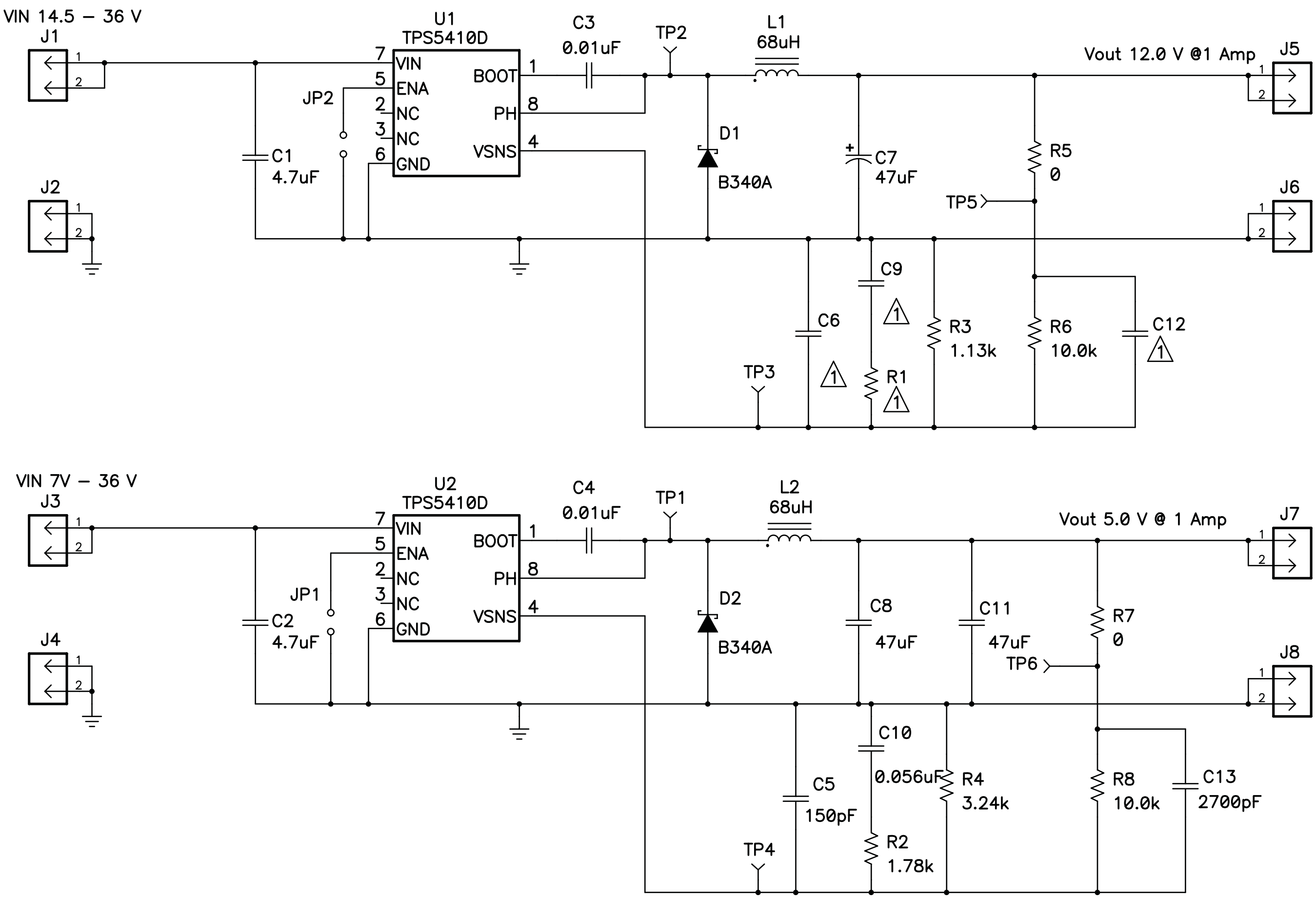

**Figure 19. Top-Side Assembly**

# 4 Schematic and Bill of Materials

The TPS5410EVM-203 and TPS5431EVM-173 schematic and bill of materials are presented in this section.

## 4.1 Schematic

The schematic for the TPS5410EVM-203 is shown in Figure 20.




(1) Not used.

**Figure 20. TPS5410EVM-203 Schematic**

## 4.2 Bill of Materials

The bill of materials for the TPS5410EVM-203 is given by Table 5.

**Table 5. Bill of Materials**

| | | | HPA203A BOM | | | |
|---|---|---|---|---|---|---|
| | | | | | | |
| **COUNT** | **RefDes** | **Value** | **DESCRIPTION** | **SIZE** | **Part Number** | **MFR** |
| 2 | C1, C2 | 4.7uF | Capacitor, Ceramic, 50V, X5R, 20% | 1812 | C4532X5R1H475MT | TDK |
| 1 | C10 | 0.056uF | Capacitor, Ceramic, 25V, X7R, 10% | 0603 | ECJ-1VB1E563K | Panasonic |
| 1 | C13 | 2700pF | Capacitor, Ceramic, 50V, C0G, 5% | 0603 | C1608C0G1H272J | TDK |
| 2 | C3, C4 | 0.01uF | Capacitor, Ceramic, 50V, X7R, 10% | 0603 | C1608X7R1H103K | TDK |
| 1 | C5 | 150pF | Capacitor, Ceramic, 50V, C0G, 5% | 0603 | C1608C0G1H151J | TDK |
| 0 | C6, C9, C12 | Open | Capacitor, Ceramic, xxV | 0603 | | |
| 1 | C7 | 47uF | Capacitor, Tantalum, 20V, | 7343 (D) | TPSE476M020R0150 | AVX |
| 2 | C8, C11 | 47uF | Capacitor, Ceramic, 10V, X5R, 20% | 1812 | C4532X5R1A476MT | TDK |
| 2 | D1, D2 | | Diode, Schottky, 3A, 40V | SMA | B340A | Diodes Inc |
| 8 | J1- J8 | | Header, 2 pin, 100mil spacing, (36-pin strip) | 0.100 x 2 | PTC36SAAN | |
| 2 | JP1, JP2 | | Header, 2 pin, 100mil spacing, (36-pin strip) | 0.100 x 2 | PTC36SAAN | Sullins |
| 2 | L1, L2 | 68uH | Inductor, SMT, 2.3A, 130milliohm | 0.484 x 0.484 | MSS1260-683MLB | Coilcraft |
| 0 | R1 | Open | Resistor, Chip, 1/16W, yy% | 0603 | | |
| 1 | R2 | 1.78k | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| 1 | R3 | 1.13k | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| 1 | R4 | 3.24k | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| 2 | R5, R7 | 0 | Resistor, Chip, 1/16W, 5% | 0603 | Std | Std |
| 2 | R6, R8 | 10.0k | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| 6 | TP1 - TP6 | | Test Point, Red, Thru Hole Color Keyed | 0.100 x 0.100 | 5000 | Keystone |
| 2 | U1, U2 | | IC, Switching Step-Down Regulator, 5.5V-36V, 1A | SO8 | TPS5410D | TI |
| 1 | -- | | PCB, 2.8 In x 1.7 In x 0.062 In | | HPA203 | Any |
| 2 | -- | | Shunt, 100mil, Black | 0.100 | 929950-00 | 3M |

## EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

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## REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

**General Statement for EVMs including a radio**

*User Power/Frequency Use Obligations*: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

**For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant**

**Caution**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

**FCC Interference Statement for Class A EVM devices**

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

**FCC Interference Statement for Class B EVM devices**

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

**For EVMs annotated as IC – INDUSTRY CANADA Compliant**

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment.

**Concerning EVMs including radio transmitters**

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

**Concerning EVMs including detachable antennas**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l’autorité de l'utilisateur pour actionner l'équipement.

**Concernant les EVMs avec appareils radio**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**Concernant les EVMs avec antennes détachables**

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d’usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

## 【Important Notice for Users of EVMs for RF Products in Japan】

**This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan**

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

**Texas Instruments Japan Limited**
**(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan**

http://www.tij.co.jp

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】

本開発キットは技術基準適合証明を受けておりません。

本製品のご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。

日本テキサス· インスツルメンツ株式会社
東京都新宿区西新宿６丁目２４番１号
西新宿三井ビル
http://www.tij.co.jp

## EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMERS

**For Feasibility Evaluation Only, in Laboratory/Development Environments.** Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM’s electronic components and packing materials.

**Certain Instructions**. It is important to operate this EVM within TI’s recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

**Agreement to Defend, Indemnify and Hold Harmless.** You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

**Safety-Critical or Life-Critical Applications.** If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265