MAXWELL SERDES PCIe x2 PERSONALITY CARD

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REV	A
VER	1.0

Designed for TI by Mistral Solutions Pvt Ltd

TEXAS INSTRUMENTS

MISTRAL

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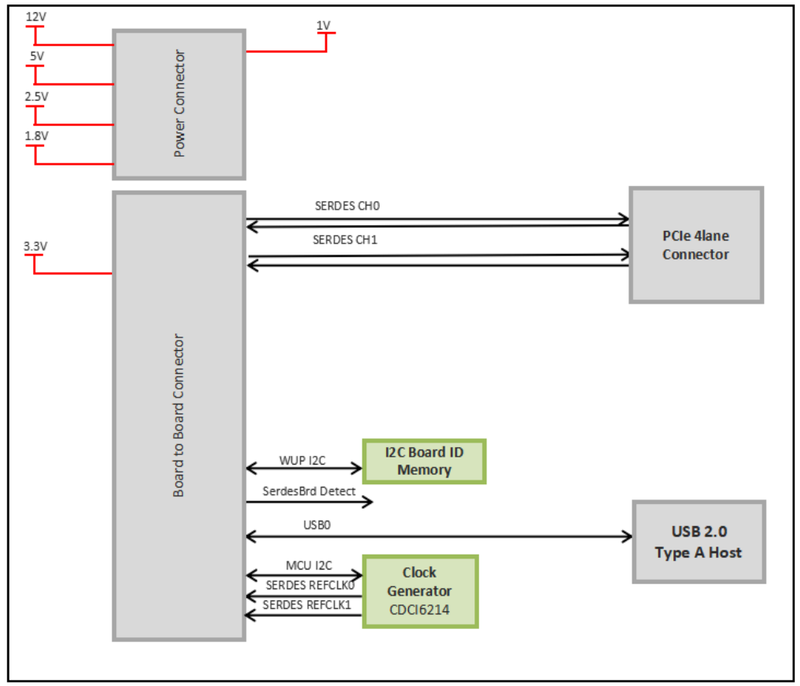
REVISION HISTORY

REV #	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
A	0.1	31th JAN 2020	Drafted from Rev E3, Ver 1.0 schematics.	Mistral Design Team	AJIT MB	AJIT MB
A	0.2	31th JAN 2020	Made R247 as DNI	Mistral Design Team	AJIT MB	AJIT MB
A	0.3	20th FEB 2020	Updated alternate components	Mistral Design Team	AJIT MB	AJIT MB
A	1.0	20th MAR 2020	Baselined	Mistral Design Team	AJIT MB	AJIT MB

BLOCK DIAGRAM



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Title	BLOCK DIAGRAM	
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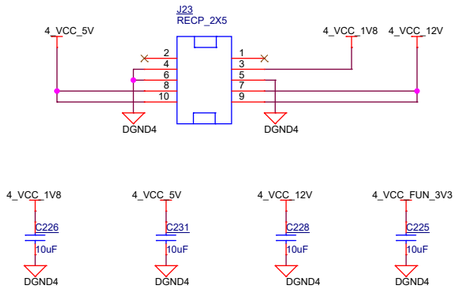
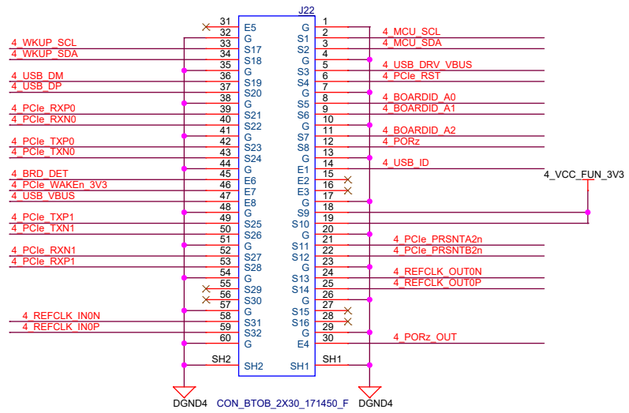
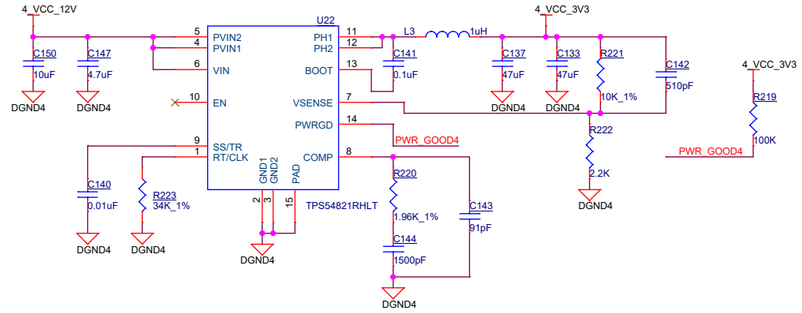
Power Connector



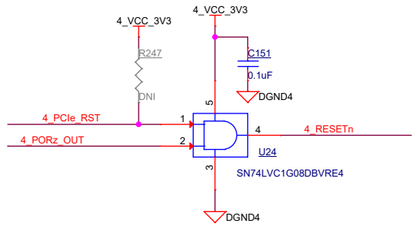
Serdes Connector

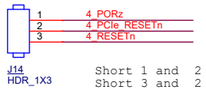


12V to 3.3V @ 6.5A Supply

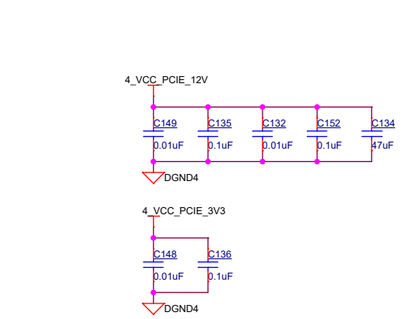


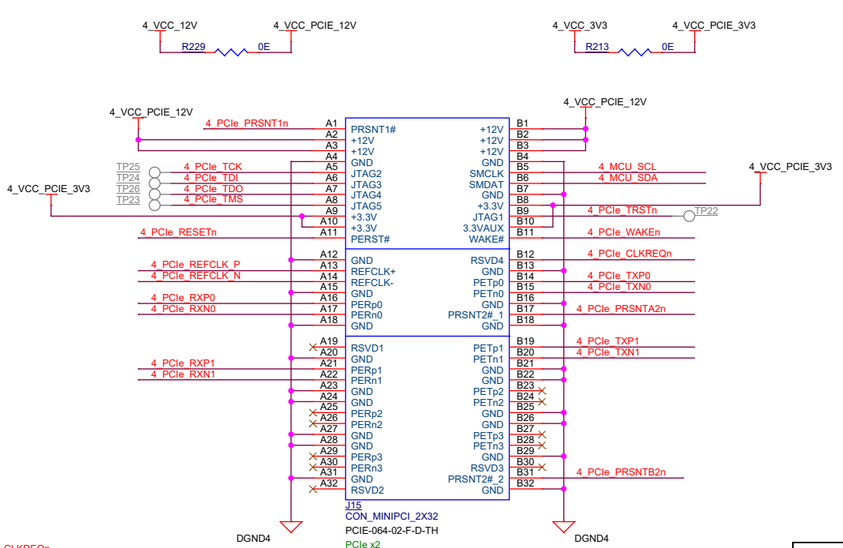
PCIe Reset

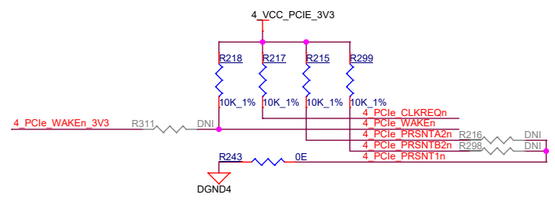




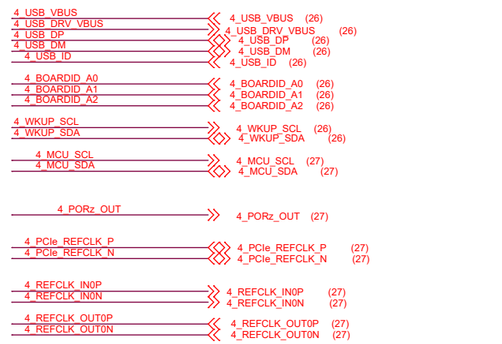
x4 Lane PCIe Connector







Do Not Mount R216 and R298 for Host operation
Mount R229, R213, R215, R299 and R243 for Host operation
Do Not Maount R229, R213, R215, R299 and R243 for Device operation
Mount R216 and R298 for Device operation



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Title	2LANEPCIe_SERDES & PCIE CON	
Size: C	PROC067A SER PCIE2LEVM	Rev: A
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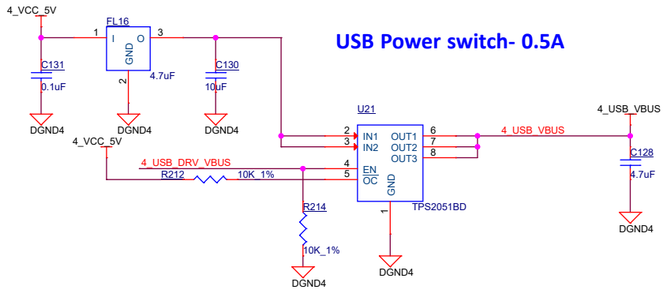
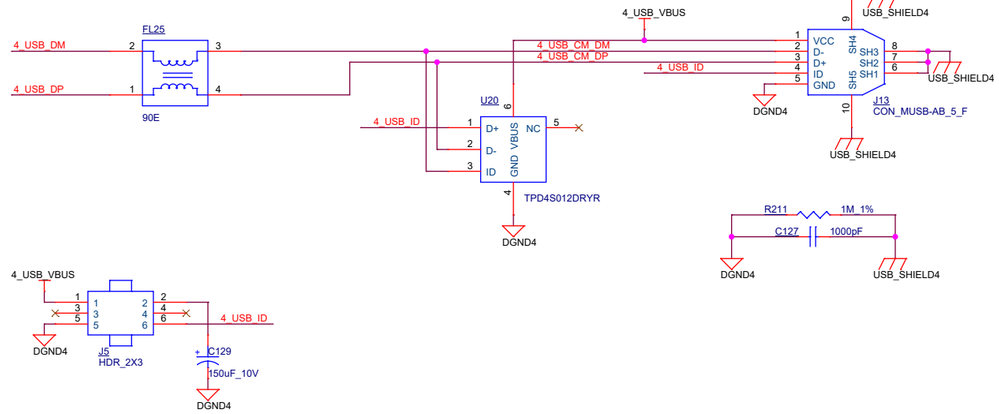
USB 2.0

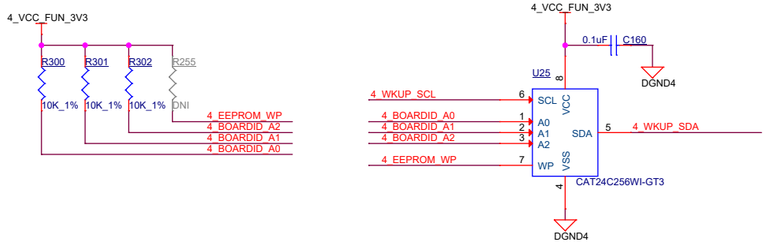
USB Power switch- 0.5A



USB 2.0 micro AB Connector



BOARD ID EEPROM



I2C address: 0x54h or Set by host

4_BOARDID_A0 → 4_BOARDID_A0 (25)
4_BOARDID_A1 → 4_BOARDID_A1 (25)
4_BOARDID_A2 → 4_BOARDID_A2 (25)

4_USB_ID → 4_USB_ID (25)
4_USB_VBUS → 4_USB_VBUS (25)
4_USB_DRV_VBUS → 4_USB_DRV_VBUS (25)
4_USB_DP → 4_USB_DP (25)
4_USB_DM → 4_USB_DM (25)

4_WKUP_SCL → 4_WKUP_SCL (25)
4_WKUP_SDA → 4_WKUP_SDA (25)

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Title	2LANEPCIE_USB2.0 &BRD_ID	
Size: C	PROC067A SER PCIE2LEVM	Rev: A
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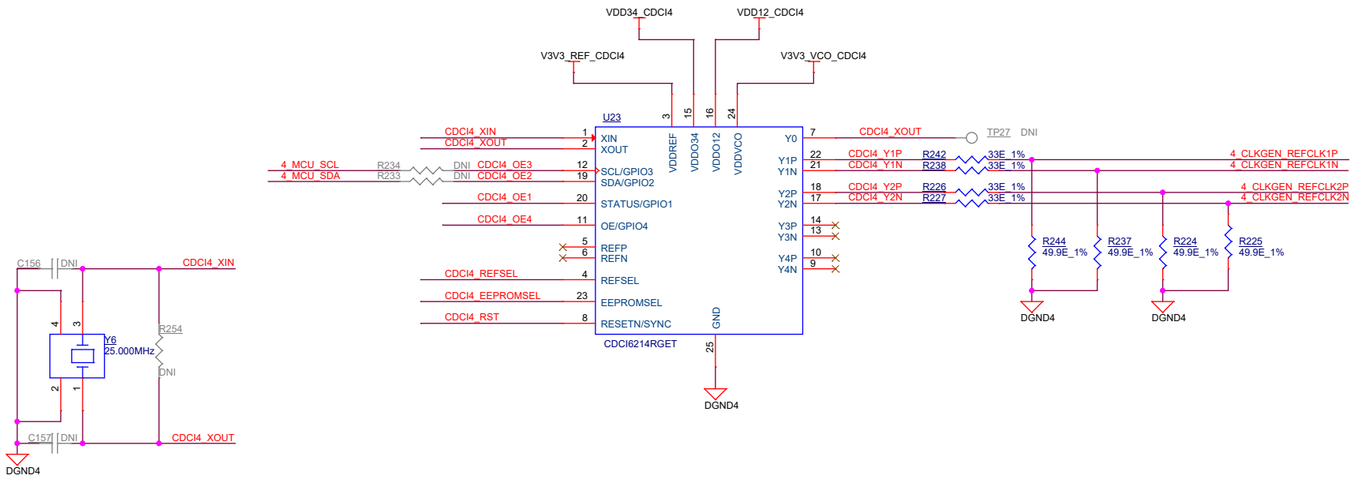
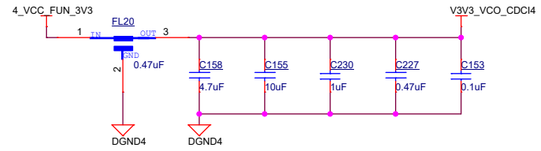
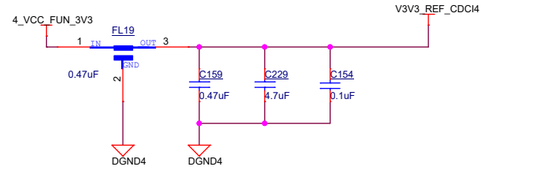
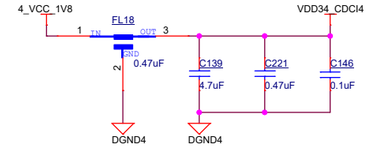
2 Lane PCIe Clock HCSL (100MHz) (EEPROM PAGE 0)

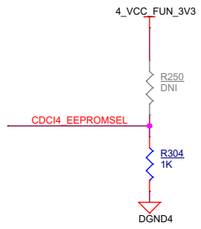


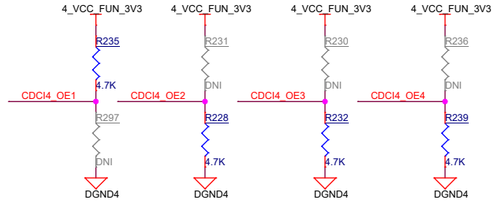


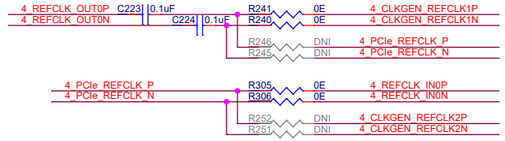


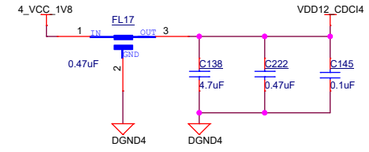


CLOCK ROOT SELECTION

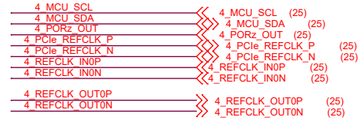








REFCLK_OUTxP	SoC Input Clock
REFCLK_OUTxN	
CLKGEN_REFCLKxP	Output Clock of Clock Generator
CLKGEN_REFCLKxN	
REFCLK_INxP	SoC Output Clock
REFCLK_INxN	
PCIe_REFCLKx_P	PCIe connector Clock lines
PCIe_REFCLKx_N	



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Title	2LANEPCIE_CLK	
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HARDWARE SCHEMATICS

SCREWS and WASHER's

MH1 MH2 MH3 MH4 MH5

29300 29300 29300 29300 29300

ACC3 ACC4 ACC5 ACC6 ACC7 ACC8 ACC9

4692 4692 4692 4692 4692 4692 4692

These mechanicals will be used to secure this board to PROC062

JUMPERs

ACC1

MNT-103-BK-G

To be mounted on J5 for USB Host operation.

ACC2

SPC02SYAN

To be mounted on J14 pin 3 and 2 for Host operation.

FIDUCIALS

FID1 DNI FID2 DNI FID3 DNI

FID4 DNI FID5 DNI FID6 DNI

LOGOs

PCB LOGO DNI — Texas Intruments

PCB LOGO DNI — For Evaluation only; not FCC approved for resale

PCB LOGO DNI — WEEE Mark

PCB LOGO DNI — CE Mark

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

LABEL

Assembly Revision

LBL1

PCB LABEL

THT-103-423-10

Board Serial No.

LBL2

PCB LABEL

THT-103-423-10

BARE PCB

PCB1

PROC067

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Title	HARDWARE SCHEMATICS		
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