AM243x LAUNCH PAD

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REV	E3
VER	1.0

Designed for TI by Mistral Solutions Pvt Ltd

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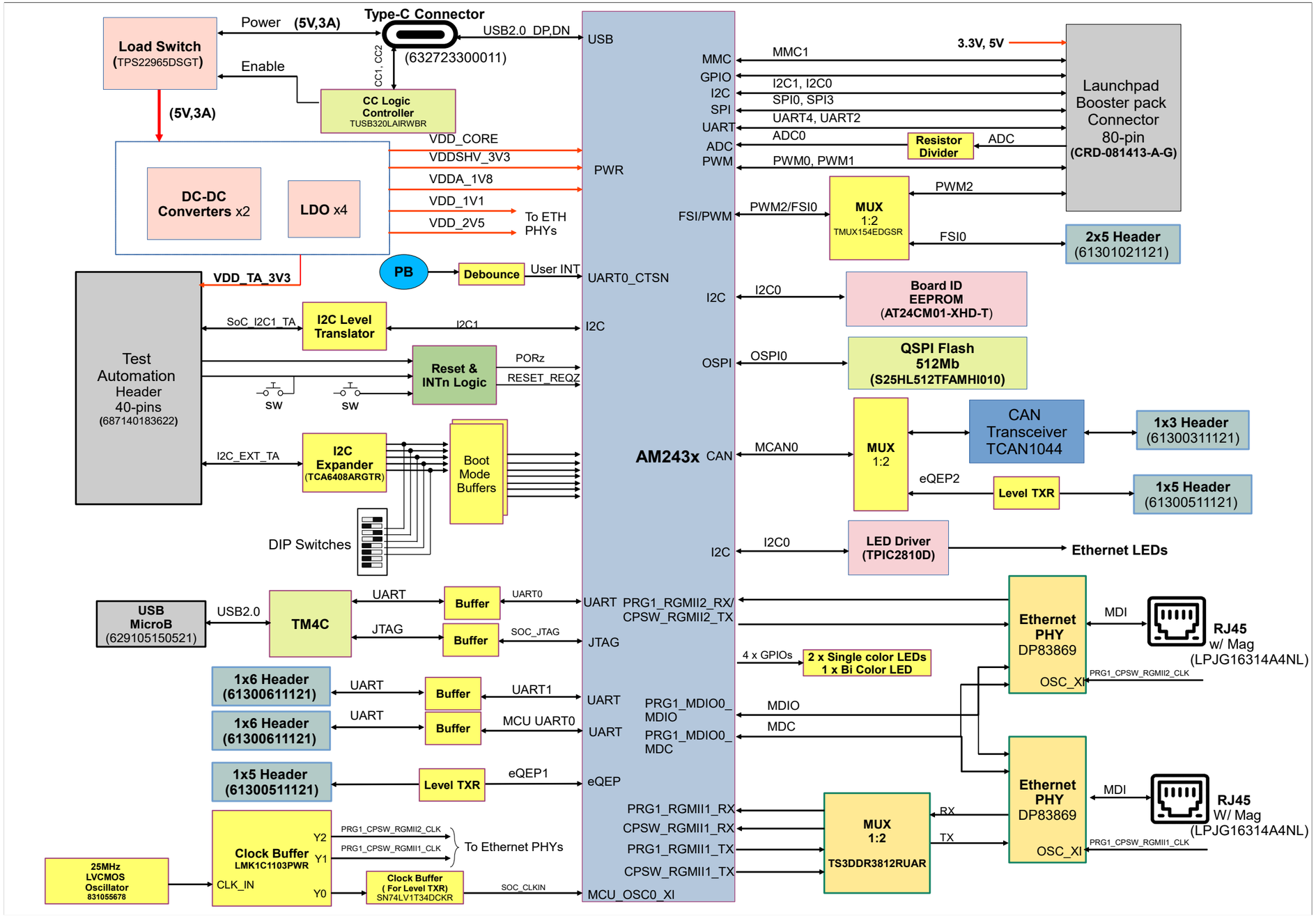
REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	10th AUG 2021	Drafted from PROC109E2 v1.0	Mistral Design Team		
0.2	10th AUG 2021	1. RJ45 Connector's J18 and J19 Mfr. Part No. changed from 7499111614A (Wurth Electronics) to LPJG16314A4NL (Link-PP) with common center tap. Removed the capacitors C164, C195, C261, C264, C83, C89, C115 & C127 2. Ethernet PHY1(U19) RX link indication signal "PRG1_CPSW_ETH1_LED_LINK" is connected to SoC GPIO signal "PRG1_PRU0_GPO8 ". VPP_1V8_REG_EN signal from SoC GPIO Signal PRG1_PRU0_GPO8 is removed. Added Pull UP resisitor (R593) and 2x1 (J22) header for enable option of VPP supply. 3. Ethernet PHY2 (U7) RX link indication Signal "PRG1_CPSW_ETH2_LED_LINK" is connected to SoC GPIO signal "PRG1_PRU1_GPO8". And the net "GPIO_RGMII1_PHY_RSTn" is moved to GPMC0_AD11. USER_LED1 ciricuit (R18, R38, Q2 & LD5) is removed. 4. Ethernet PHY1(U19) RX ERROR Status signal "PRG1_CPSW_ETH1_LED_1000/RX_ER" is connected to SoC GPIO signal "PRG1_PRU0_GPO5". And the net "GPIO_50" is removed from Boosterpack header J5 Pin11. 5. Ethernet PHY2 (U7) RX ERROR Status signal "PRG1_CPSW_ETH2_LED_1000/RX_ER" is connected to SoC GPIO signal "PRG1_PRU1_GPO5". And the signal "PRG_CPSW_RGMII1_MUX_SEL" is moved to GPMC0_AD12. USER_LED2 circuit (R7, R14, Q1 & LD4) is removed. 6. PRG1_CPSW_ETH1_LED_ACT and PRG1_CPSW_ETH2_LED_ACT is connected to SoC GPIOs PRG1_PRU0_GPO9 & PRG1_PRU1_GPO9 respectively using R-Mux.	Mistral Design Team		
0.3	11th AUG 2021	Updated for Internal Review comments	Mistral Design Team		
0.4	19th AUG 2021	1. The net "GPIO_RGMII1_PHY_RSTn" is moved from GPMC0_AD11 to GPMC0_AD13. 2. The net "FSI/BP_MUX_SEL" is moved from GPMC0_AD13 to GPMC0_AD11.And the resistor R190 is DNI'd.	Mistral Design Team		
0.5	08th NOV 2021	1. Isolation Buffer for Bootmode Input pins 'U32' Mfr. Part No. changed from SN74AVC8T245PWR to TXB0106PWR. 2. Removed the IC U29 (SN74LVC1G04DCK) and capacitor C87. 3.BOOTMODE0's Pull up Resistor R39 value changed from 10K to 49.9K BOOTMODE2's, BOOTMODE10's Pull down Resistor R206, R205 respectively value changed from 10K to 49.9K.	Mistral Design Team		
0.6	15th NOV 2021	1. The Resistor R160 value changed from '1M' to '0E' and the capacitor C266 is DNI'd	Mistral Design Team		

BLOCK DIAGRAM



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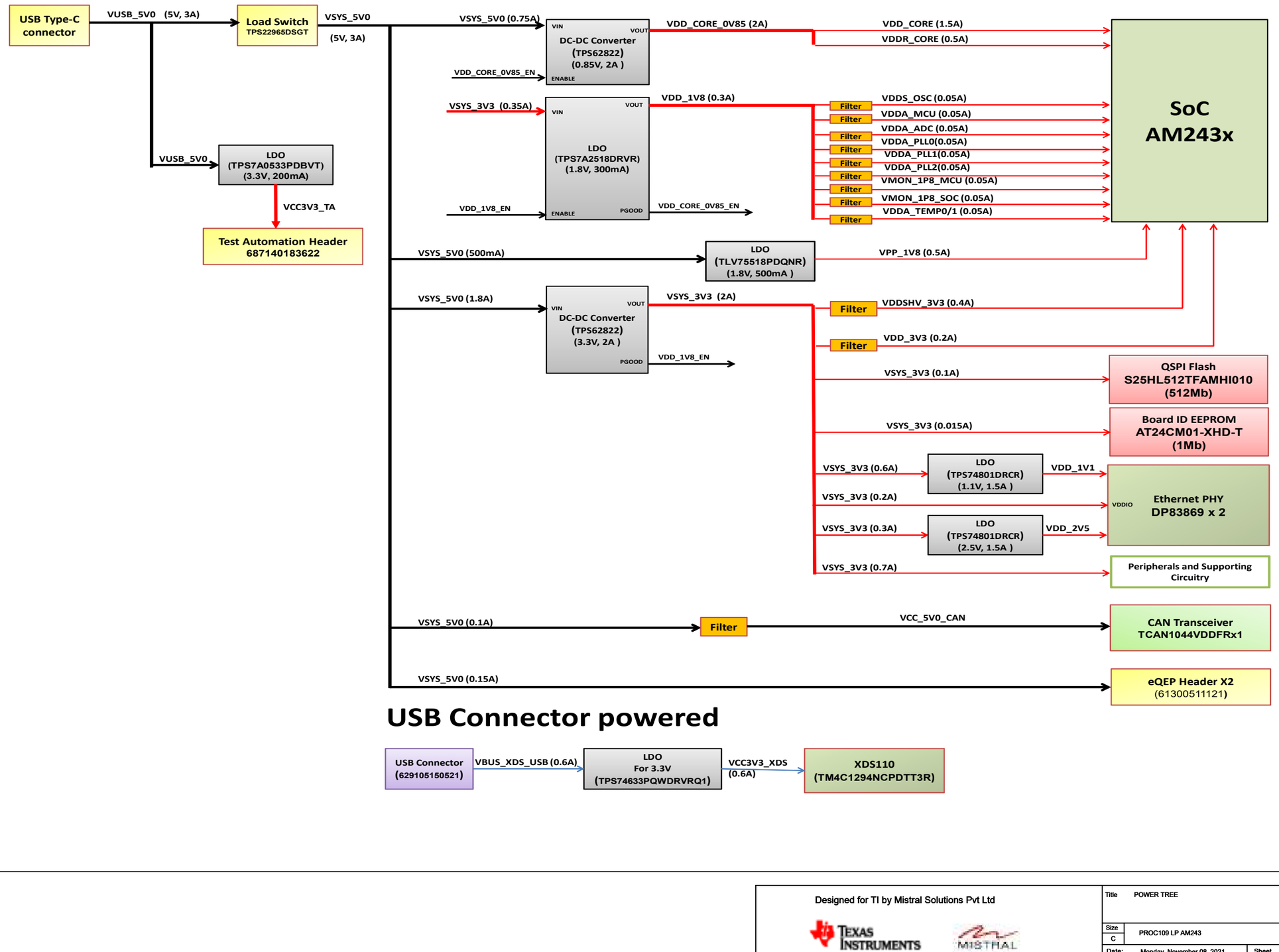
POWER TREE



USB Connector powered

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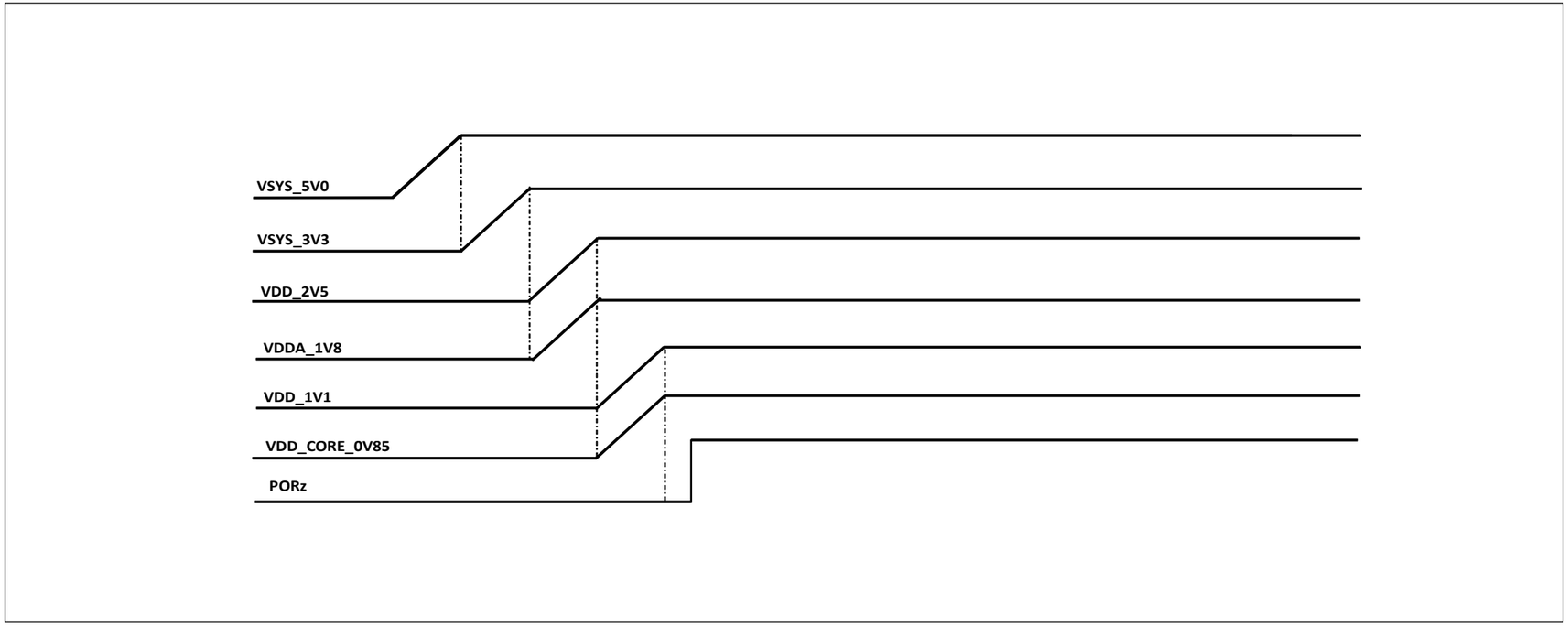
POWER ON SEQUENCE



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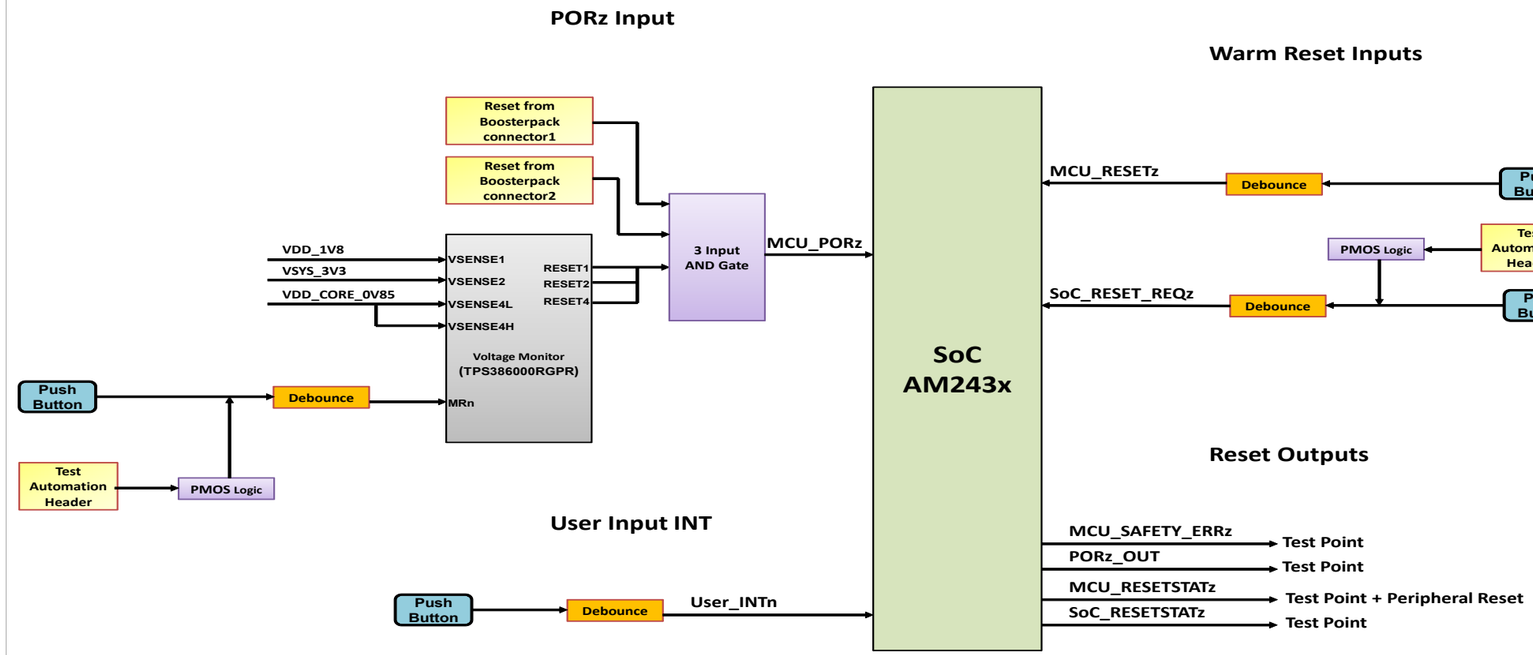
RESET ARCHITECTURE



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Title	RESET ARCHITECTURE		
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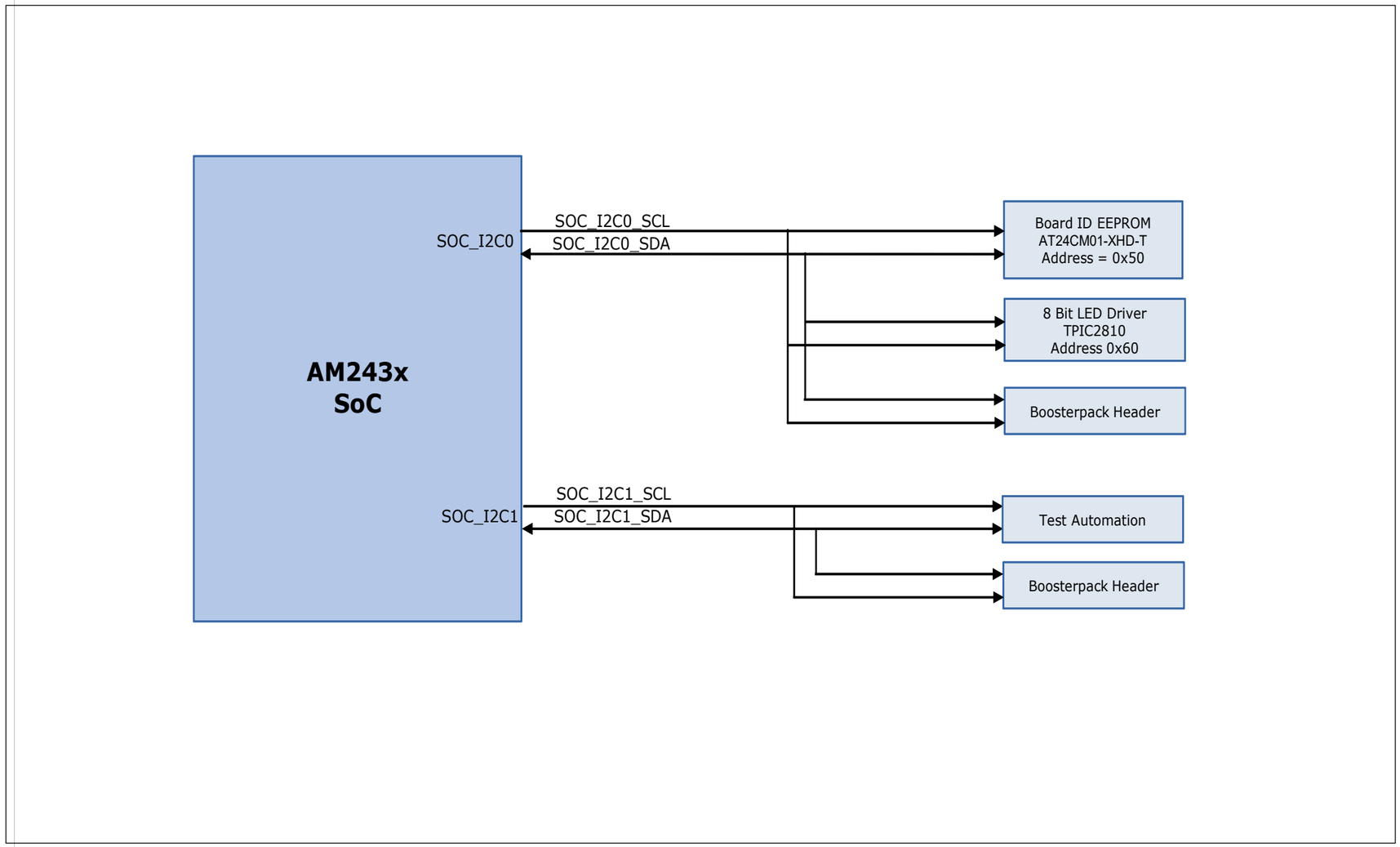
GPIO MAPPING TABLE

AM243x LP - GPIO Mapping Table						
Net name	AM243x LP Mapping					
	Package Signal Name	GPIO Number	Input/Output	Default	State	Remarks
TEST_LED1_GREEN	GPMC0_AD7	GPIO0_22	Output	PD	Active High	To Turn ON the test LED (Green)
TEST_LED2_RED	UART0_RTSN	GPIO1_55	Output	PD	Active High	To Turn ON the test LED (Red)
TEST_LED3_RED	PRG1_PRU1_GPO18	GPIO1_39	Output	PD	Active High	To Turn ON the test LED (Red) in Bicolor LED
TEST_LED4_GREEN	PRG1_PRU1_GPO19	GPIO1_38	Output	PD	Active High	To Turn ON the test LED (Green) in Bicolor LED
GPIO_RGMII1_PHY_RSTn	GPMC0_AD13	GPIO0_26	Output	PU	Active Low	To Reset the RGMII1 Ethernet PHY
PRG_CPSW_RGMII1_MUX_SEL	GPMC0_AD12	GPIO0_27	Output	PD	NA	To select the RGMII1 path between PRG and CPSW
USER_INTn	UART0_CTSN	GPIO1_54	Input	PU	Active Low	User Interrupt input from Push Button Switch
OSPI0_RESET_N	OSPI0_CSN1	GPIO0_12	Output	PU	Active Low	To reset the QSPI FLASH on OSPI0 Instance
MCAN/eQEP_MUX_SEL	PRG0_PRU1_GPO8	GPIO1_28	Output	PD	NA	To select the functionality of MCAN0_RX pin as MACN0_RX or eQEP_I
FSI/BP_MUX_SEL	GPMC0_AD11	GPIO0_28	Output	PD	NA	To select the functionality of GPMC0_AD8 and GPMC0_AD9 pins as FSI_RX or PWM
MCAN0_STB	PRG0_PRU1_GPO5	GPIO1_25	Output	PU	Active Low	To put the CAN Transceiver out of Standby
PRG1_CPSW_ETH2_LED_1000/RX_ER	PRG1_PRU1_GPO5	GPIO0_70	Input	PD	NA	Ethernet PHY2 RX ER indication to SoC
PRG1_CPSW_ETH2_LED_LINK	PRG1_PRU1_GPO8	GPIO0_73	Input	PD	NA	Ethernet PHY2 RX link indication to SoC
GPIO_RGMII2_PHY_RSTn	PRG1_PRU1_GPO18	GPIO0_20	Output	PU	Active Low	To Reset the RGMII2 Ethernet PHY
PRG1_CPSW_RGMII_INTn	PRG1_PRU1_GPO19	GPIO0_84	Input	PU	Active Low	Interrupt signal from Both RGMII1 & RGMII2 Ethernet PHYs
PRG1_CPSW_ETH1_LED_1000/RX_ER	PRG1_PRU0_GPO5	GPIO0_50	Input	PD	NA	Ethernet PHY1 RX ER indication to SoC
PRG1_CPSW_ETH1_LED_LINK	PRG1_PRU0_GPO8	GPIO0_53	Input	PD	NA	Ethernet PHY1 RX link indication to SoC
PRG1_CPSW_ETH1_LED_ACT	PRG1_PRU0_GPO9	GPIO0_54	Input	PD	NA	Ethernet PHY1 MII COL indication to SoC
PRG1_CPSW_ETH2_LED_ACT	PRG1_PRU1_GPO9	GPIO0_74	Input	PD	NA	Ethernet PHY2 MII COL indication to SoC

I2C TREE



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Title	I2C TREE	
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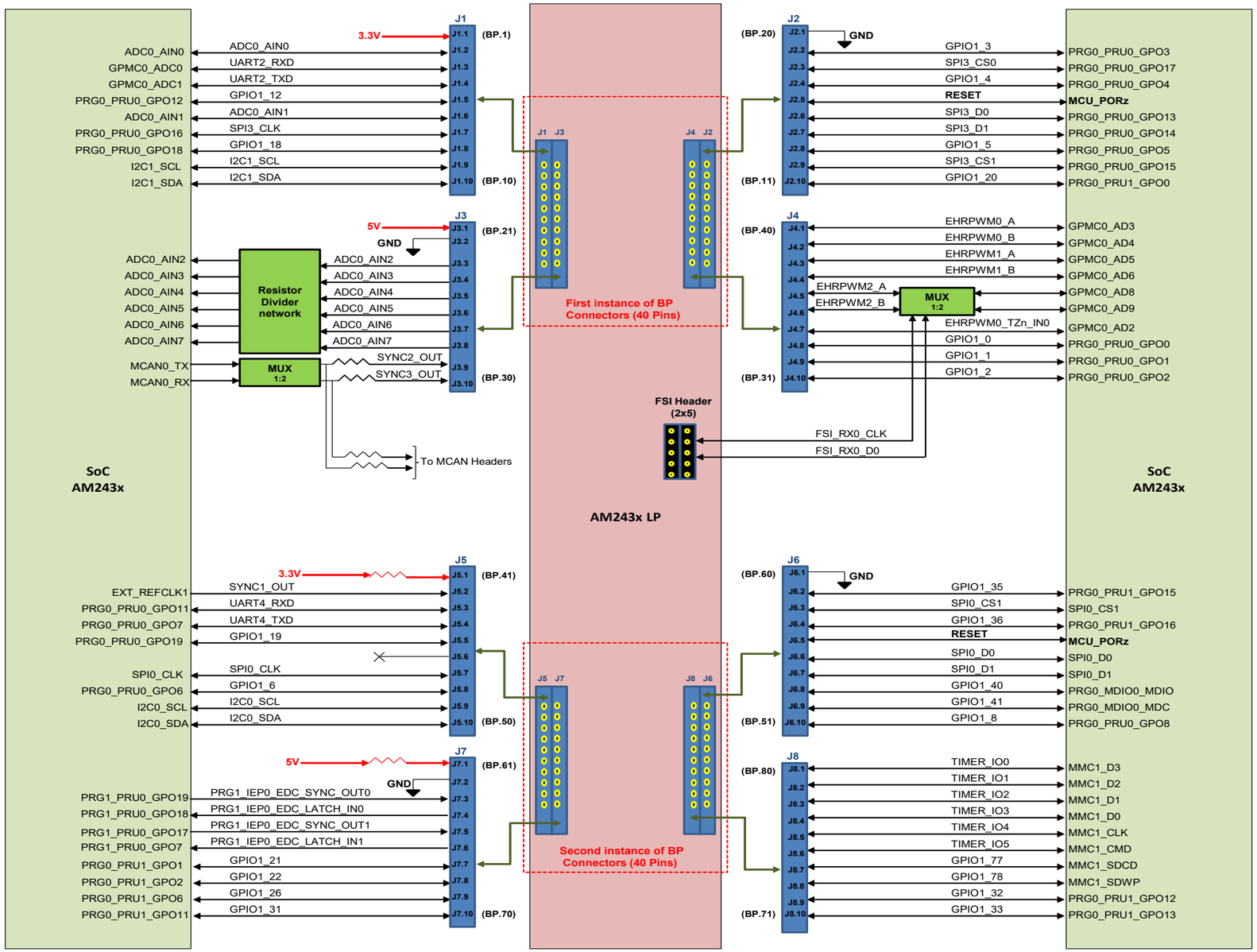
BOOSTERPACK CONNECTOR PINOUTs



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Title	BOOSTERPACK CONNECTOR PINOUTS	
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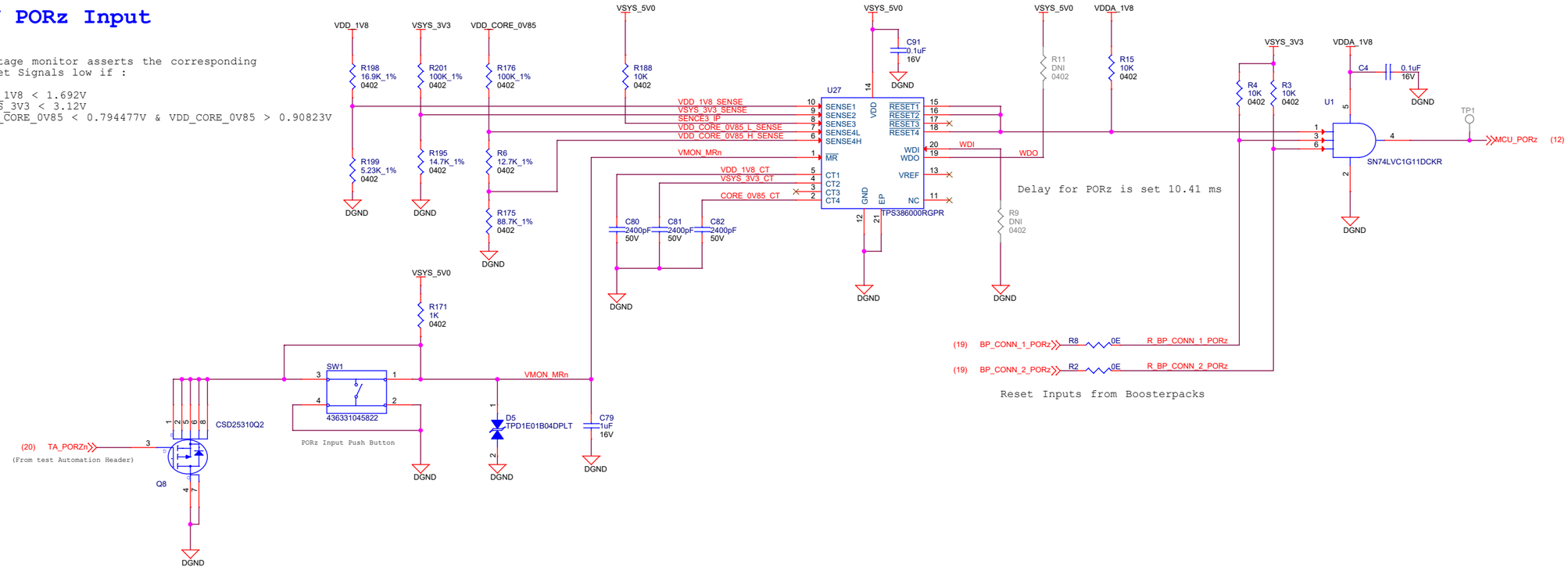
Reset Inputs

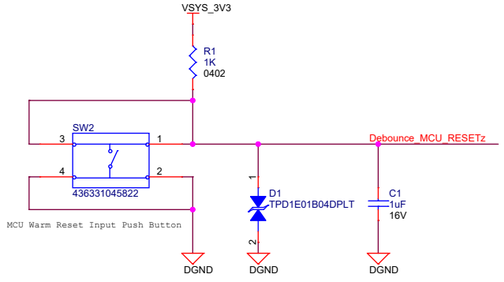
MCU PORz Input

Voltage monitor asserts the corresponding reset Signals low if :

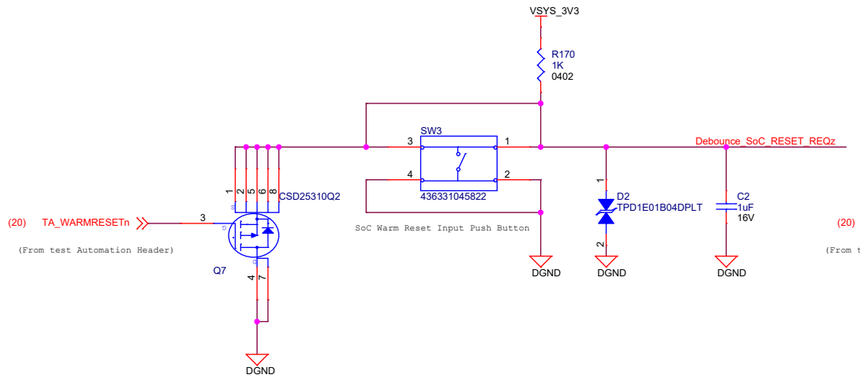
VDD_1V8 < 1.692V
VSYS_3V3 < 3.12V
VDD_CORE_0V85 < 0.794477V & VDD_CORE_0V85 > 0.90823V



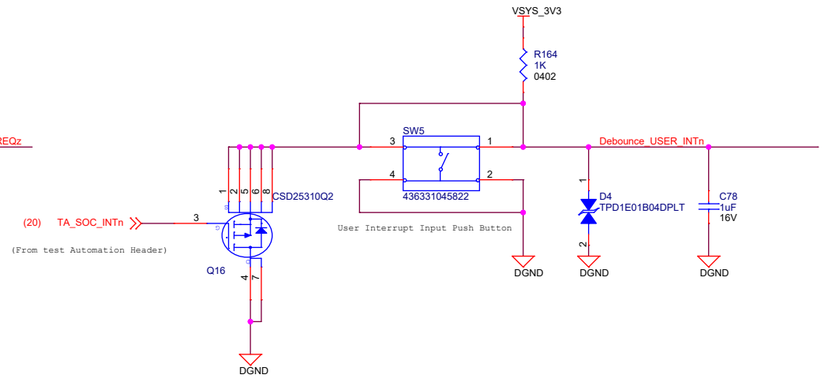
MCU Warm Reset Input



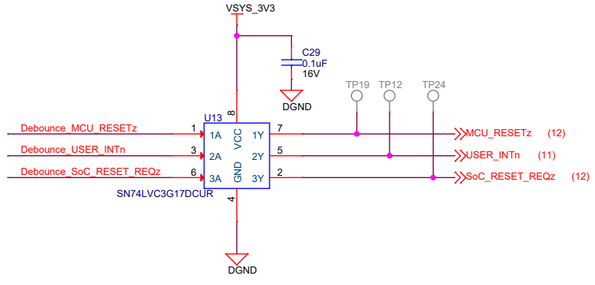
SoC Warm Reset Input



User Push Button



DEBOUNCE CIRCUIT



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Title	RESET INPUTs	
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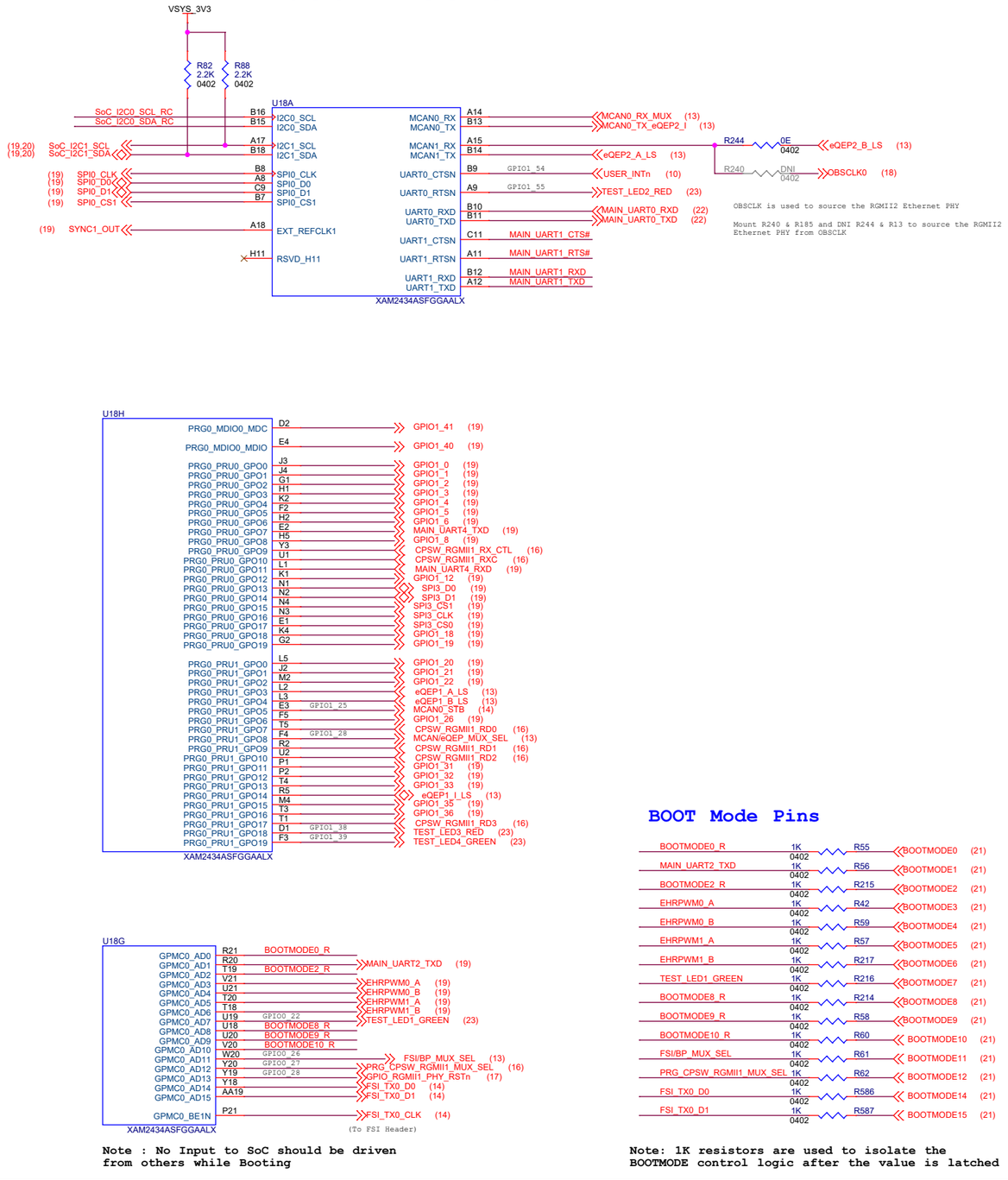
SoC Blocks

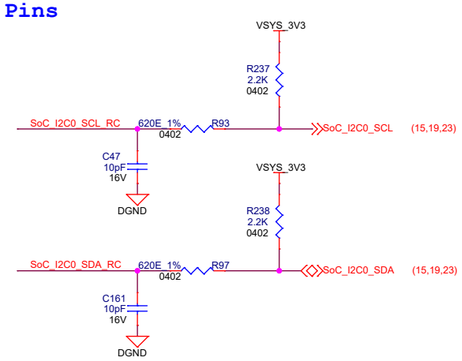


Note : No Input to SoC should be driven from others while Booting

BOOT Mode Pins

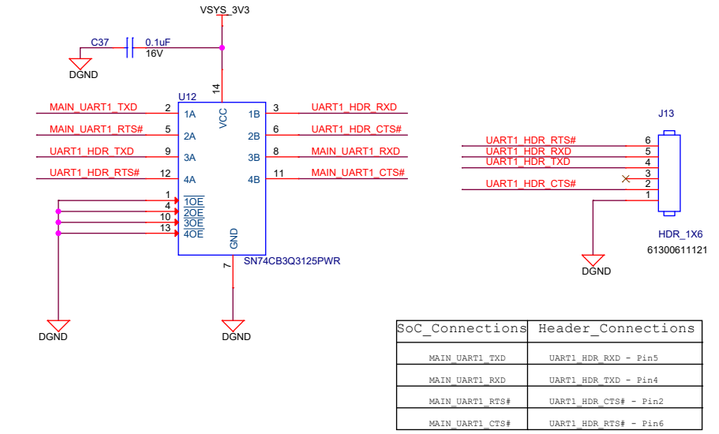
Note: 1K resistors are used to isolate the BOOTMODE control logic after the value is latched

LPF For I2C Pins



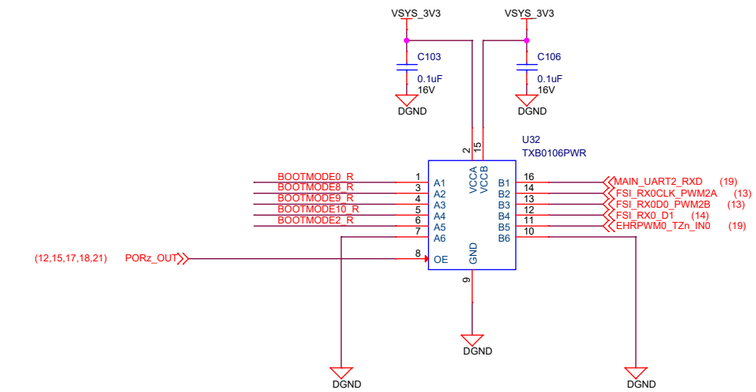
LPF Designed for 25MHz Cutoff
Have to change resistor and capacitor values accordingly

UART Buffer & EXT UART HDR for UART1



SoC_Connections	Header_Connections
MAIN_UART1_TXD	UART1_HDR_RXD - Pin5
MAIN_UART1_RXD	UART1_HDR_TXD - Pin4
MAIN_UART1_RTS#	UART1_HDR_CTS# - Pin2
MAIN_UART1_CTS#	UART1_HDR_RTS# - Pin6

Isolation Buffer for Bootmode Input pins



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Title	SOC1		
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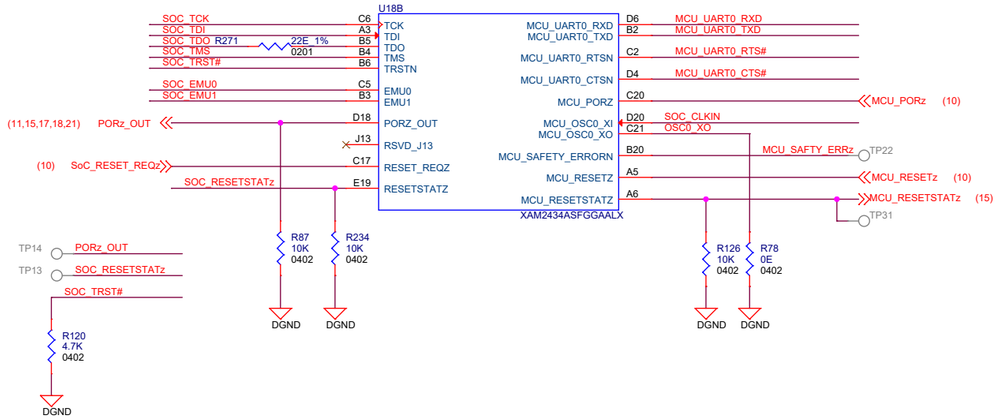
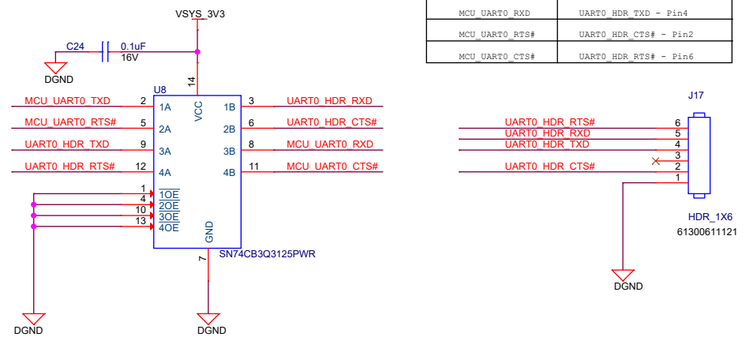
SoC Blocks

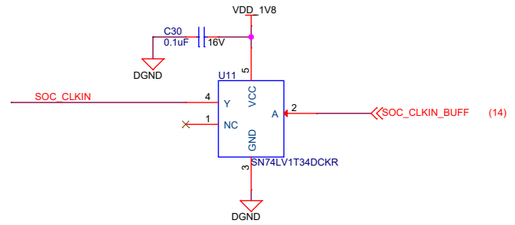


MCU UART0 Buffer & Header

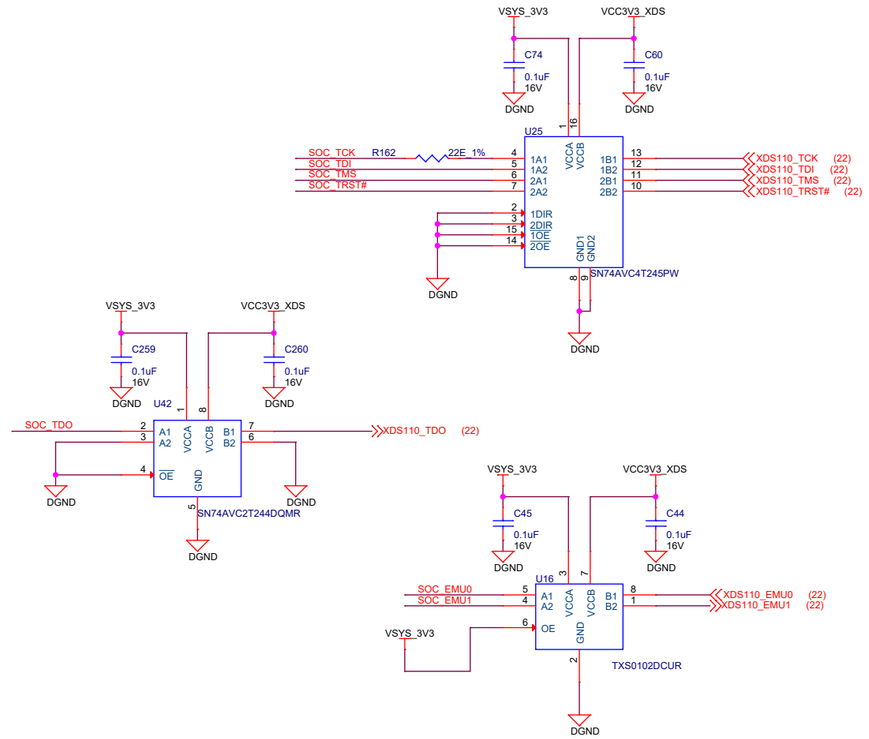
SoC_Connections	Header_Connections
MCU_UART0_TXD	UART0_HDR_RXD - Pin5
MCU_UART0_RXD	UART0_HDR_TXD - Pin4
MCU_UART0_RTS#	UART0_HDR_CTS# - Pin2
MCU_UART0_CTS#	UART0_HDR_RTS# - Pin6



SoC Clock Buffer



XDS110 JTAG Isolation Buffer



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Title	SOC2	
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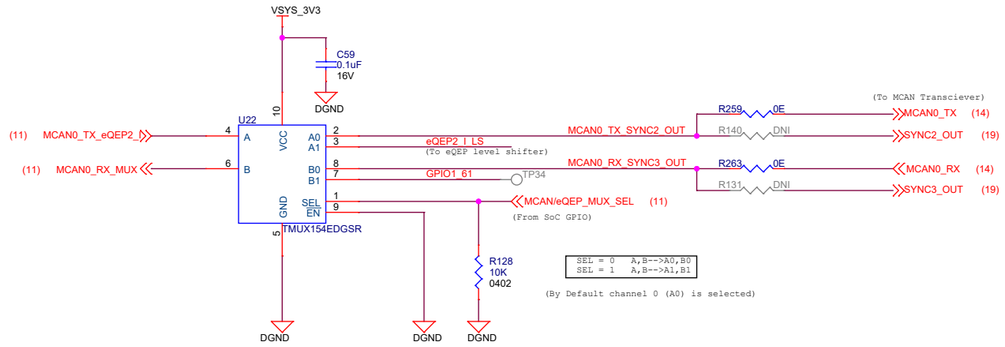
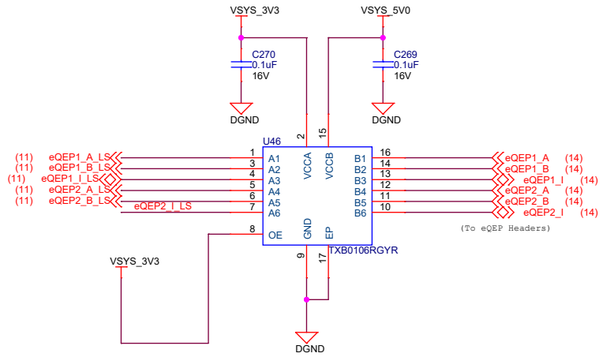
MCAN/eQEP FET Switch



eQEP Level Shifter



FSI/BP FET Switch

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Title	MCAN_eQEP_FSI_MUX	
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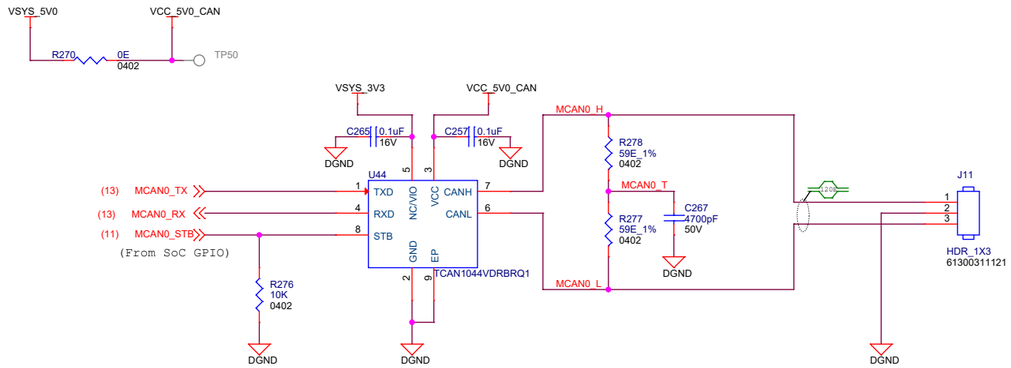
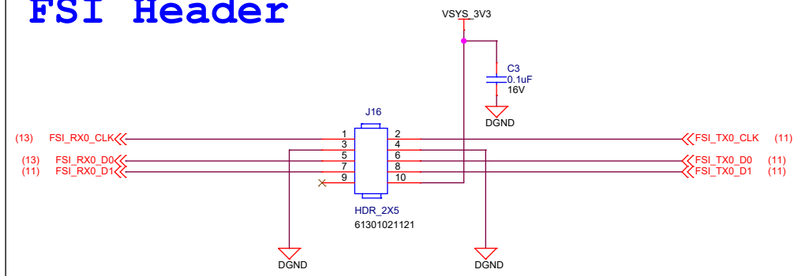
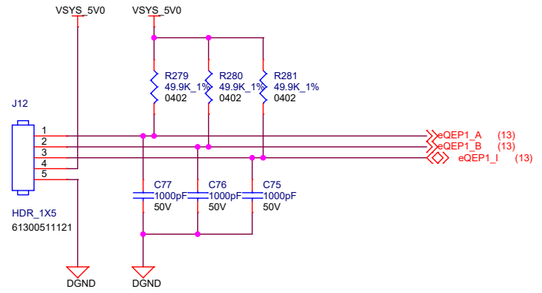
MCAN Transceiver & Header

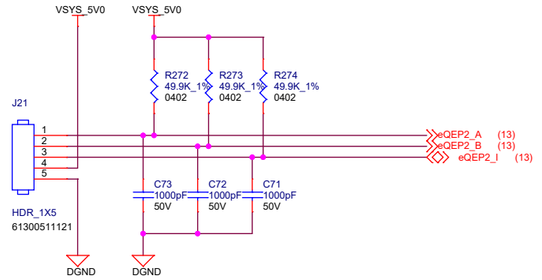


FSI Header

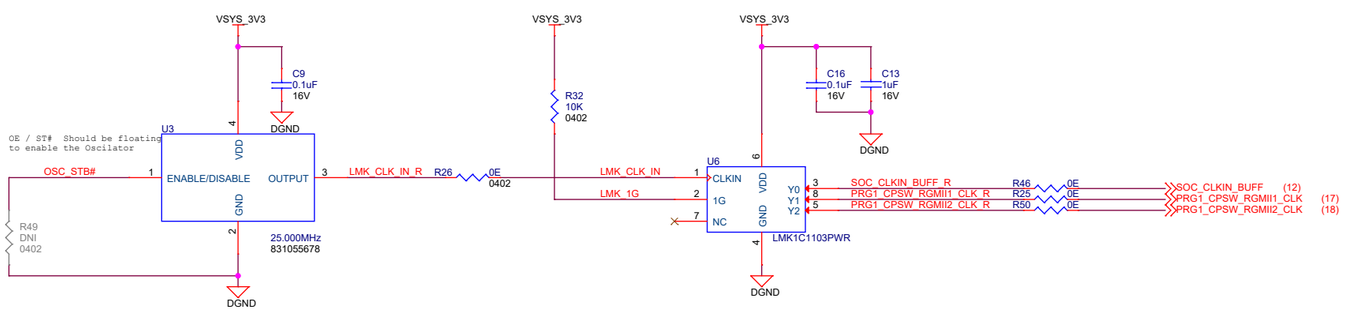


eQEP Headers





SoC and Ethernet PHY Clock Buffer



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Title	CAN_eQEP_FSI_HEADERs & CLOCK BUFFER	
Size C	PROC109 LP AM243	Rev E3
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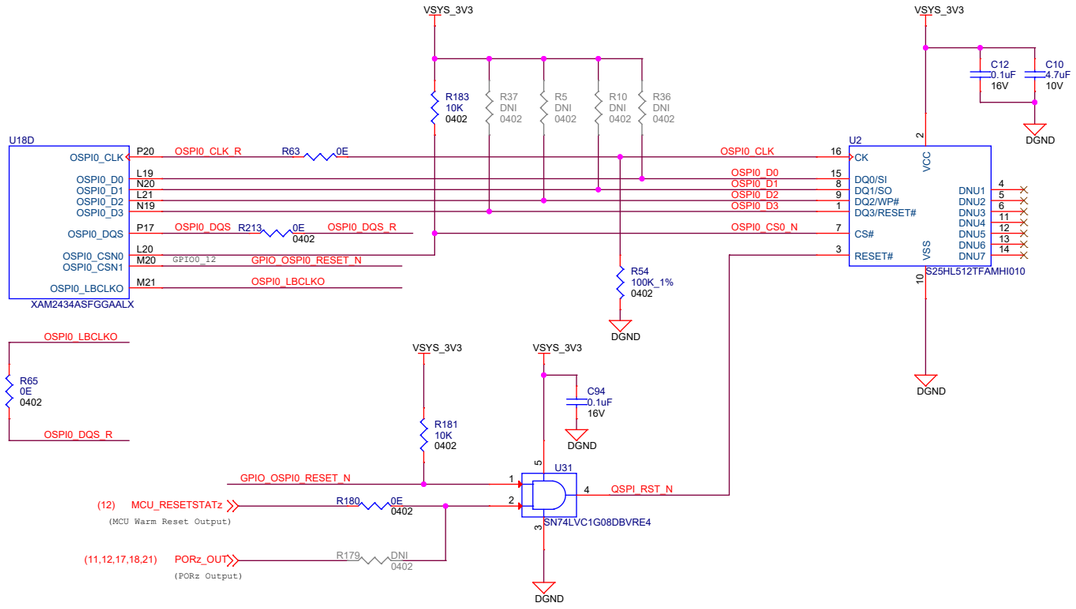
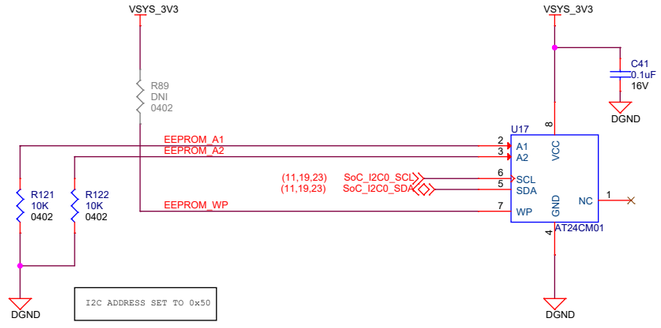
QSPI FLASH



Board ID EEPROM



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Title	QSPI_BOARD_ID_EEPROM	
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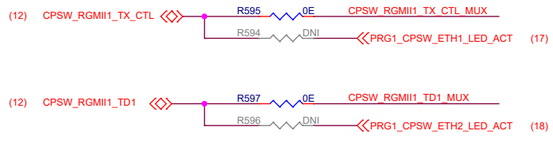
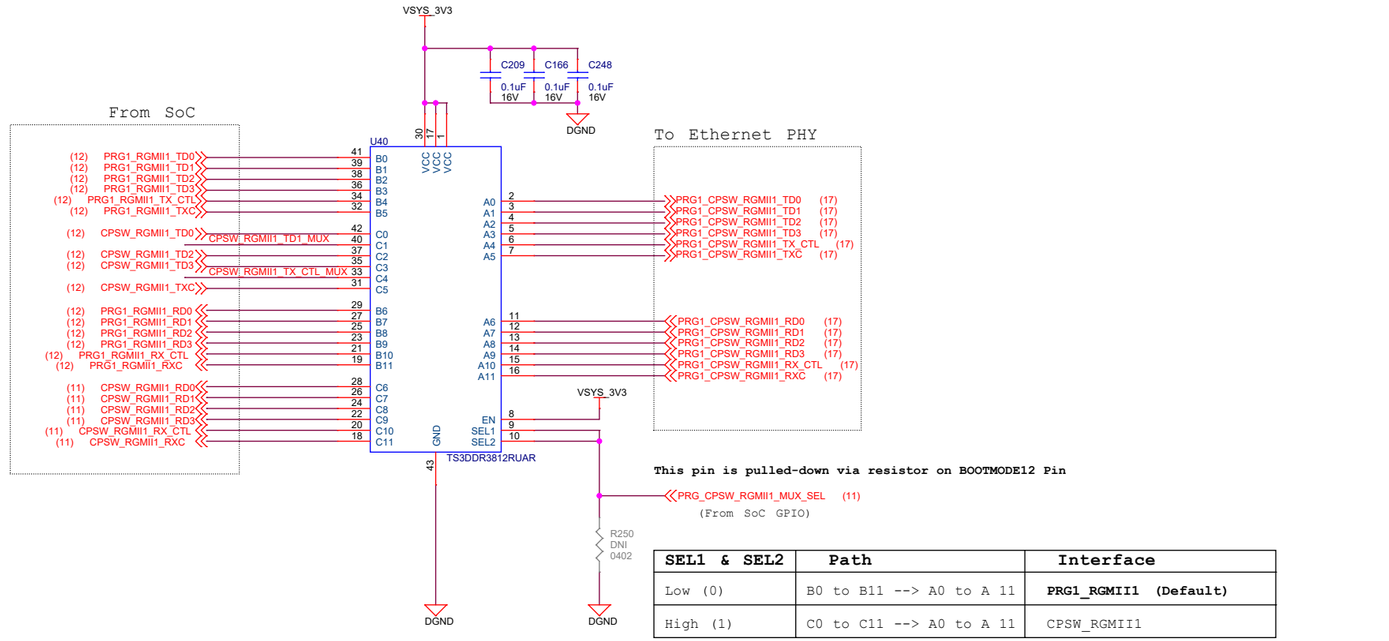
CPSW or PRG RGMII1 Ethernet Data MUX

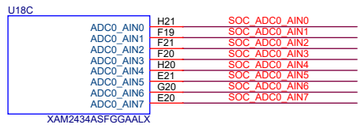


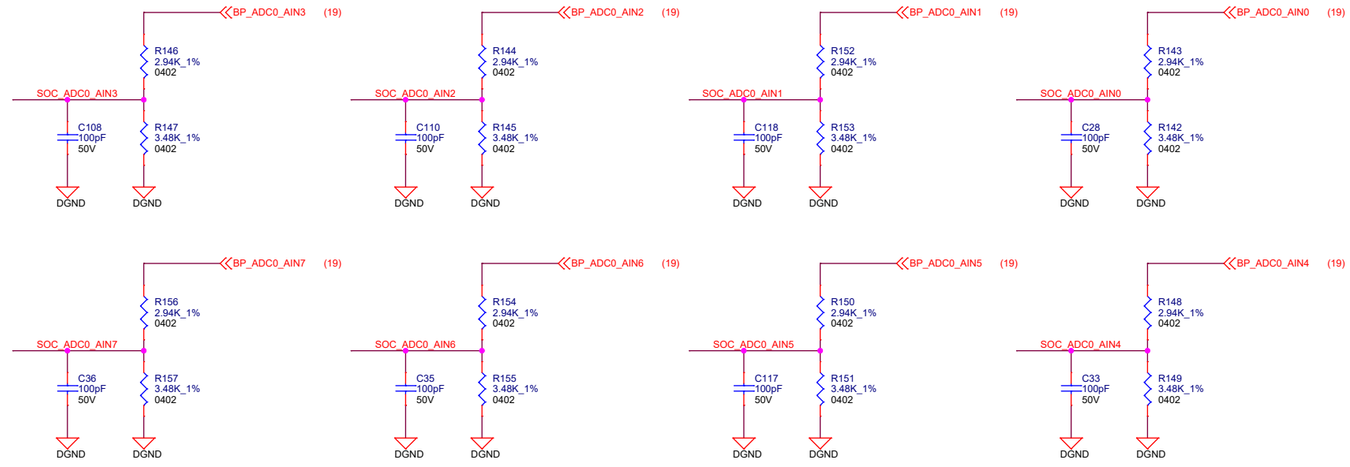


Interface	Mount	DNI
CPSW_RGMII1_TX_CTL & CPSW_RGMII1_TD1 (Default)	R595, R597	R594, R596
PRG1_CPSW_ETH1_LED_ACT & PRG1_CPSW_ETH2_LED_ACT	R594, R596	R595, R597

SEL1 & SEL2	Path	Interface
Low (0)	B0 to B11 --> A0 to A 11	**PRG1_RGMII1 (Default)**
High (1)	C0 to C11 --> A0 to A 11	CPSW_RGMII1

ADC Inputs





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Title	ETHERNET DATA MUX & ADC INPUTS	
Size C	PROC109 LP AM243	Rev E3
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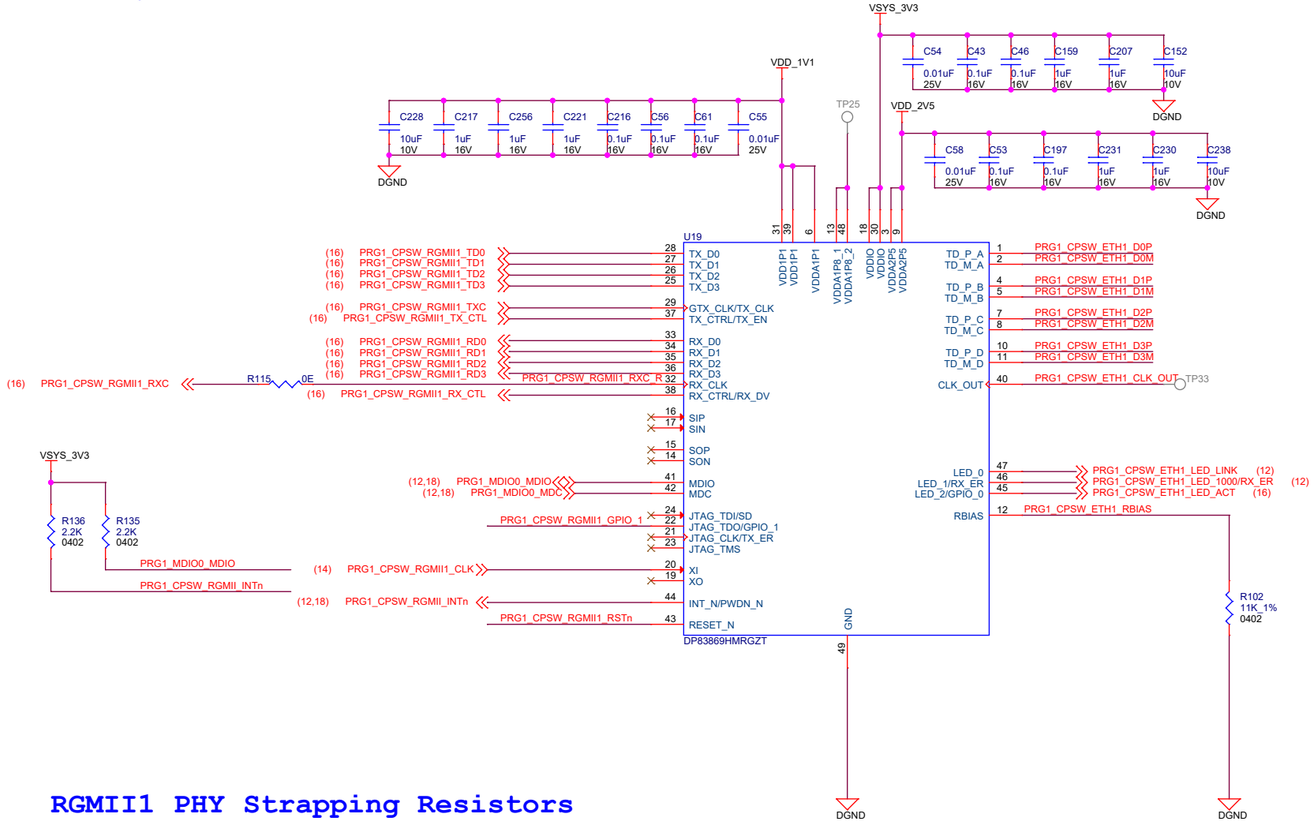
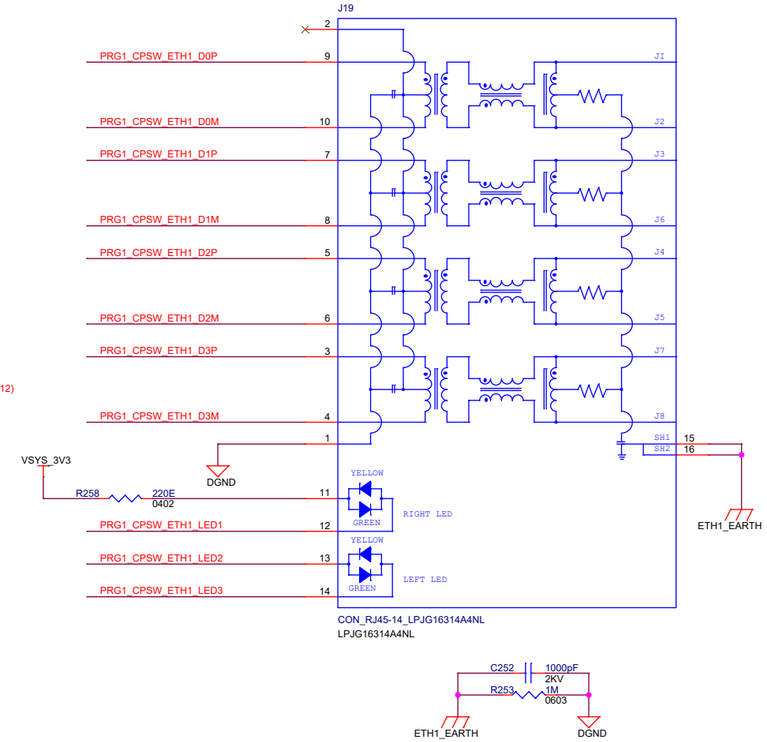
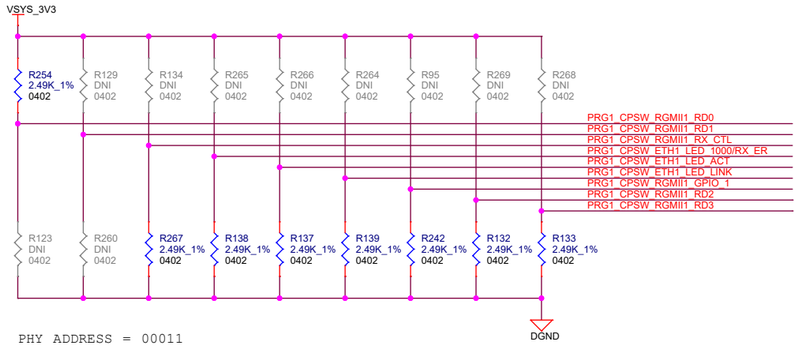
PRG / CPSW RGMII1 Ethernet PHY



RJ45 Connector with Integrated Magnetics



RGMII1 PHY Strapping Resistors

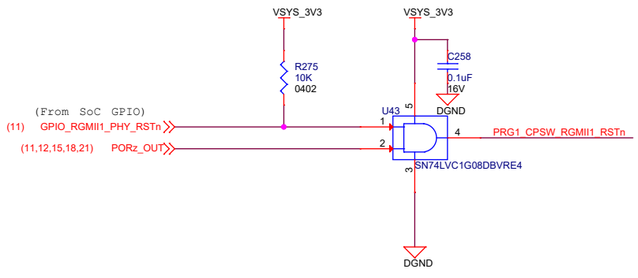


PHY ADDRESS = 00011

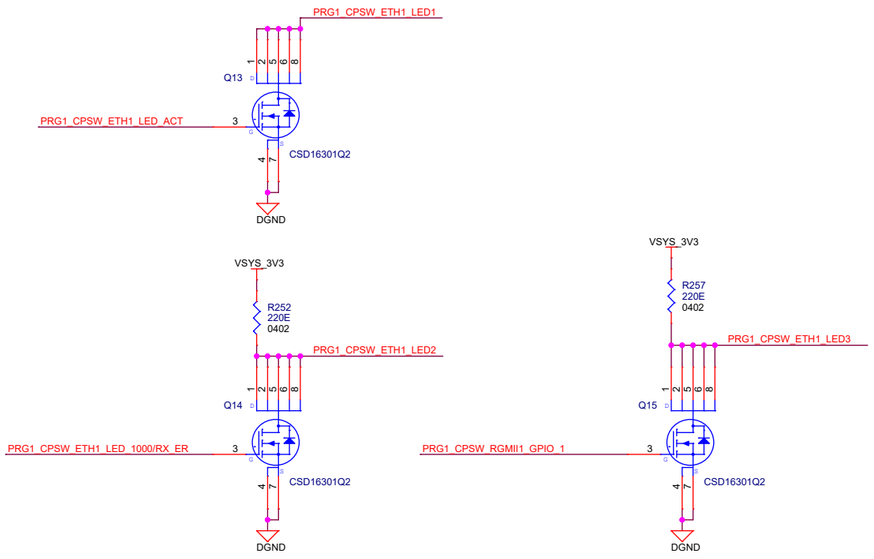
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X

RGMII to Copper (1000BaseT/100Base-TX/10Base-Te)

RGMII1 PHY Reset



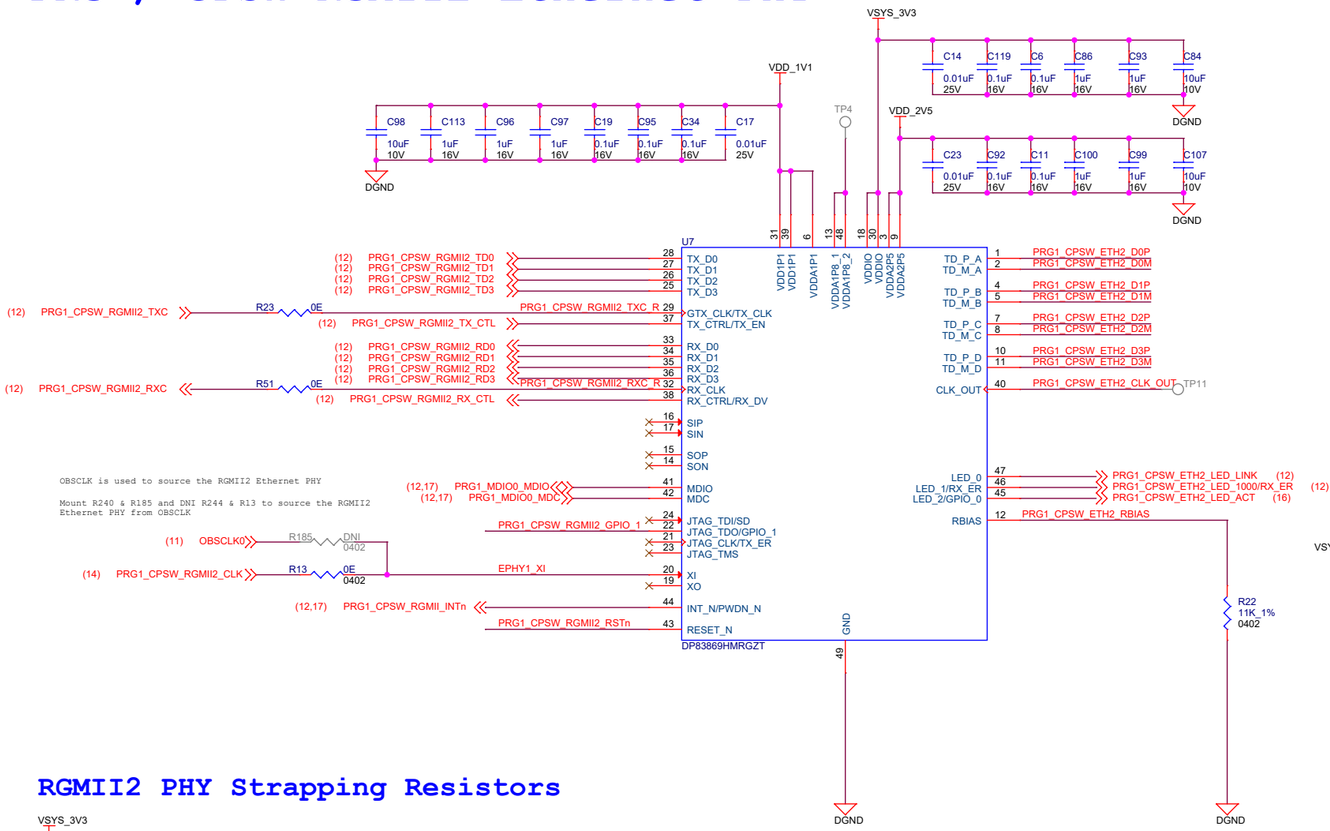
RGMII1 PHY Speed & Activity LED Drivers



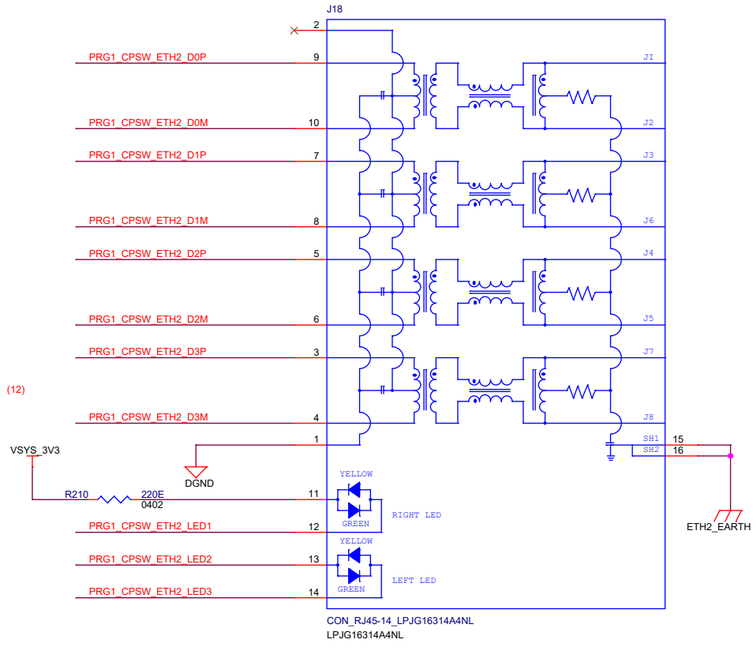
Designed for TI by Mistral Solutions Pvt Ltd

Title	PRG/CPSW RGMII1 ETHERNET PHY	
Size C	PROC109 LP AM243	Rev E3
Date: Monday, November 08, 2021	Sheet 17 of 29	

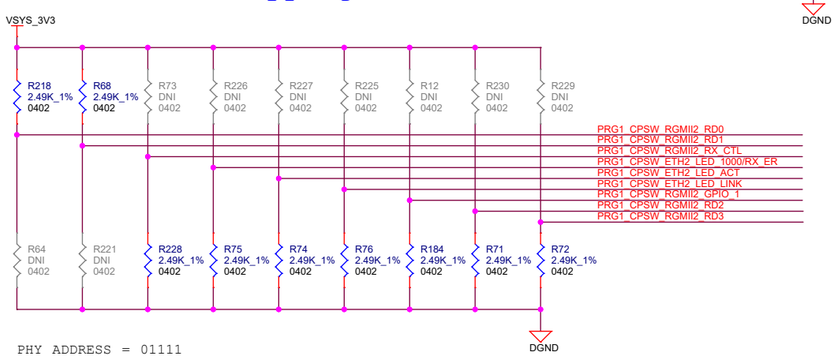
PRG / CPSW RGMII2 Ethernet PHY



RJ45 Connector with Integrated Magnetics



RGMII2 PHY Strapping Resistors

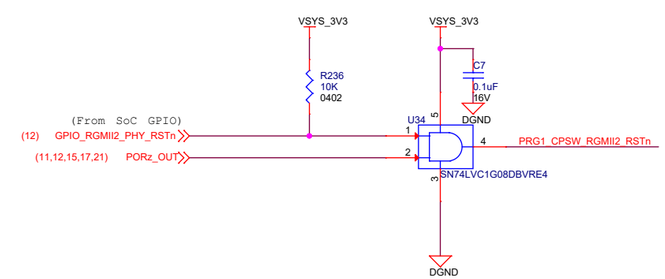


PHY ADDRESS = 01111

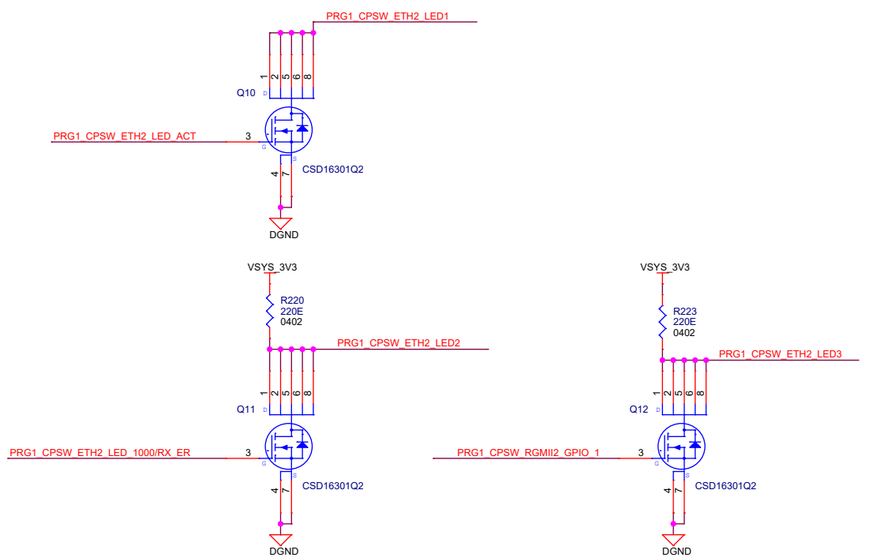
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X

RGMII to Copper (1000BaseT/100Base-TX/10Base-Te)

RGMII2 PHY Reset



RGMII2 PHY Speed & Activity LED Drivers



Designed for TI by Mistral Solutions Pvt Ltd

Title	PRG/CPSW RGMII2 ETHERNET PHY	
Size	PROC109 LP AM243	Rev
C		E3
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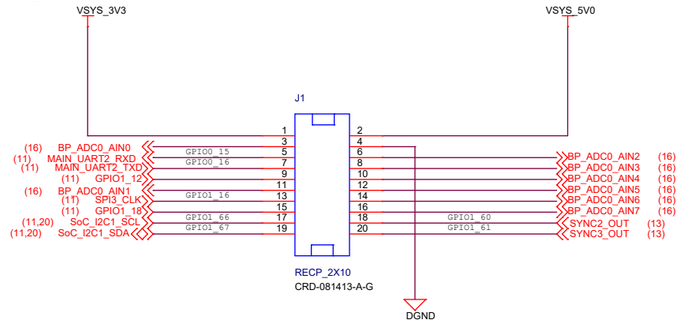
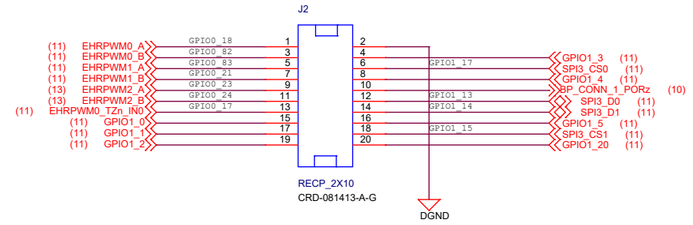
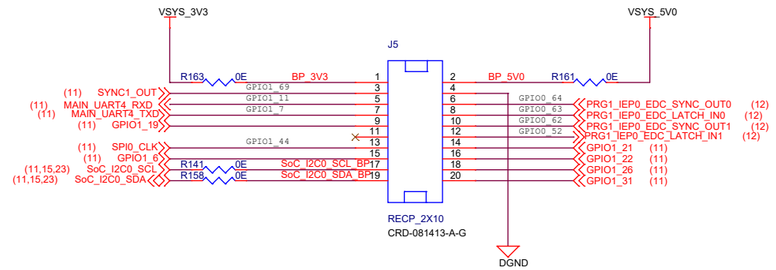
Booster Pack Header

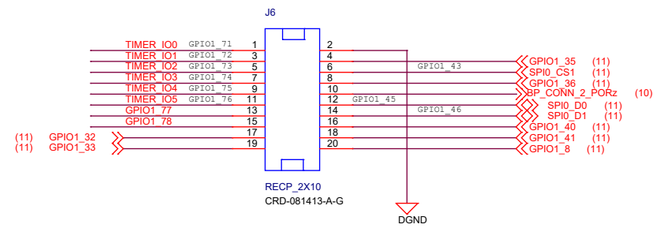
Boosterpack Header Site - 1

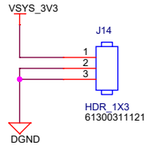


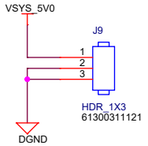


Boosterpack Header Site - 2

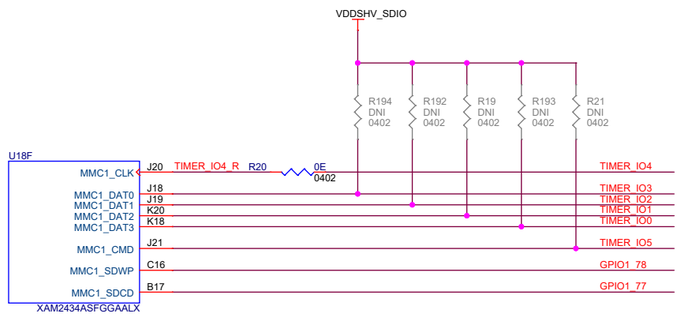








SoC MMC1 Connection to BP Header



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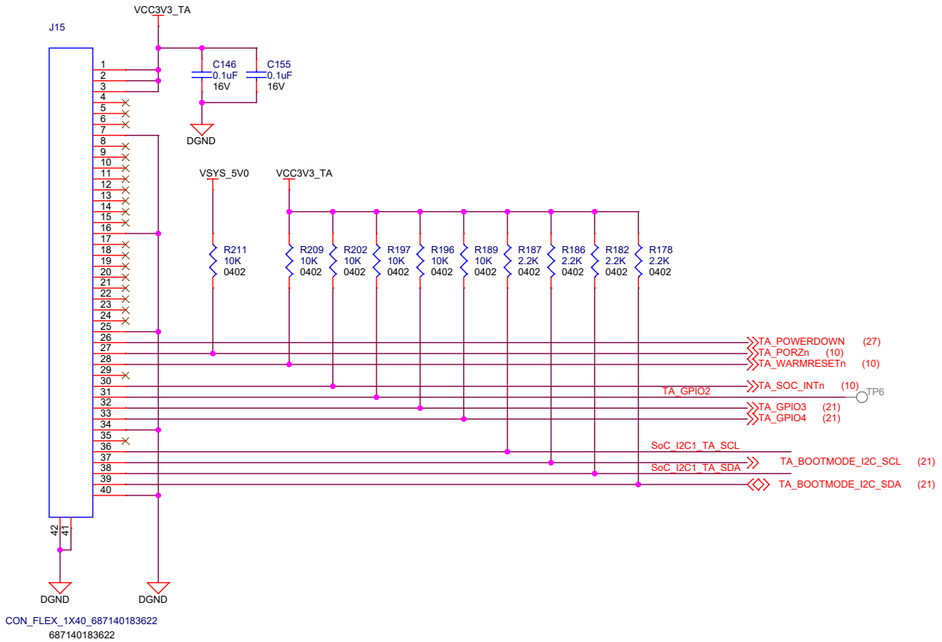
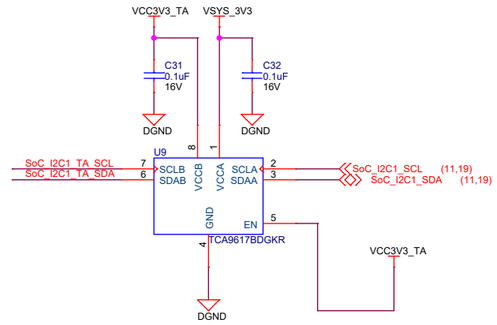
Title	BOOSTERPACK CONNECTOR	
Size	PROC109 LP AM243	Rev
C		E3
Date:	Monday, November 08, 2021	Sheet 19 of 29

40 - Pin Test Automation Header



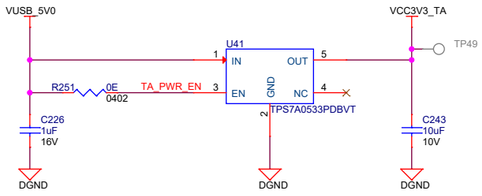
I2C Buffer for TA Header



Test Automation GPIO Mappping

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Powerdown the Board	OUTPUT	External Pullup
TA_PORZn	Used to Reset the SoC PORZ	OUTPUT	External Pullup
TA_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TA_GPIO3	Used to Disable the BOOTMODE Buffer	OUTPUT	External Pullup
TA_GPIO4	Used to Reset the BOOTMODE IO Expander	OUTPUT	External Pullup
TA_SOC_INTn	Interrupt to SoC	OUTPUT	External Pullup

Test Automation Board Power



3.3V @ 200mA

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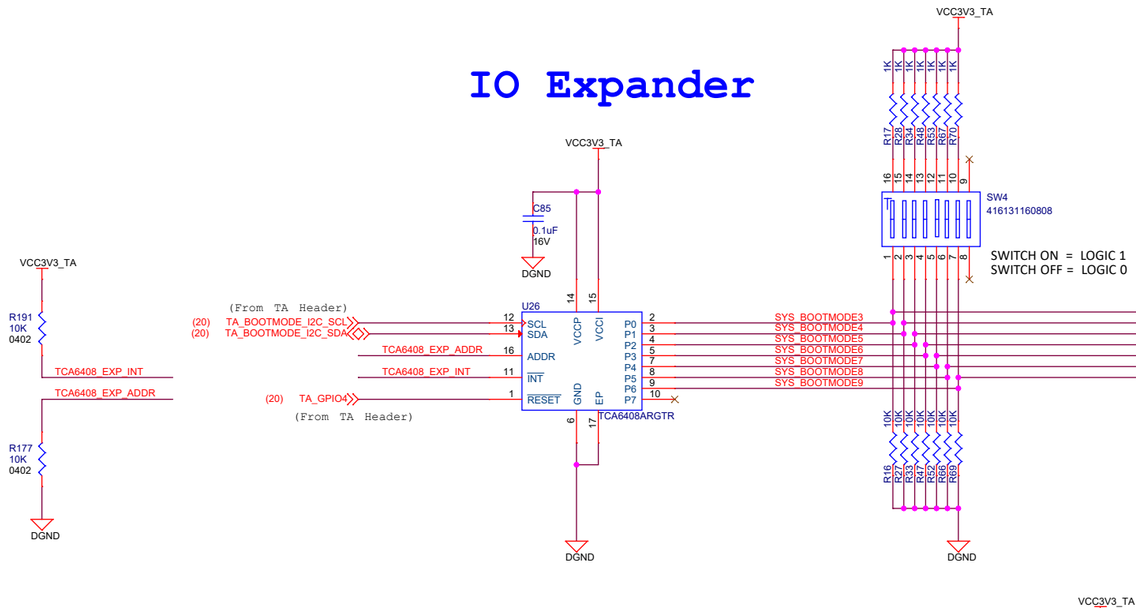
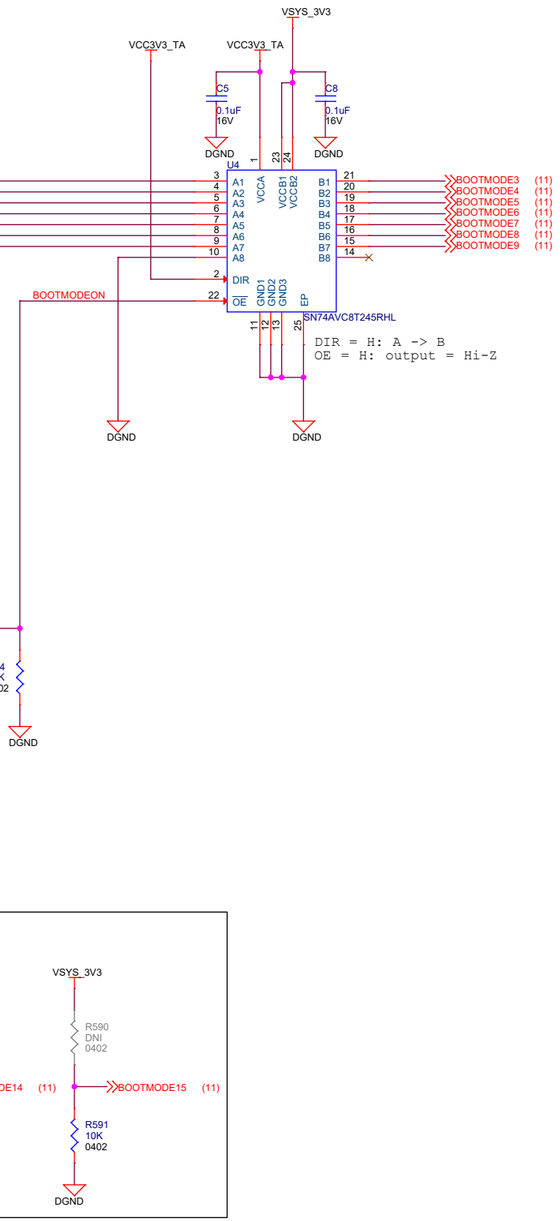
Title	TEST AUTOMATION HEADER	
Size C	PROC109 LP AM243	Rev E3
Date: Monday, November 08, 2021	Sheet 20 of 29	

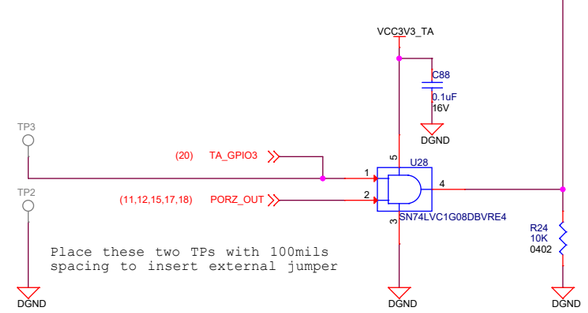
BOOT Mode Switch

IO Expander



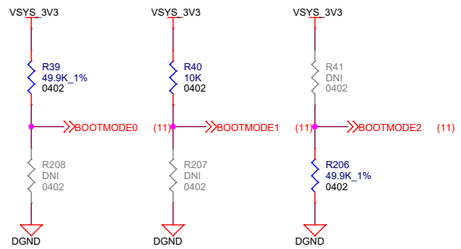
BOOT Mode Buffer



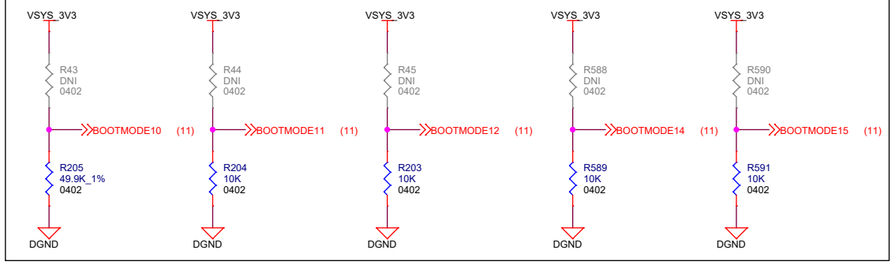


AM243x LP - Boot-Mode selection table							
Boot Modes Supported	**SW4.1**	**SW4.2**	**SW4.3**	**SW4.4**	**SW4.5**	**SW4.6**	**SW4.7**
QSPI FLASH	0	1	0	0	0	1	0
MMC1/SD Card	0	0	0	1	0	0	1
UART	1	1	1	0	0	0	0
USB - DFU	0	1	0	1	0	0	0
No Boot	1	1	1	1	0	0	0

BOOT_MODE0, 1 & 2 are used to select system Clock frequency
(Default 25 MHz is selected)



BOOT_MODE10, 11 & 12 are used to select Back-up Boot Mode
(By Default No Back-up Boot mode is selected)



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Title	BOOT MODE BUFFER & SWITCHES	
Size: C	PROC109 LP AM243	Rev: E3
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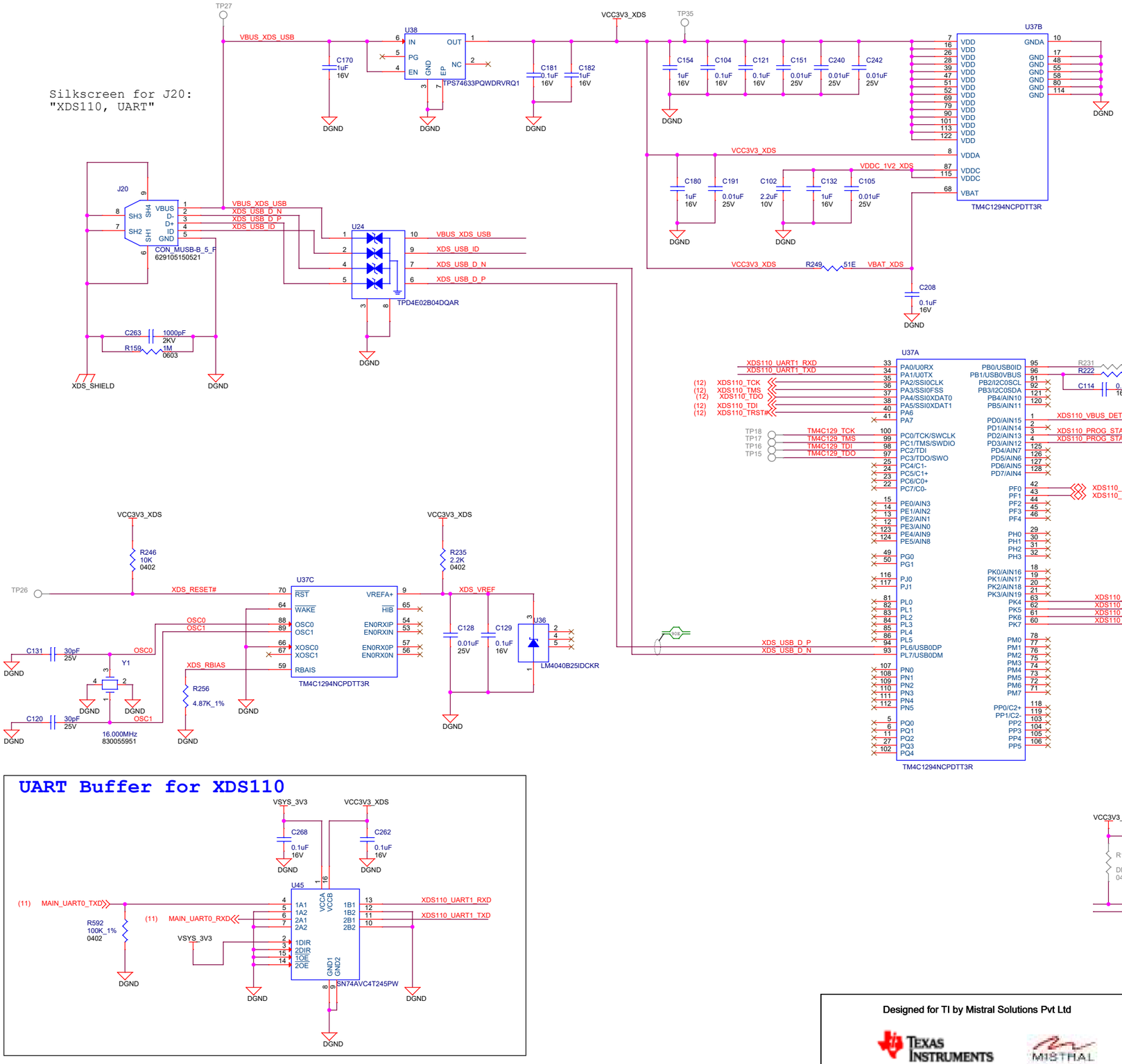
XDS110 Debugger

Silkscreen for J20:
"XDS110, UART"



UART Buffer for XDS110

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Title	XDS110 DEBUGGER	
Size C	PROC109 LP AM243	Rev E3
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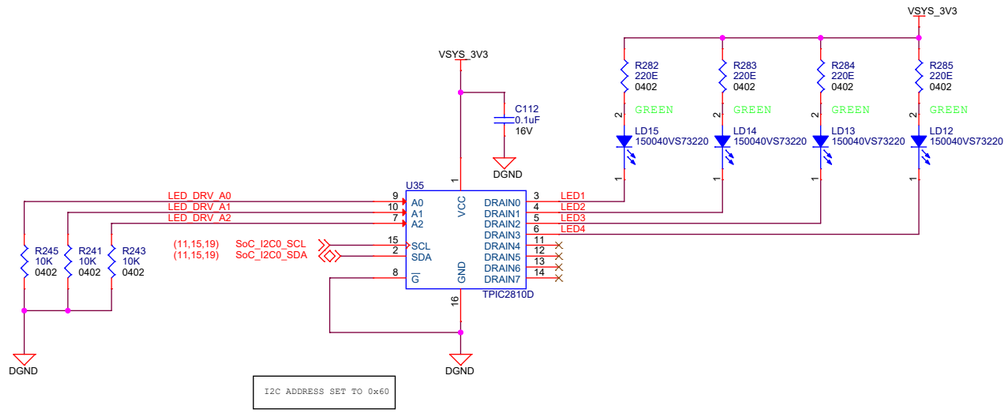
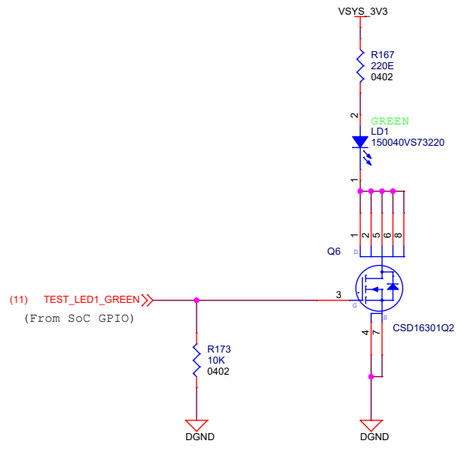
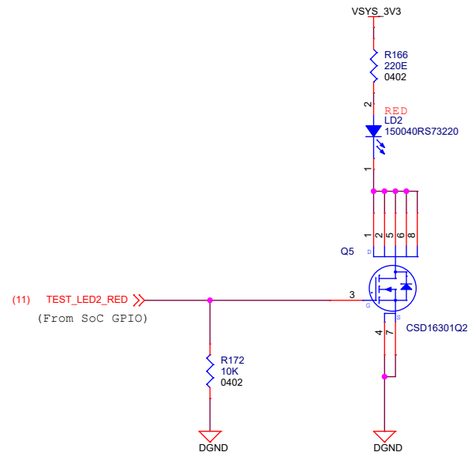
Industrial Communication LEDs



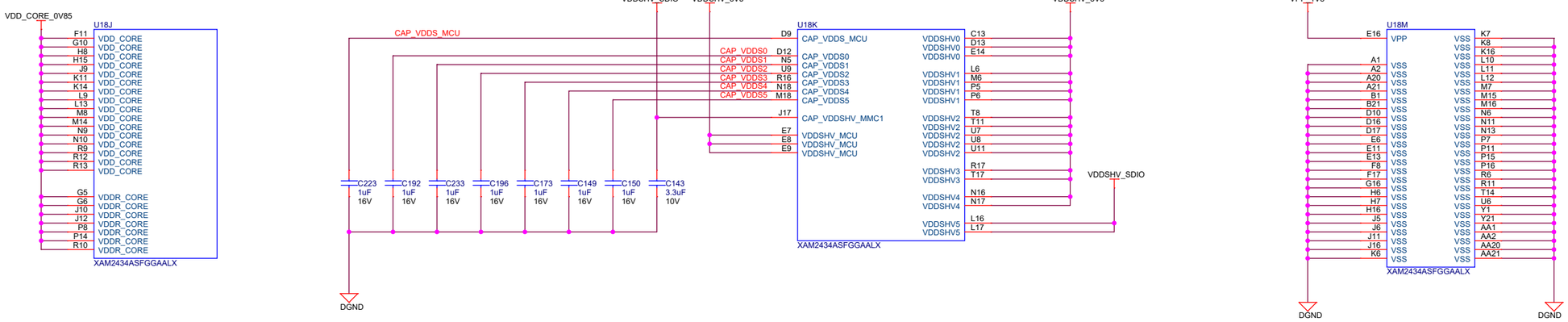


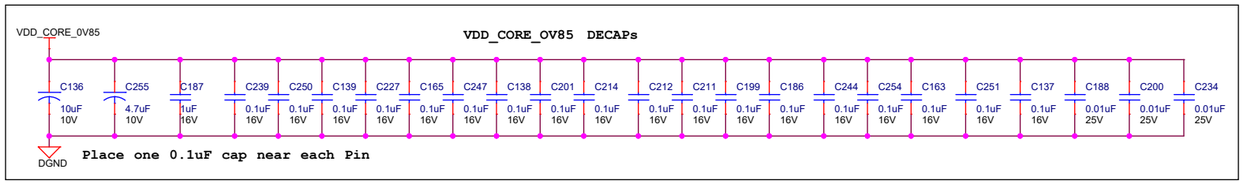


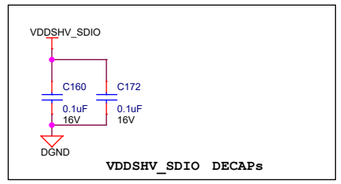
Designed for TI by Mistral Solutions Pvt Ltd

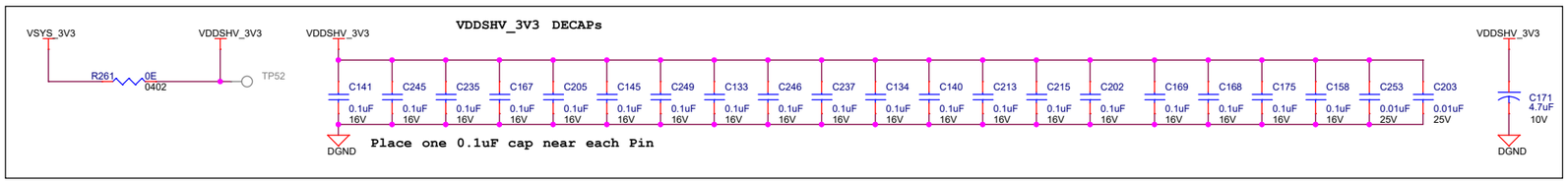
Title	INDUSTRIAL COMMUNICATION LEDs	
Size C	PROC109 LP AM243	Rev E3
Date: Monday, November 08, 2021	Sheet 23 of 29	

SoC Digital POWER & DECAPs









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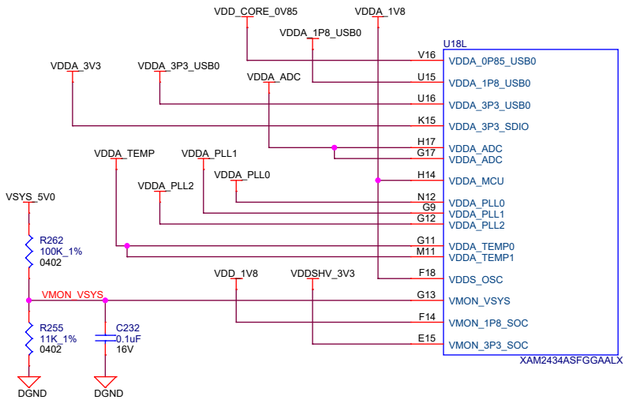
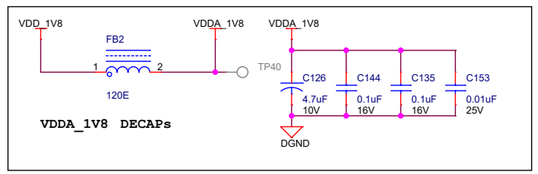
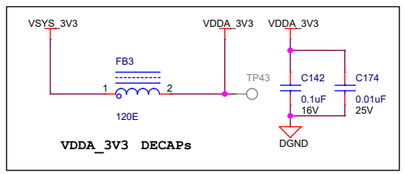
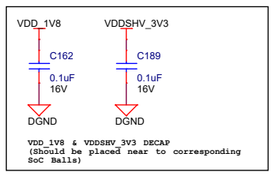
Title	SoC Digital POWER & DECAPs	
Size C	PROC109 LP AM243	Rev E3
Date: Monday, November 08, 2021	Sheet 24 of 29	

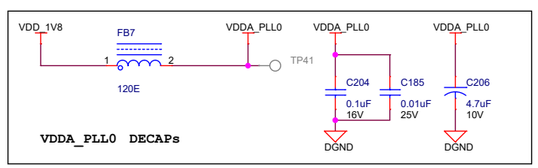
SoC Analog POWER & DECAPs

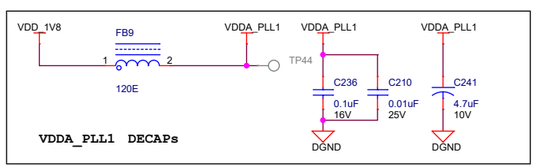


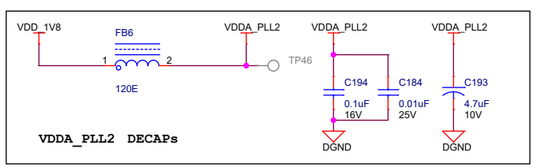


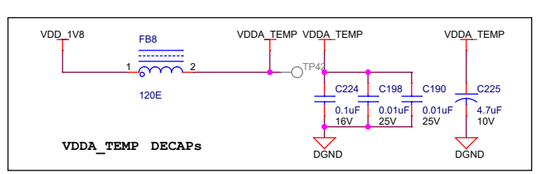


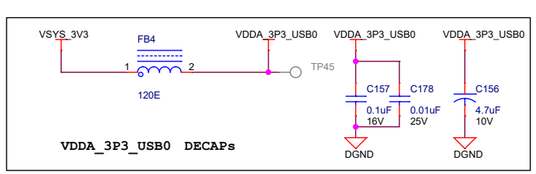


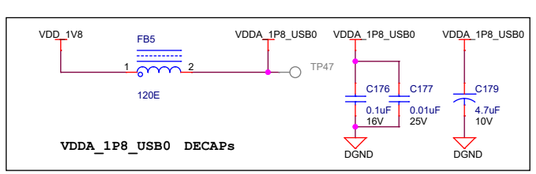


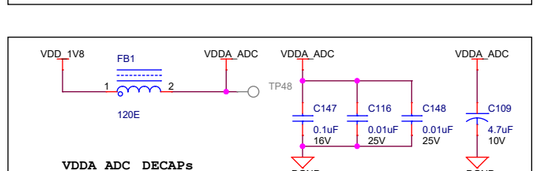












Designed for TI by Mistral Solutions Pvt Ltd

Title	SoC Analog POWER & DECAPs	
Size: C	PROC109 LP AM243	Rev: E3
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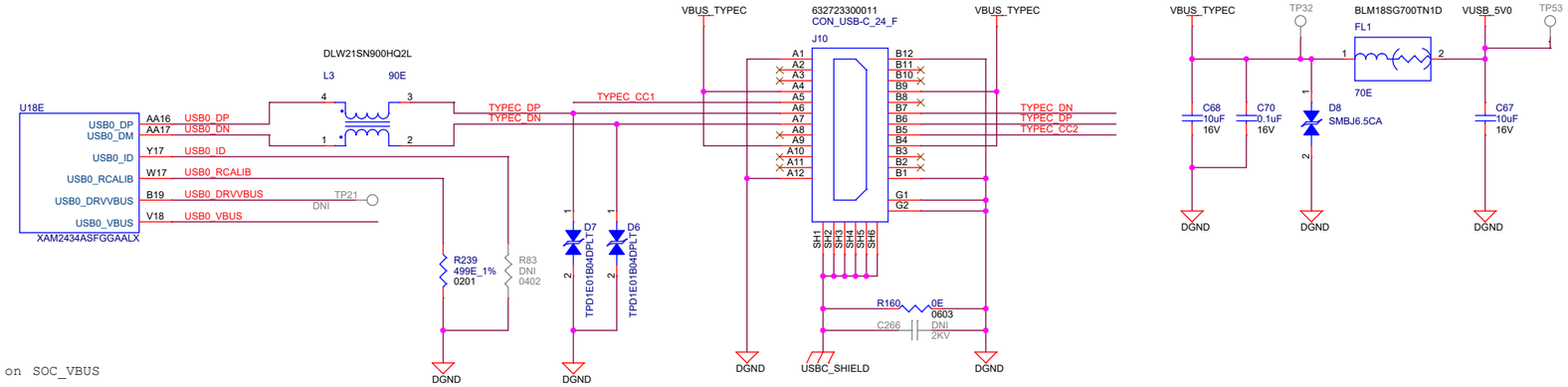
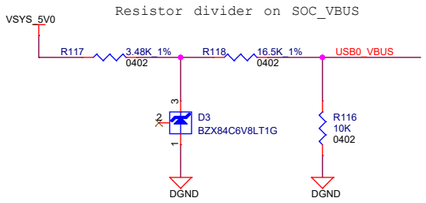
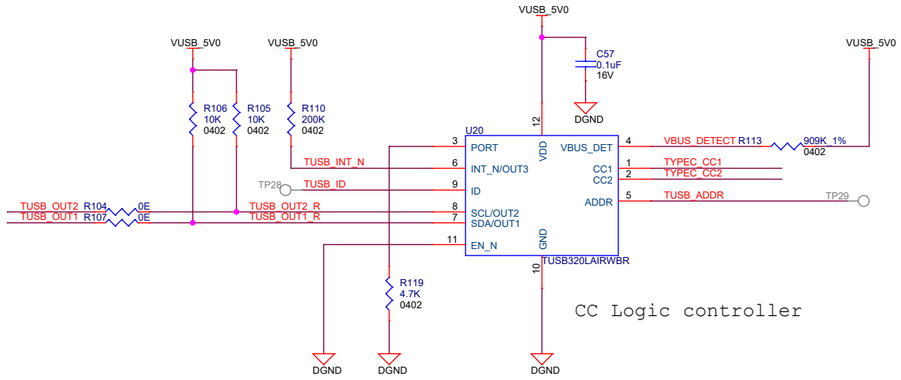
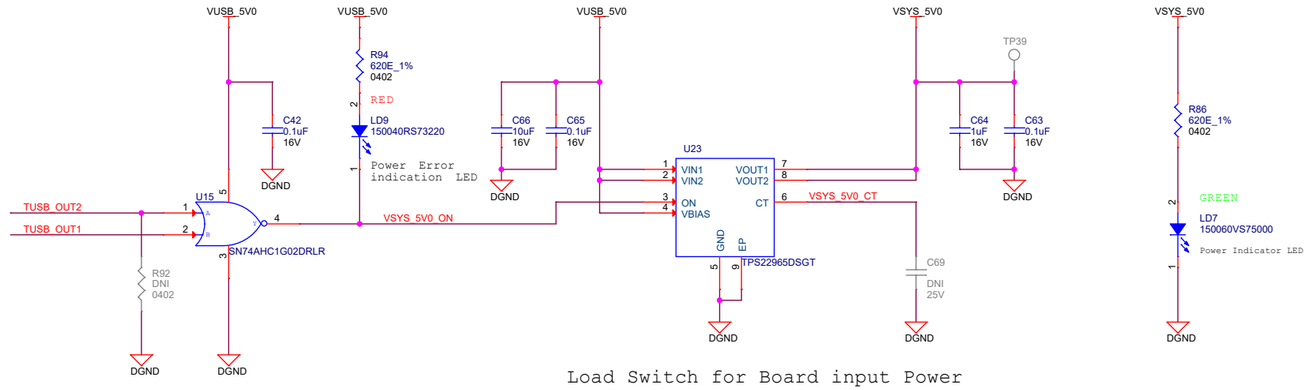
Type C Connector for Power Input & USB2.0









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Title	BOARD POWER INPUT & USB2.0	
Size C	PROC109 LP AM243	Rev E3
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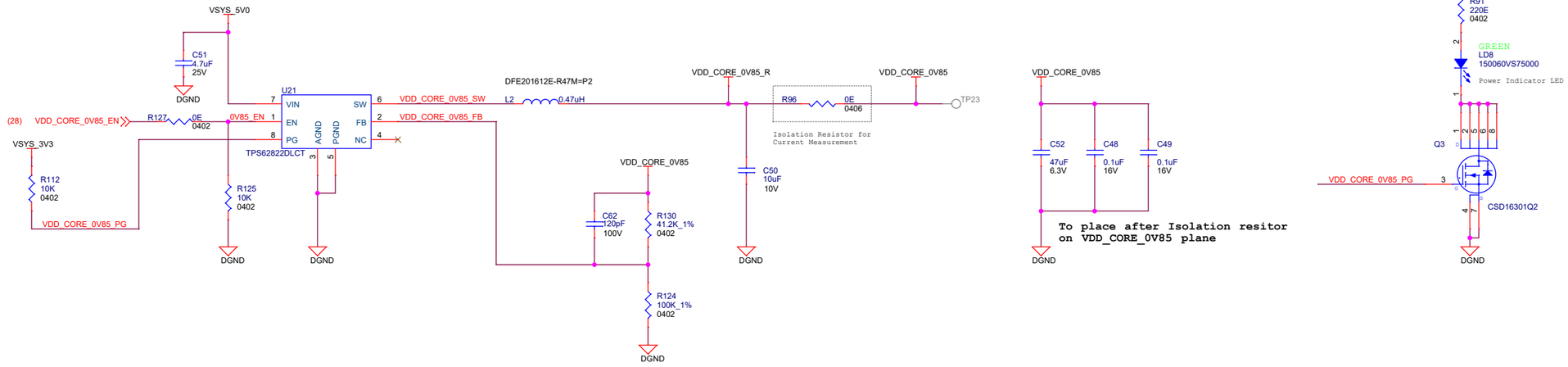
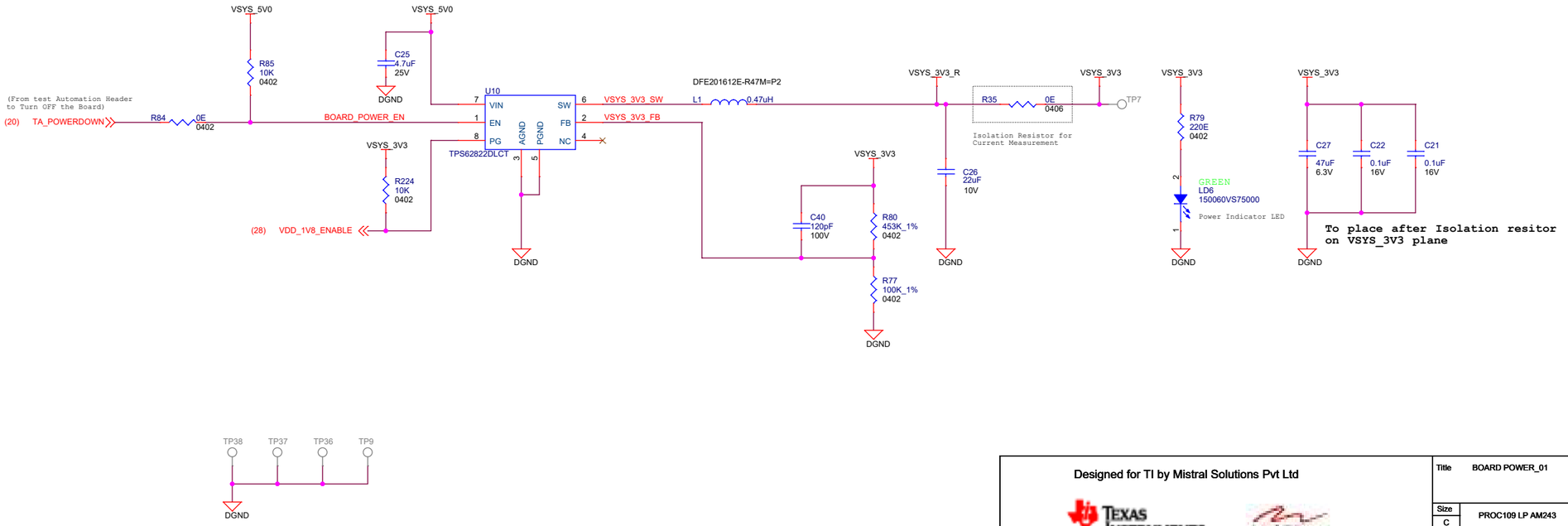
Core Voltage Generator

(0.85V, 2A)



Peripheral Voltage Generator

(3.3V, 2A)



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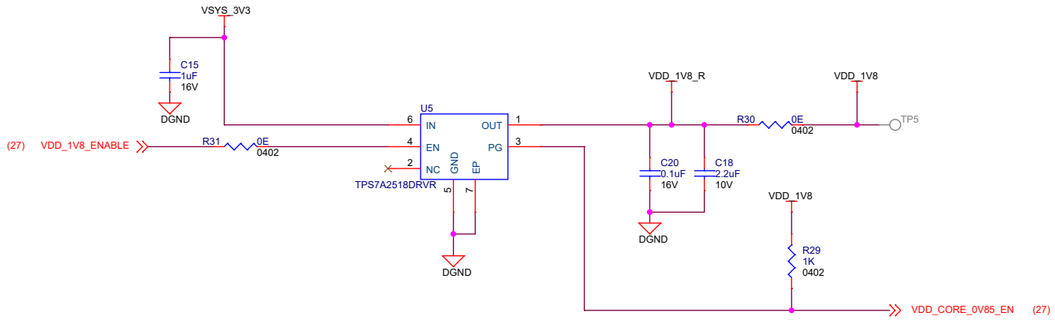
Title	BOARD POWER_01	
Size	PROC109 LP AM243	Rev
C		E3
Date:	Monday, November 08, 2021	Sheet 27 of 29

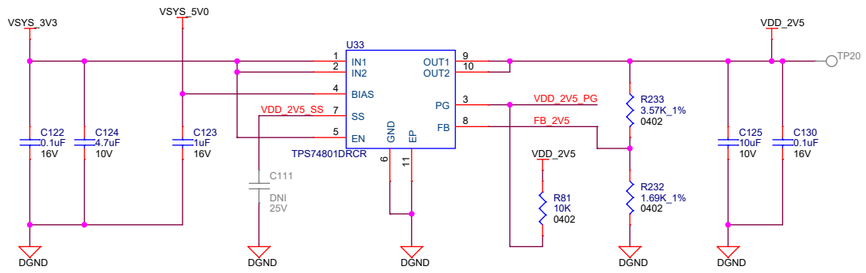
Analog Voltage LDO

(1.8V, 300mA)

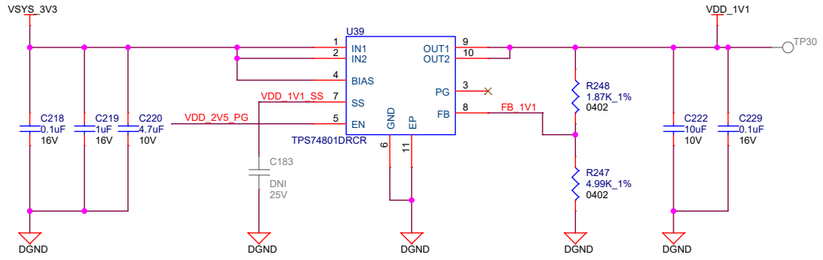


EPHY LDOs

3.3V to 2.5V

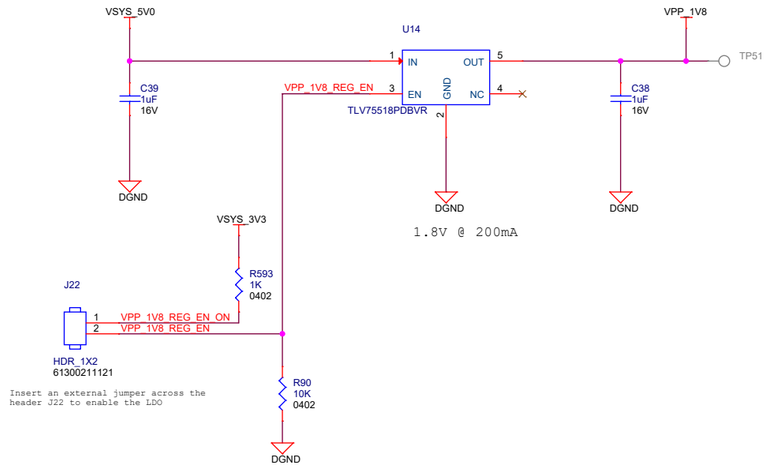


3.3V to 1.1V



eFUSE Programming Voltage LDO

(1.8V, 200mA)



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Title	BOARD POWER_02		
Size	PROC109 LP AM243		Rev
C			E3
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HARDWARE SCHEMATICS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards.
IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions
shall be observed.

5. These assemblies must be clean and free from flux and
all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and
packed securely before shipment.

Fiducials

FID1 DNI
FID2 DNI
FID3 DNI
FID4 DNI
FID5 DNI
FID6 DNI

BARE PCB

PCB1
PROC109E3

LABELS

Board Serial No.

LBL1
PCB LABEL
THT-103-423-10

Assembly Revision

LBL2
PCB LABEL
THT-103-423-10

LOGOs

PCB LOGO DNI
Texas Intruments

PCB LOGO DNI
TI Launch Pad Logo with web link

PCB LOGO DNI
Mistral Solutions

PCB LOGO DNI
WEEE Mark

PCB LOGO DNI
CE Mark

PCB LOGO DNI
For Evaluation only; not FCC approved for resale

Designed for TI by Mistral Solutions Pvt Ltd

Title	HARDWARE SCHEMATICS	
Size C	PROC109 LP AM243	Rev E3
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