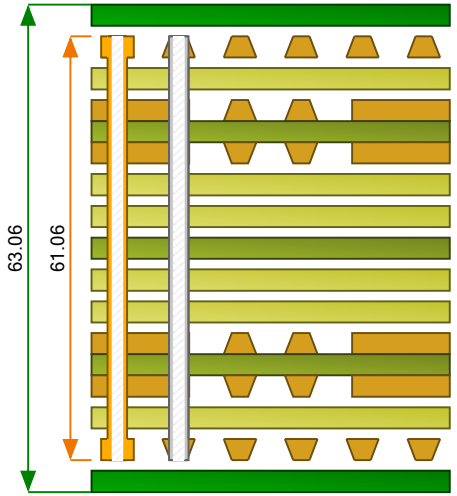
Layer	Stack up	Description	Type	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID
		Taiyo PSR 4000 HFX DI-GREEN	SolderMask	1.000			3.500	
1		Copper Foil 18 microns	Copper	2.087		100.000		1, 2, 3, 4
		Iteq IT180A Prepreg 2113 RC58	Dielectric	3.511	3.511		4.130	
2				1.260		60.000		
		Iteq IT180A 4 mil core 1/1	FR4	4.000	4.000		4.400	
3				1.260		30.000		5, 6, 7, 8
		Iteq IT180A Prepreg 106 RC71.5	Dielectric	1.750	36.826		3.790	
		Iteq IT180A Prepreg 1080 RC65	Dielectric	2.663	-		3.860	
		Iteq IT180A 28 mil core H/H	FR4	28.000	-		4.530	
		Iteq IT180A Prepreg 1080 RC65	Dielectric	2.663	-		3.860	
		Iteq IT180A Prepreg 106 RC71.5	Dielectric	1.750	-		3.790	
4				1.260		30.000		
		Iteq IT180A 4 mil core 1/1	FR4	4.000	4.000		4.400	
5				1.260		60.000		
		Iteq IT180A Prepreg 2113 RC58	Dielectric	3.511	3.511		4.130	
6		Copper Foil 18 microns	Copper	2.087		100.000		9, 10, 11, 12
		Taiyo PSR 4000 HFX DI-GREEN	SolderMask	1.000			3.500	

Copper Thickness = 9.213 | Dielectric Thickness = 51.848 | Solder Mask Thickness = 2.000 | Stack Up Thickness = 61.061 | Stack Up Thickness with Soldermask = 63.061

Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
1	1	Coated Microstrip 1B	2	0	5.300	0.000	0.000	50.140	50.000	10.000
2	1	Edge Coupled Coated Microstrip 1B	2	0	4.200	5.000	0.000	89.830	90.000	10.000
3	1	Edge Coupled Coated Microstrip 1B	2	0	4.000	7.700	0.000	99.840	100.000	10.000
4	1	Edge Coupled Coated Microstrip 2B	3	0	4.100	6.800	0.000	120.030	120.000	10.000
5	3	Offset Stripline 1B1A	2	4	4.750	0.000	0.000	49.960	50.000	10.000
6	3	Edge Coupled Offset Stripline 1B1A	2	4	4.000	6.000	0.000	90.040	90.000	10.000
7	3	Edge Coupled Offset Stripline 1B1A	2	4	3.500	8.100	0.000	99.880	100.000	10.000

StackName: Master						
Version:	Associated Documents:	Revision:	Modification:	Date of Revision:	Editor	Pag
Date: 21-01-2021						
Author:						
Department: Engg. CAM						
Site: www.hiqelectronics.com						

Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
8	3	Edge Coupled Offset Stripline 1B1A	2	4	4.000	12.000	0.000	100.160	100.000	10.000
9	6	Coated Microstrip 1B	5	0	5.300	0.000	0.000	50.140	50.000	10.000
10	6	Edge Coupled Coated Microstrip 1B	5	0	4.200	5.000	0.000	89.830	90.000	10.000
11	6	Edge Coupled Coated Microstrip 1B	5	0	4.000	7.700	0.000	99.840	100.000	10.000
12	6	Edge Coupled Coated Microstrip 2B	4	0	4.100	6.800	0.000	120.030	120.000	10.000

Notes

StackName:							
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