AM243x LAUNCH PAD

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VER	1.0

Designed for TI by Mistral Solutions Pvt Ltd

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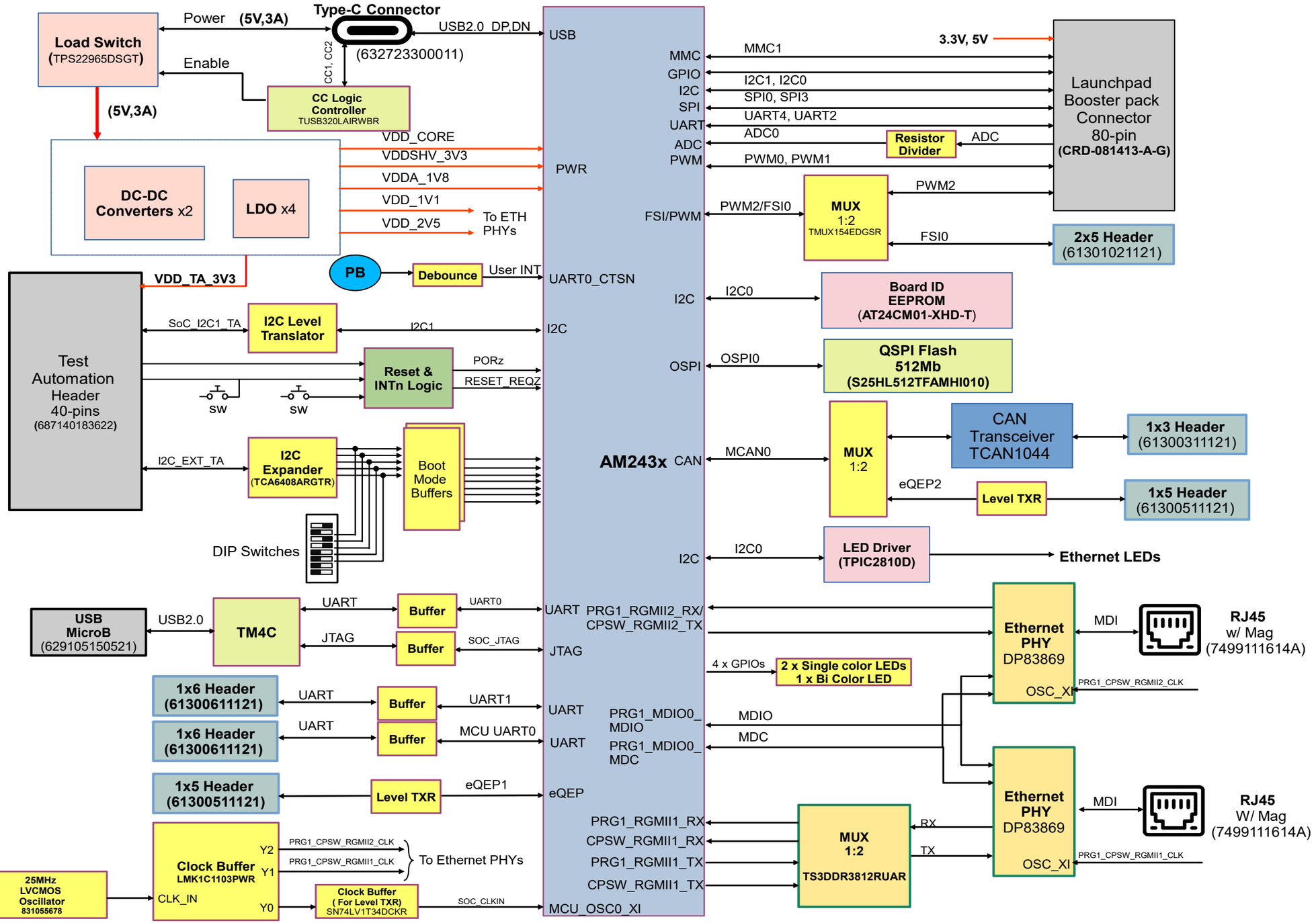
REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	15th APR 2021	Drafted from PROC109E1 v3.1	Mistral Design Team		
0.2	15th APR 2021	ADC Capacitors value is changed to 100pF from 1000pF as per TI's Review comment. Updated the FSI Header pinout as per	Mistral Design Team		
0.3	16th APR 2021	Changed the VBias supply of LDO U33 (TPS74801DRCR) to 5V from 3.3V	Mistral Design Team		
0.4	21st APR 2021	1.Changed the LDO U5 (TPS7A2518DRVR) to TPS74601PDRVR as there was an overshoot observed in the former. 2.R584 (47.5k) & R585 (21k) added as feedback resistors for U5. 3.U18 value and Mfg PN changed to XAM2434ASFGGAALX. 4.Boosterpack Connector pinouts (J2.2 & J4.10) block diagram updated as per SCH.	Mistral Design Team		
0.5	23rd APR 2021	Pull up(R588,R590)/Pull down(R589,R591) resistors option provided for BOOTMODE14 and BOOTMODE15 signals. R586 and R587 added to isolate the BOOTMODE signals after latching	Mistral Design Team		
0.6	27th APR 2021	Reverted the VDD_1V8 LDO circuit to E1 (TPS7A2518DRVR) design as the newly selected part is no stock available	Mistral Design Team		
0.7	30th APR 2021	1.Test Points(TP40-TP53) added for all probing points which had components as reference. 2.R272,R273,R274,R279,R280,R281 changed from 1K to 49.9K as per TXB0106RGYR datasheet and TI's recommendation as the strong pull up provided on signals from Header J12 and J21 ends up in improper level translation.	Mistral Design Team		
0.8	4th MAY 2021	R592-100K pull down added to MAIN_UART0_TXD signal to avoid junk values	Mistral Design Team		
0.9	24th MAY 2021	Alternates updated	Mistral Design Team		
1.0	08th JUN 2021	Baselined for E2	Mistral Design Team		

BLOCK DIAGRAM



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Title	BLOCK DIAGRAM	
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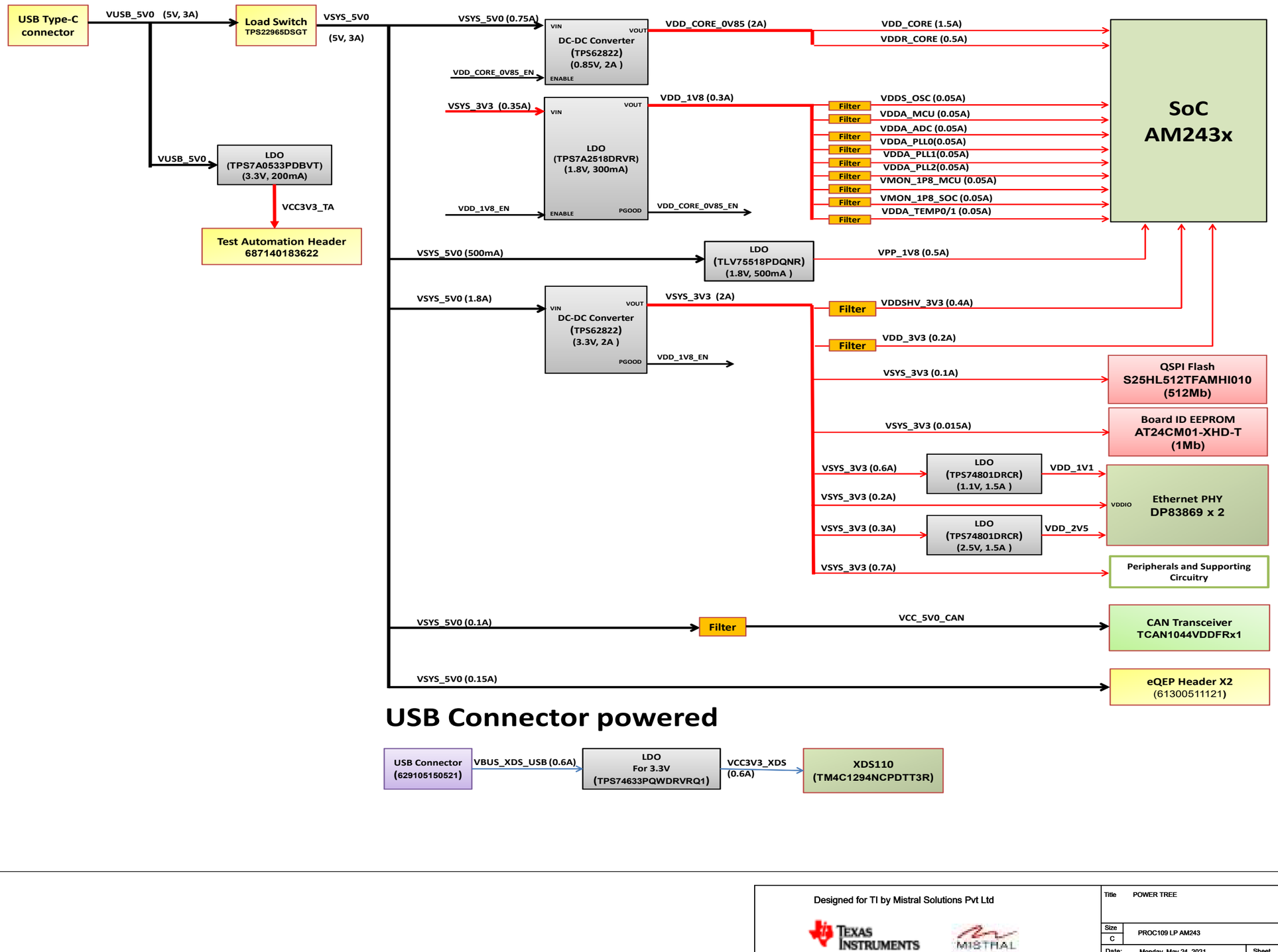
POWER TREE



USB Connector powered

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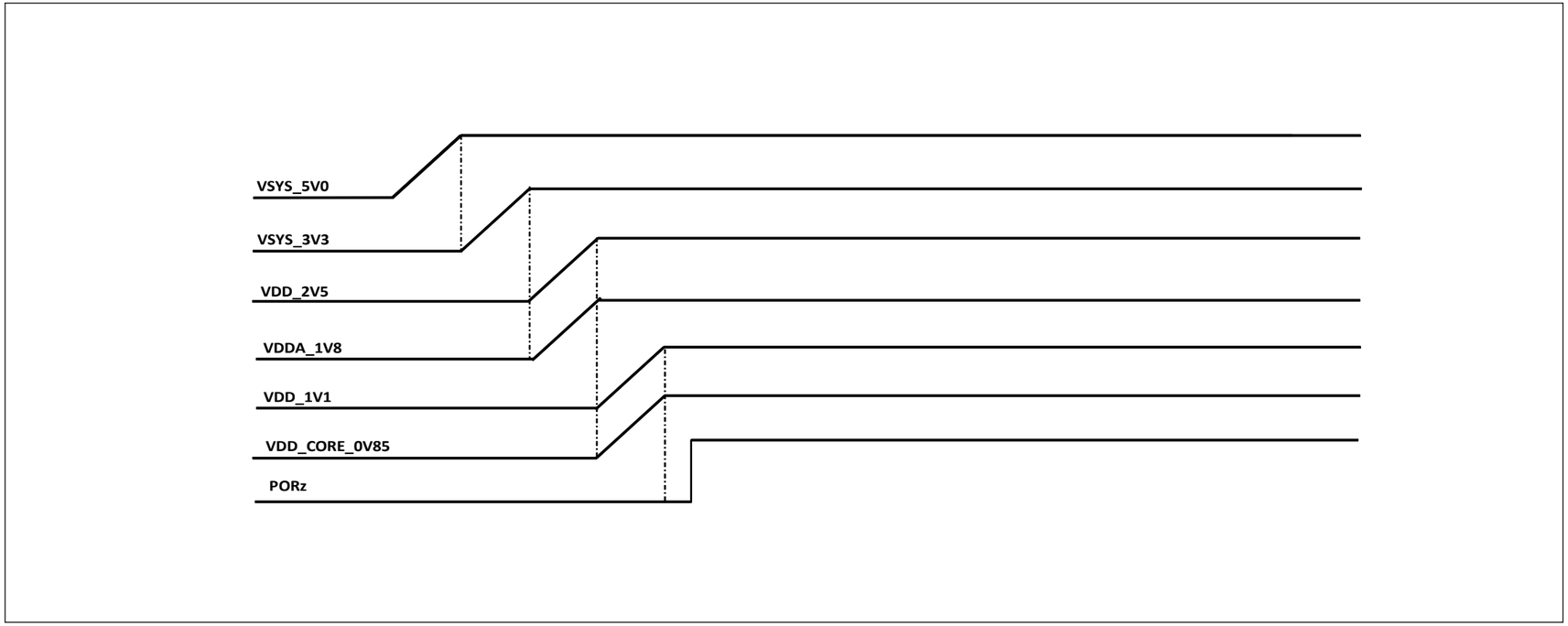
POWER ON SEQUENCE



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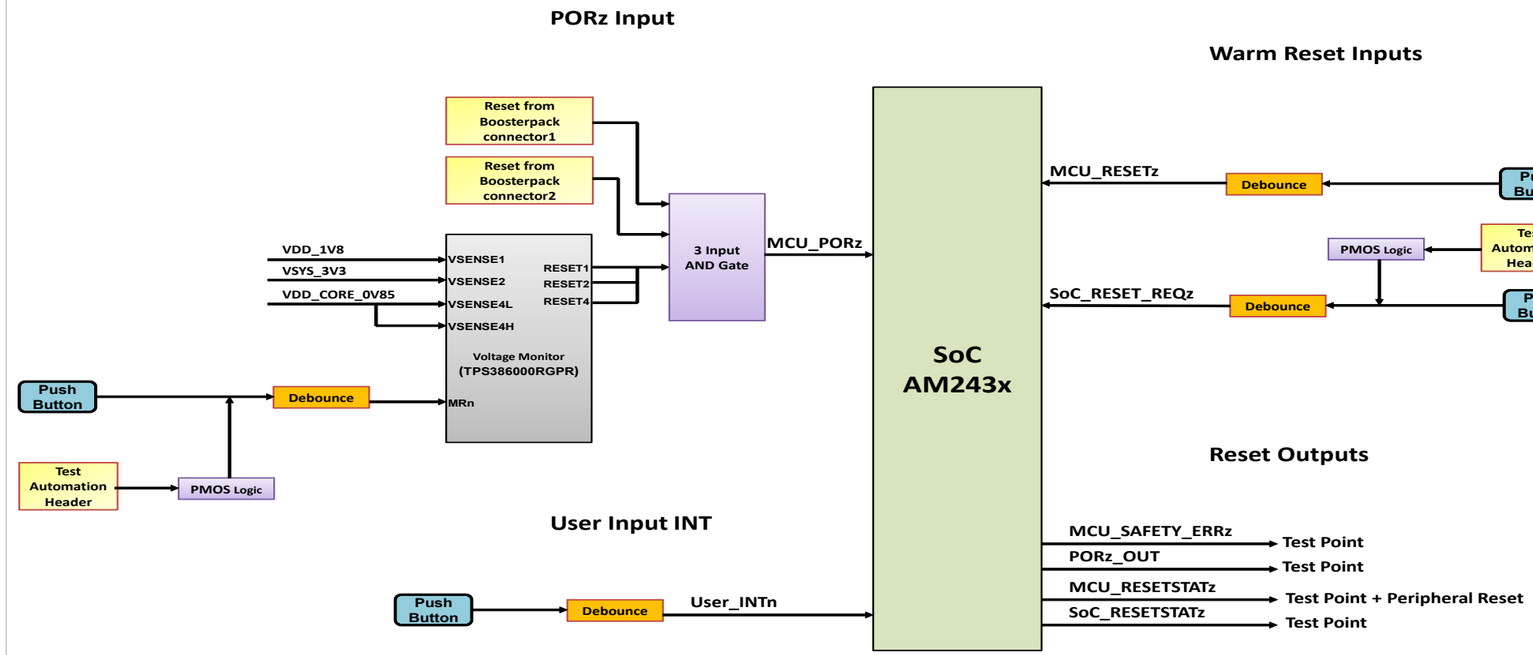
RESET ARCHITECTURE



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Title	RESET ARCHITECTURE	
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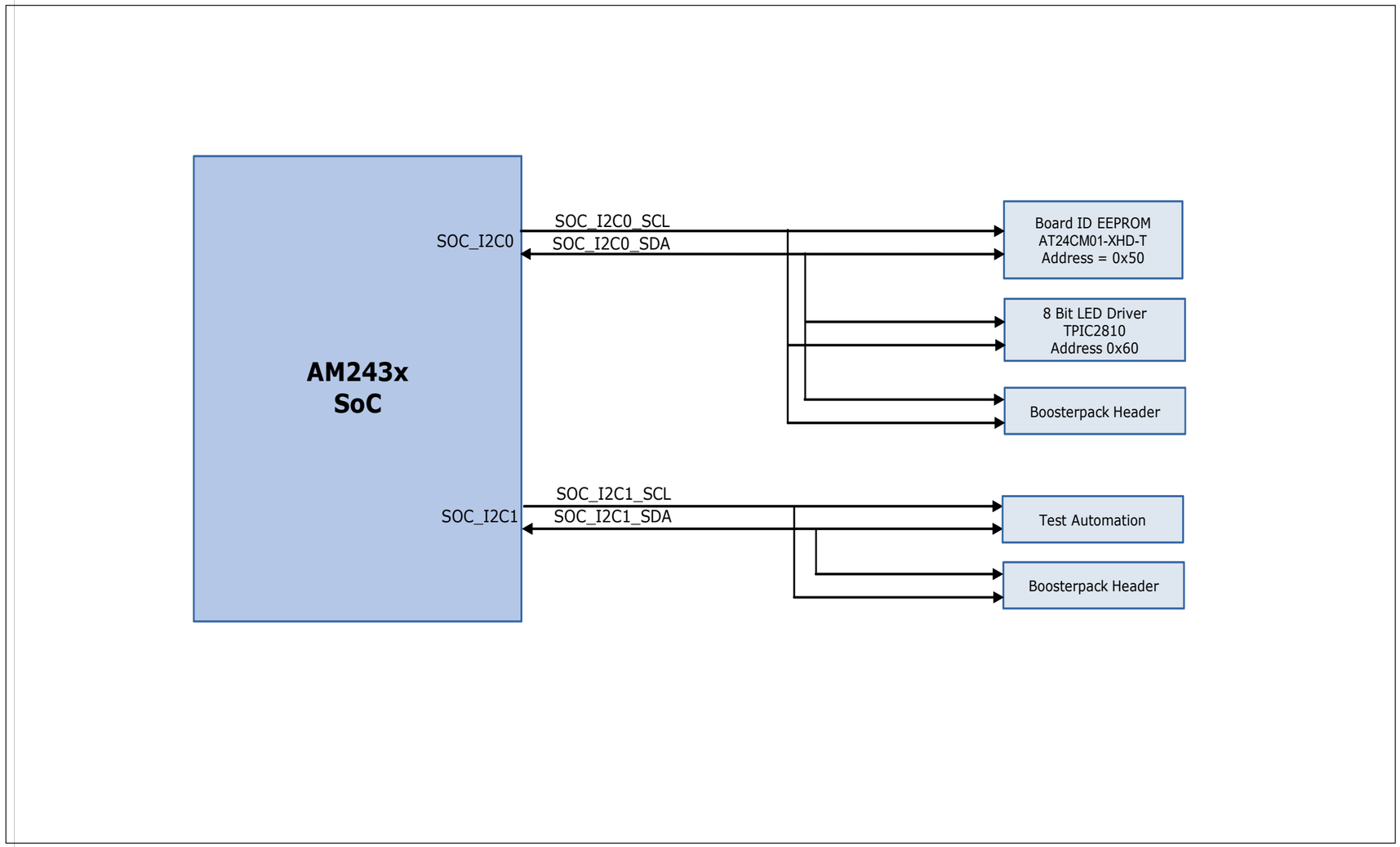
GPIO MAPPING TABLE

AM243x LP - GPIO Mapping Table						
Net name	**AM243x LP Mapping**					
	Package Signal Name	**GPIO Number**	**Input/Output**	**Default**	**State**	**Remarks**
TEST_LED1_GREEN	GPMC0_AD7	GPIO0_22	Output	PD	Active High	To Turn ON the test LED (Green)
TEST_LED2_RED	UART0_RTSN	GPIO1_55	Output	PD	Active High	To Turn ON the test LED (Red)
TEST_LED3_RED	PRG1_PRU1_GPO18	GPIO1_39	Output	PD	Active High	To Turn ON the test LED (Red) in Bicolor LED
TEST_LED4_GREEN	PRG1_PRU1_GPO19	GPIO1_38	Output	PD	Active High	To Turn ON the test LED (Green) in Bicolor LED
USER_LED1	GPMC0_AD11	GPIO0_26	Output	PD	Active High	To turn ON the User LED1 (Green)
USER_LED2	GPMC0_AD12	GPIO0_27	Output	PD	Active High	To turn ON the User LED2 (Green)
USER_INTn	UART0_CTSN	GPIO1_54	Input	PU	Active Low	User Interrupt input from Push Button Switch
OSPI0_RESET_N	OSPI0_CSN1	GPIO0_12	Output	PU	Active Low	To reset the QSPI FLASH on OSPI0 Instance
MCAN/eQEP_MUX_SEL	PRG0_PRU1_GPO8	GPIO1_28	Output	PD	NA	To select the functionality of MCAN0_RX pin as MACN0_RX or eQEP_I
FSI/BP_MUX_SEL	GPMC0_AD13	GPIO0_28	Output	PD	NA	To select the functionality of GPMC0_AD8 and GPMC0_AD9 pins as FSI_RX or PWM
MCAN0_STB	PRG0_PRU1_GPO5	GPIO1_25	Output	PU	Active Low	To put the CAN Tranciever out of Standby
PRG_CPSW_RGMII1_MUX_SEL	PRG1_PRU1_GPO5	GPIO0_70	Output	PD	NA	To select the RGMII1 path between PRG and CPSW
GPIO_RGMII1_PHY_RSTn	PRG1_PRU1_GPO8	GPIO0_73	Output	PU	Active Low	To Reset the RGMII1 Ethernet PHY
GPIO_RGMII2_PHY_RSTn	PRG1_PRU1_GPO18	GPIO0_20	Output	PU	Active Low	To Reset the RGMII2 Ethernet PHY
PRG1_CPSW_RGMII_INTn	PRG1_PRU1_GPO19	GPIO0_84	Input	PU	Active Low	Interrupt signal from Both RGMII1 & RGMII2 Ethernet PHYs
GPIO0_50	PRG1_PRU0_GPO5	GPIO0_50	IO	NA	NA	GPIO Connected to Booster pack header
VPP_1V8_REG_EN	PRG1_PRU0_GPO8	GPIO0_53	Output	PD	Active High	To enable the VPP Regulator for eFUSE Programming

I2C TREE



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Title	I2C TREE	
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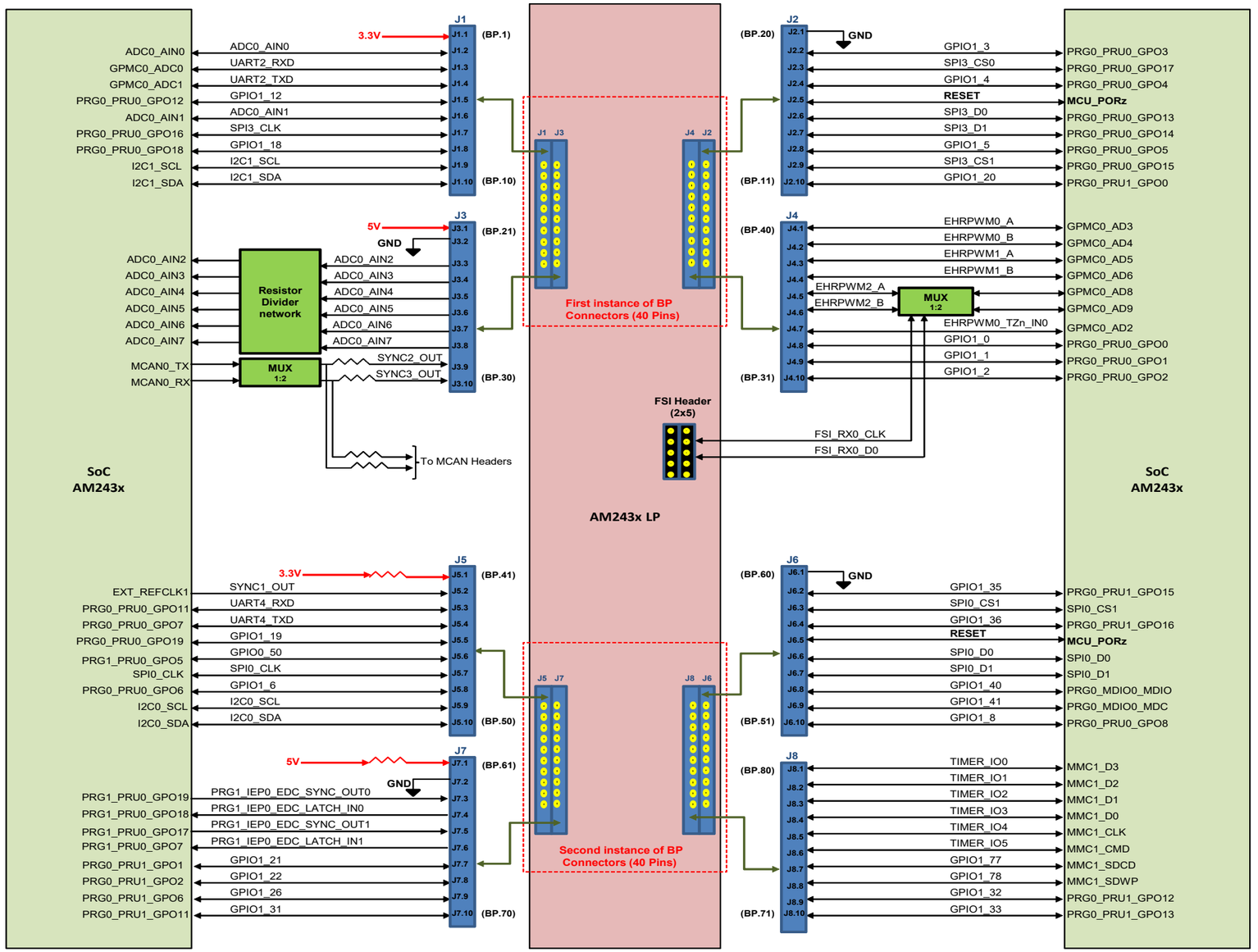
BOOSTERPACK CONNECTOR PINOUTs



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Title	BOOSTERPACK CONNECTOR PINOUTS		
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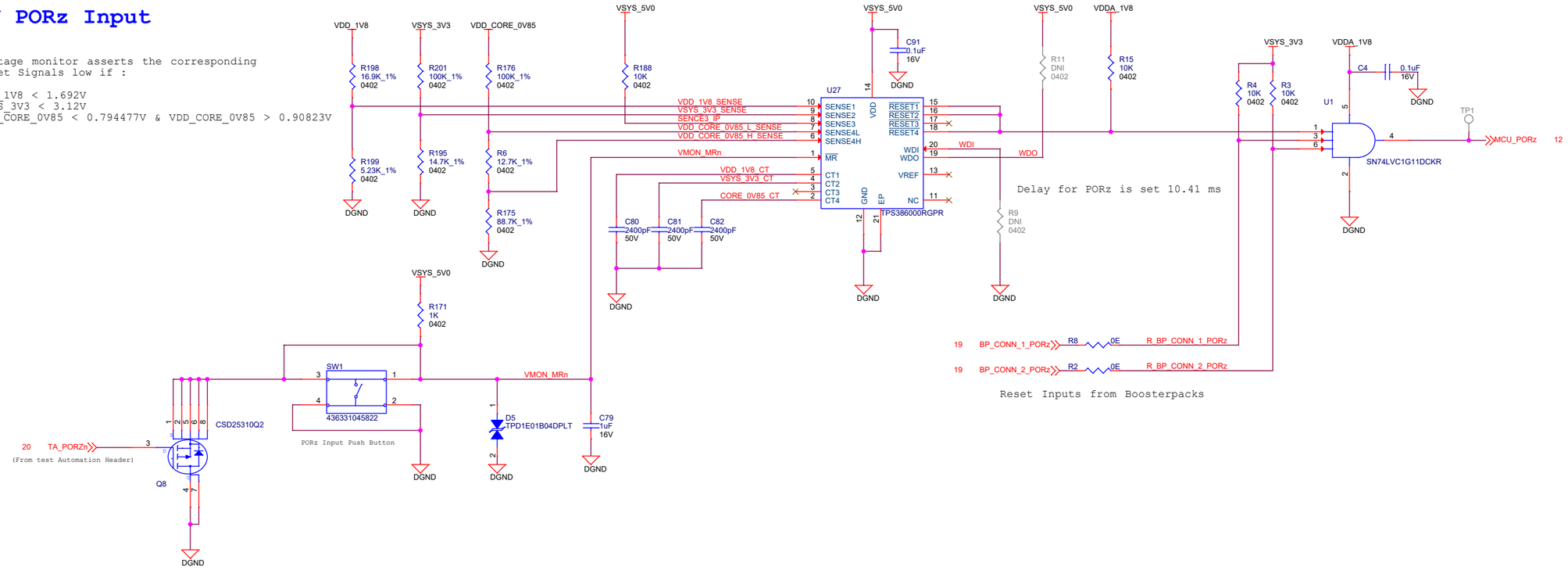
Reset Inputs

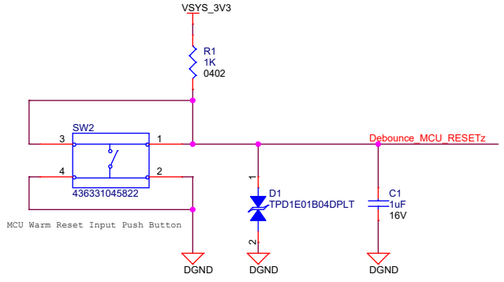
MCU PORz Input

Voltage monitor asserts the corresponding reset Signals low if :

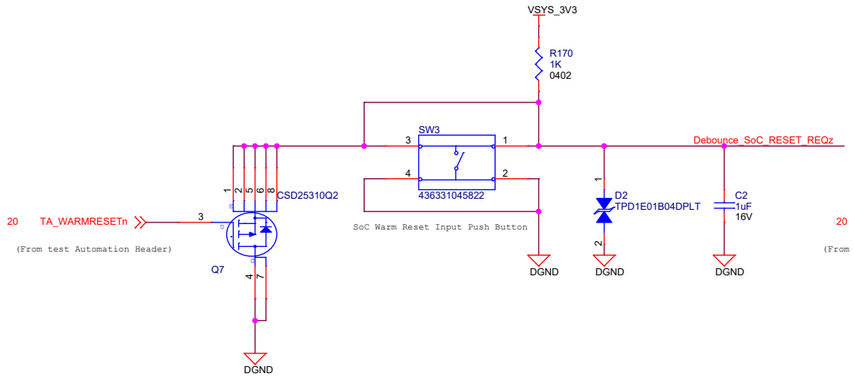
VDD_1V8 < 1.692V
VSYS_3V3 < 3.12V
VDD_CORE_0V85 < 0.794477V & VDD_CORE_0V85 > 0.90823V



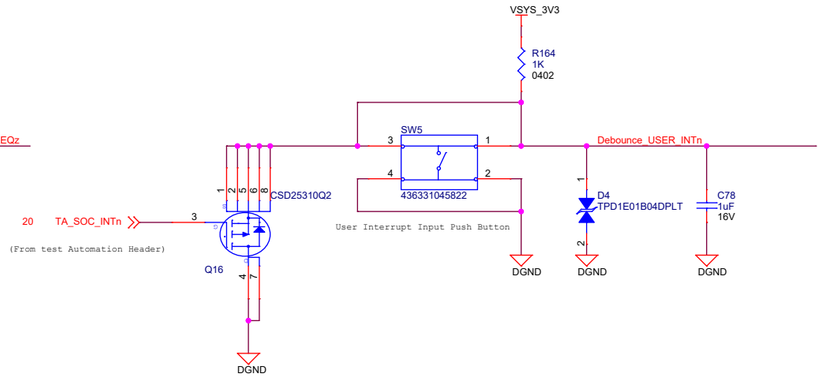
MCU Warm Reset Input



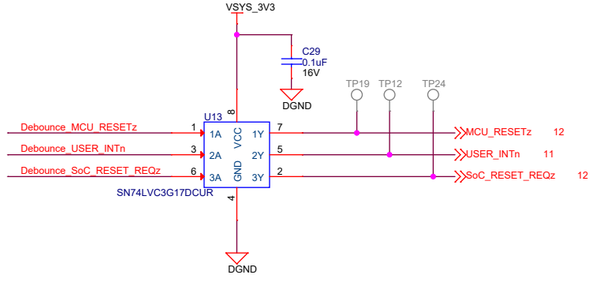
SoC Warm Reset Input



User Push Button



DEBOUNCE CIRCUIT



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Title	RESET INPUTs	
Size	PROC109 LP AM243	Rev
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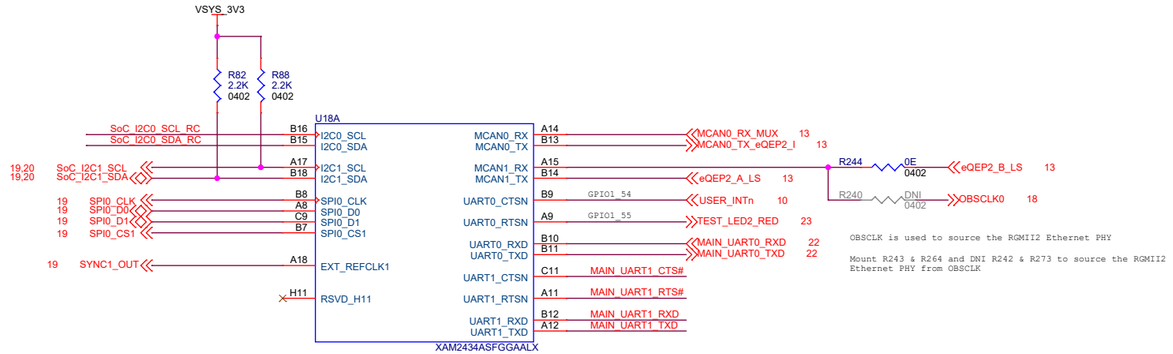
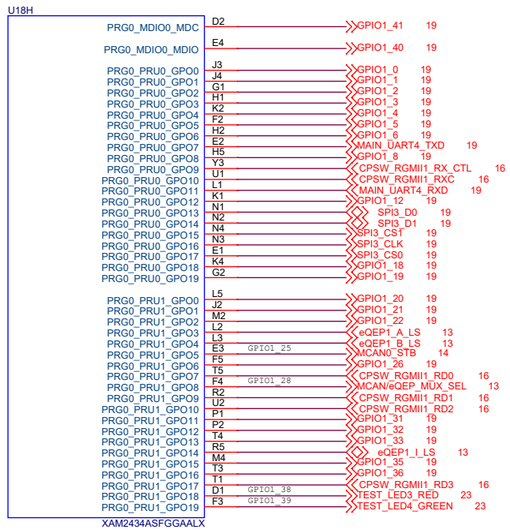
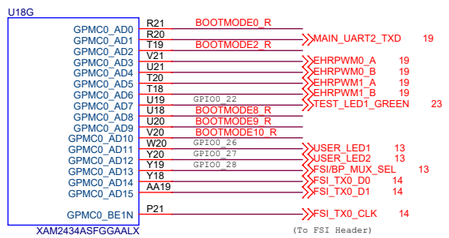
SoC Blocks

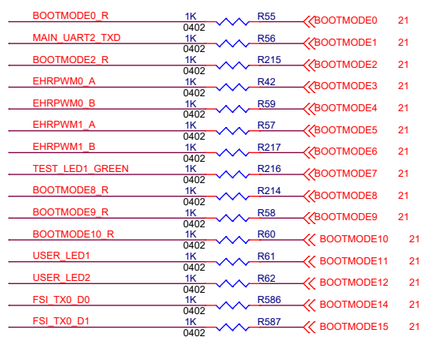






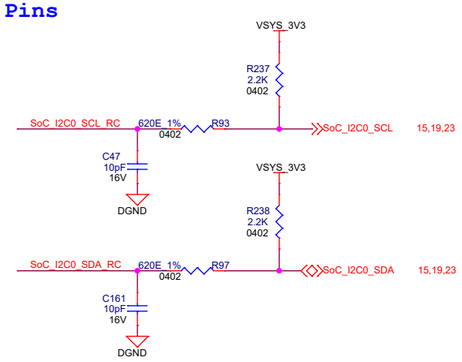
Note : No Input to SoC should be driven from others while Booting

BOOT Mode Pins



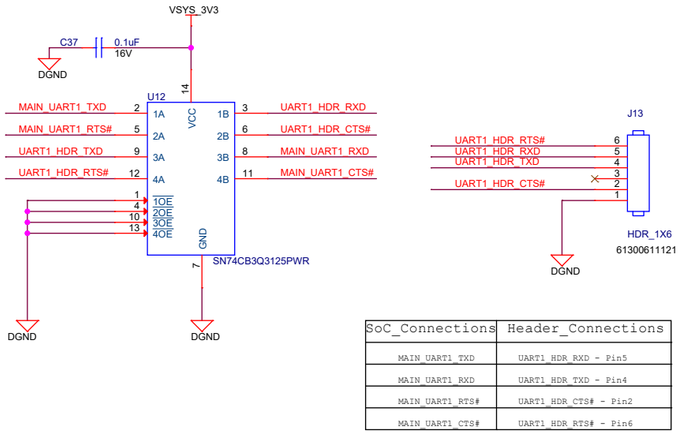
Note: 1K resistors are used to isolate the BOOTMODE control logic after the value is latched

LPF For I2C Pins



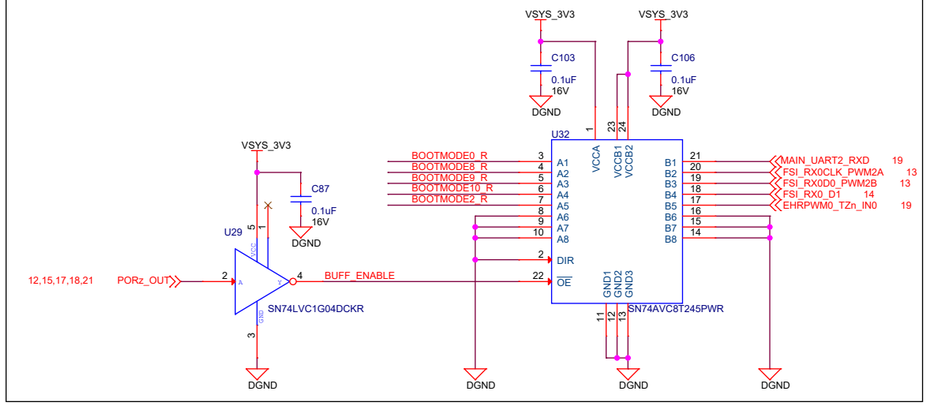
LPF Designed for 25MHz Cutoff
Have to change resistor and capacitor values accordingly

UART Buffer & EXT UART HDR for UART1



SoC_Connections	Header_Connections
MAIN_UART1_TXD	UART1_HDR_RXD - Pin5
MAIN_UART1_RXD	UART1_HDR_TXD - Pin4
MAIN_UART1_RTS#	UART1_HDR_CTS# - Pin2
MAIN_UART1_CTS#	UART1_HDR_RTS# - Pin6

Isolation Buffer for Bootmode Input pins



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Title	SOC1		
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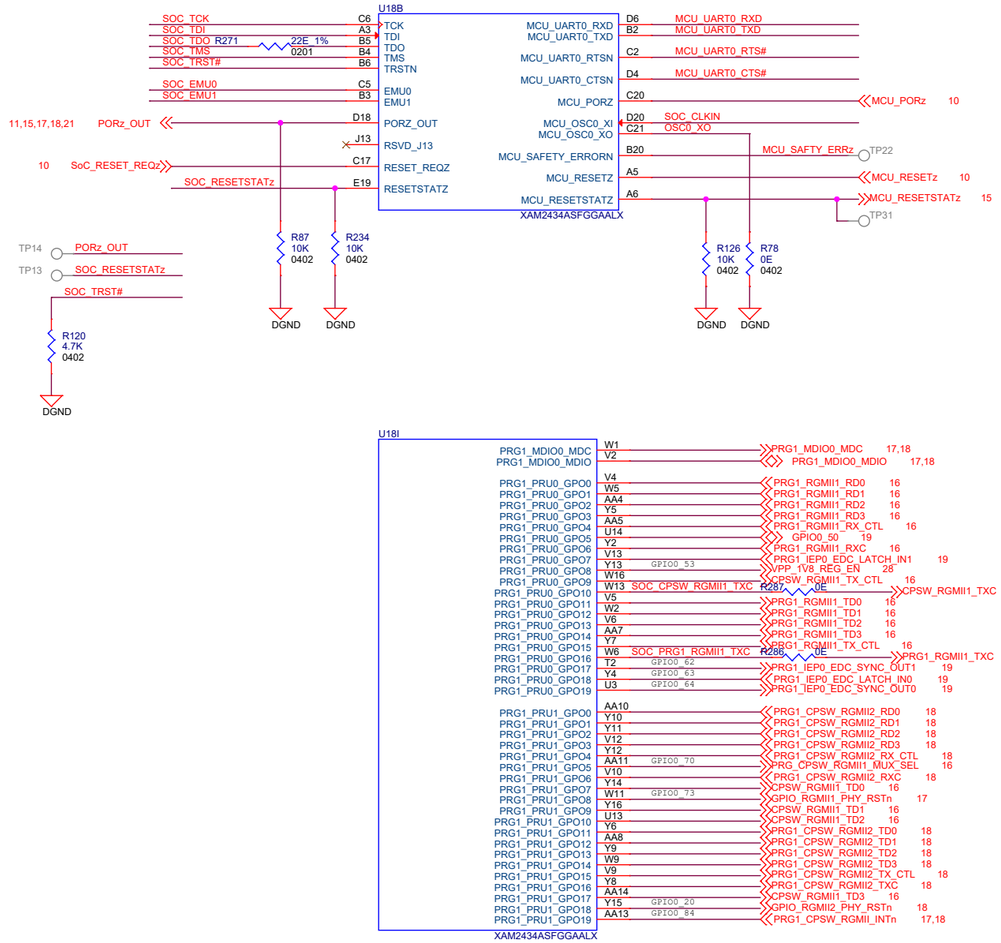
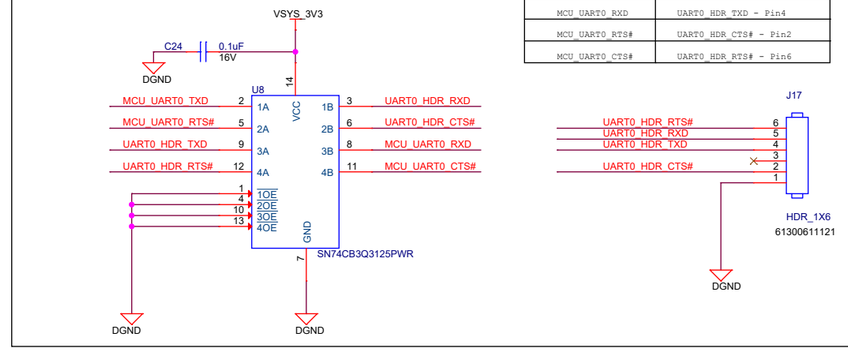
SoC Blocks

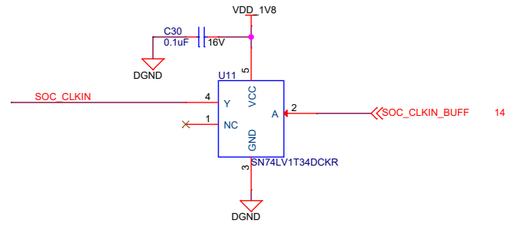


MCU UART0 Buffer & Header

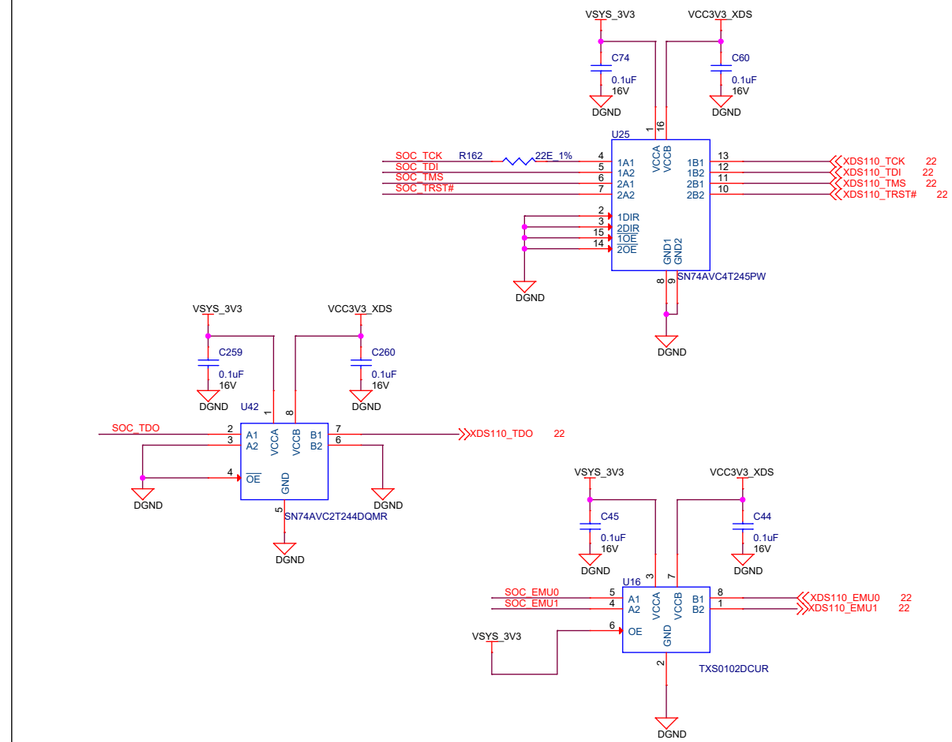
SoC_Connections	Header_Connections
MCU_UART0_TXD	UART0_HDR_RXD - Pin5
MCU_UART0_RXD	UART0_HDR_TXD - Pin4
MCU_UART0_RTS#	UART0_HDR_CTS# - Pin2
MCU_UART0_CTS#	UART0_HDR_RTS# - Pin6



SoC Clock Buffer



XDS110 JTAG Isolation Buffer



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Title	SOC2	
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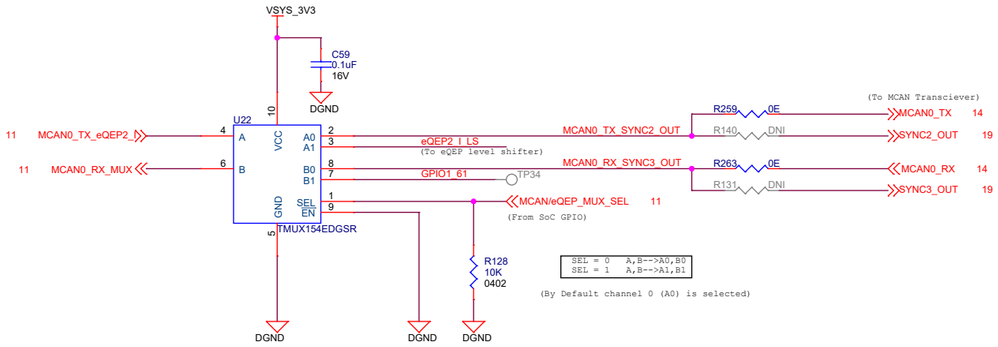
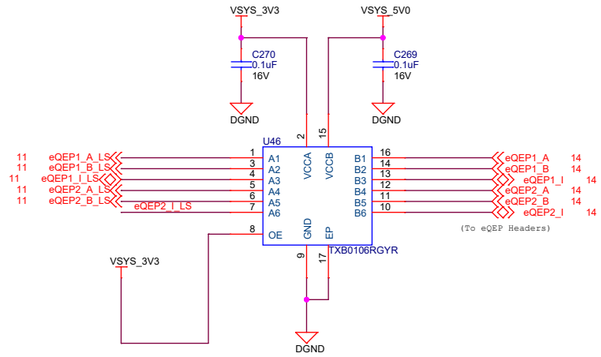
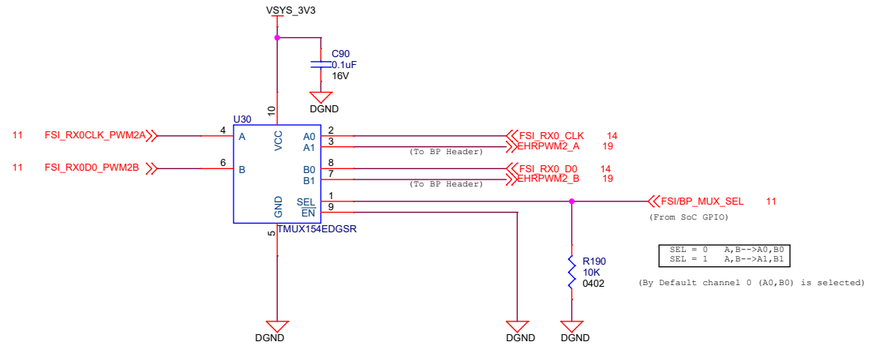
MCAN/eQEP FET Switch



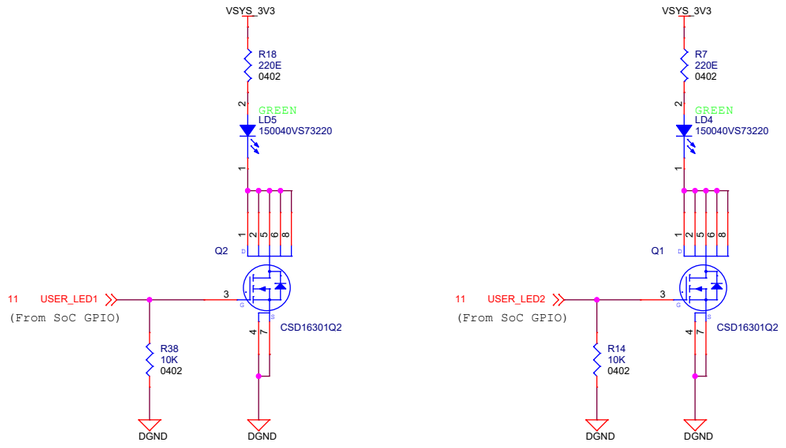
eQEP Level Shifter



FSI/BP FET Switch



User Test LEDs



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Title	MCAN_eQEP_FSI_MUX & USER LEDs	
Size C	PROC109 LP AM243	Rev E2
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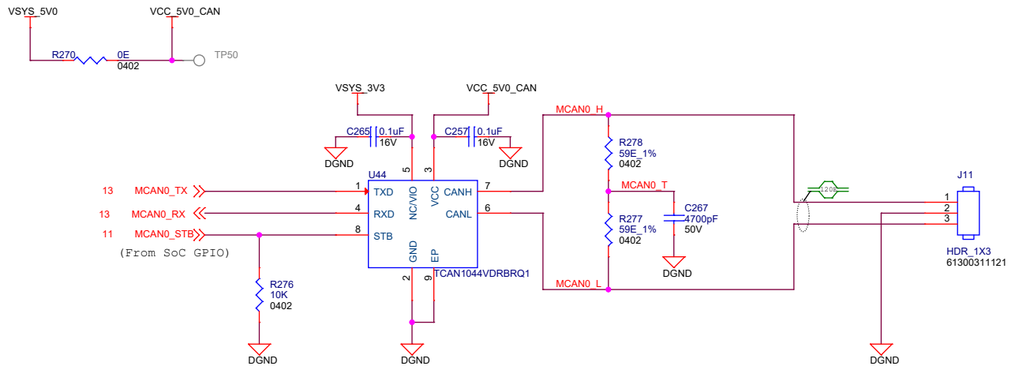
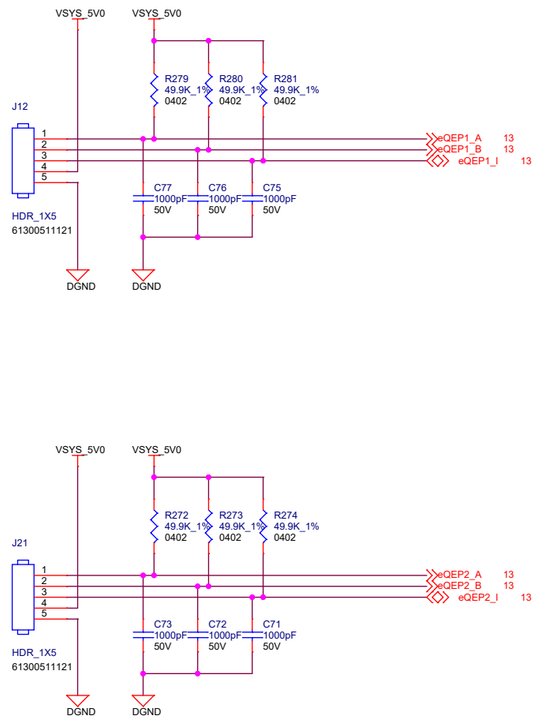
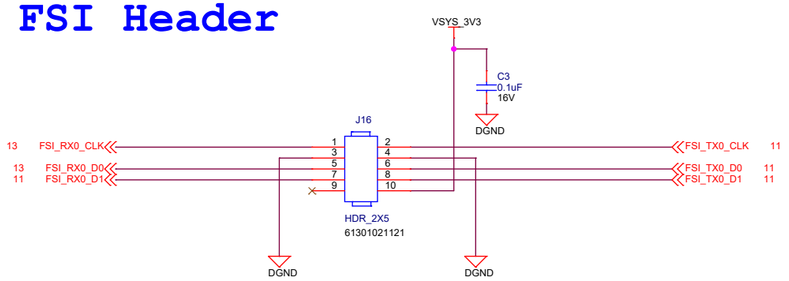
MCAN Transceiver & Header



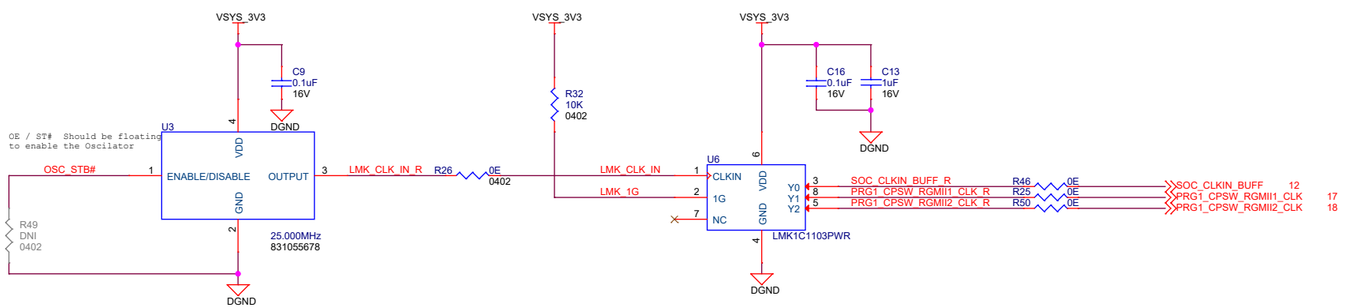
eQEP Headers



FSI Header



SoC and Ethernet PHY Clock Buffer



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Title	CAN_eQEP_FSI_HEADERs & CLOCK BUFFER	
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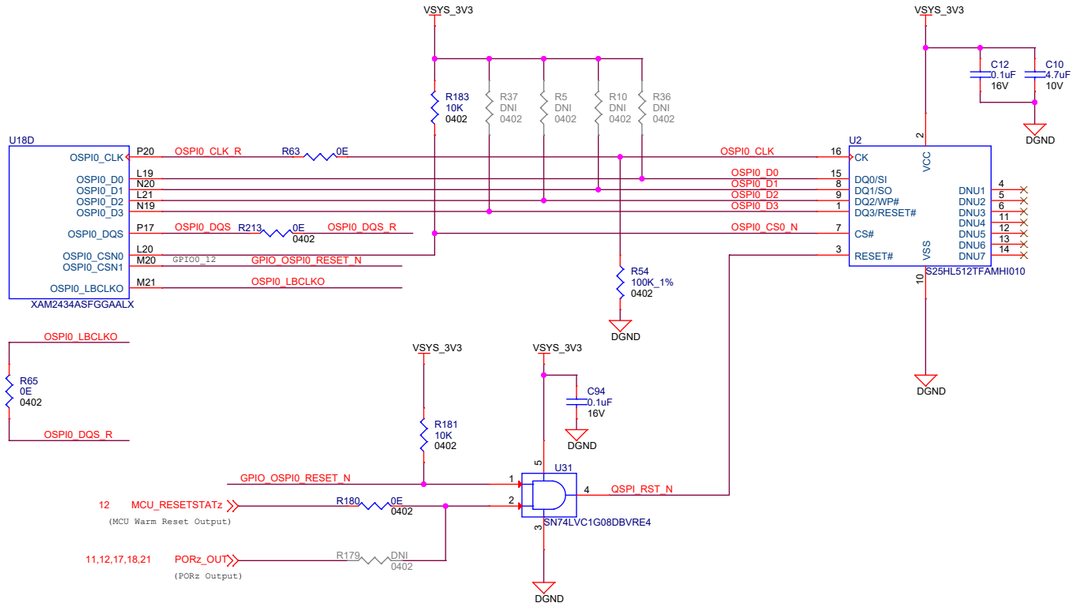
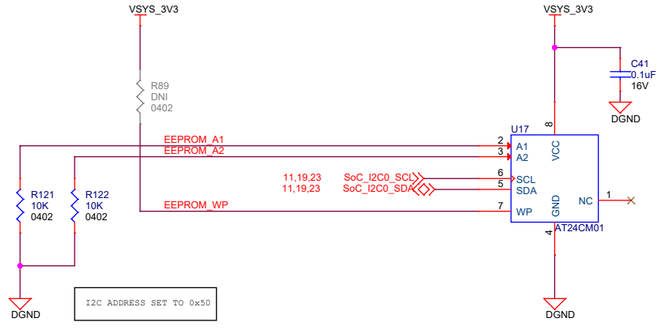
QSPI FLASH



Board ID EEPROM



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Title	QSPI_BOARD_ID_EEPROM	
Size C	PROC109 LP AM243	Rev E2
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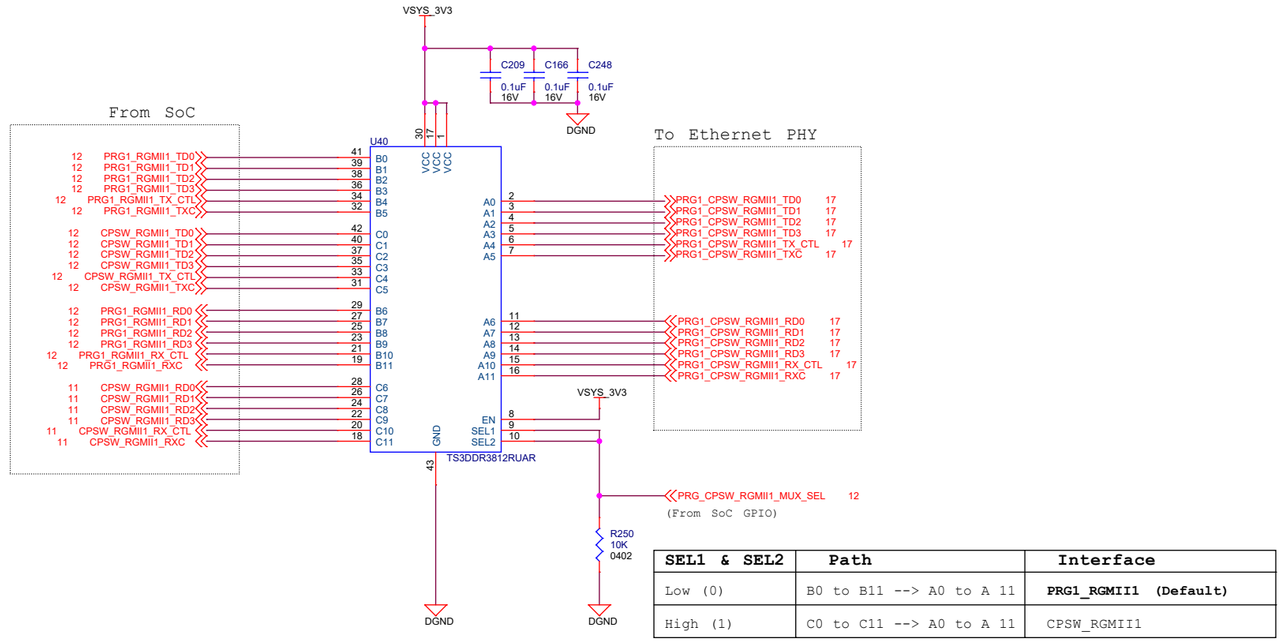
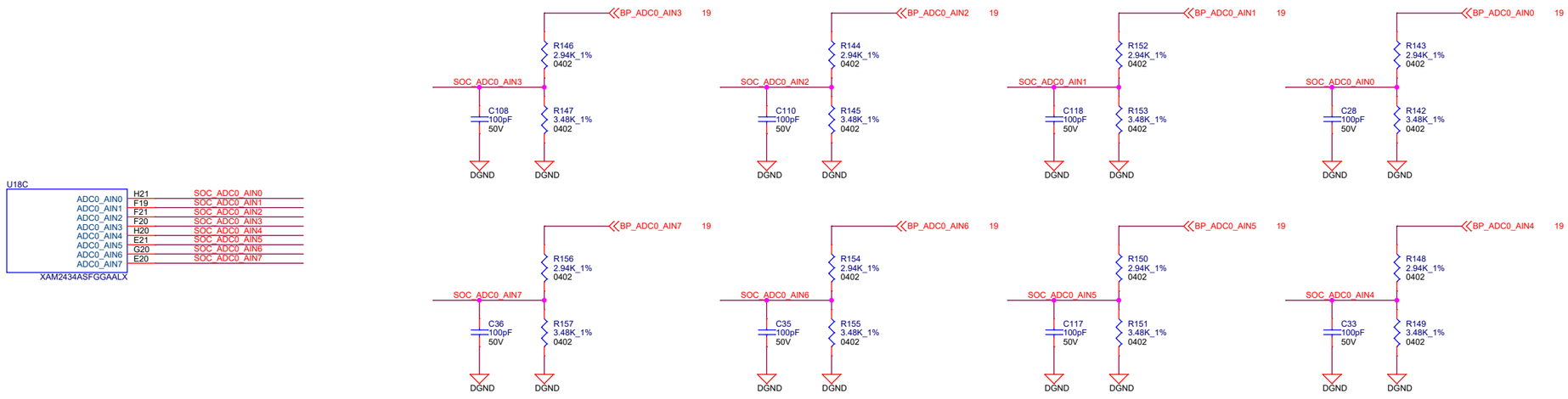
CPSW or PRG RGMII1 Ethernet Data MUX



SEL1 & SEL2	Path	Interface
Low (0)	B0 to B11 --> A0 to A 11	**PRG1_RGMII1 (Default)**
High (1)	C0 to C11 --> A0 to A 11	CPSW_RGMII1

ADC Inputs



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Title	ETHERNET DATA MUX & ADC INPUTS	
Size C	PROC109 LP AM243	Rev E2
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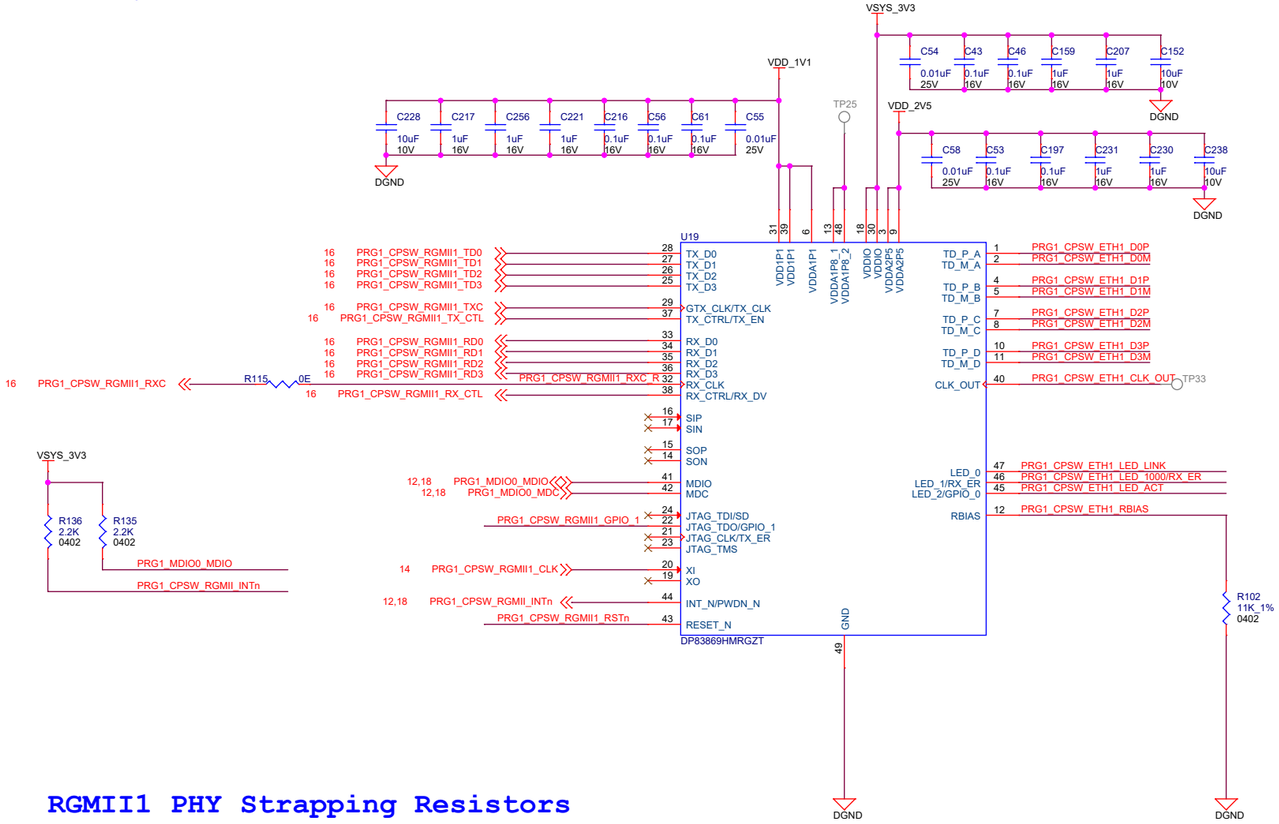
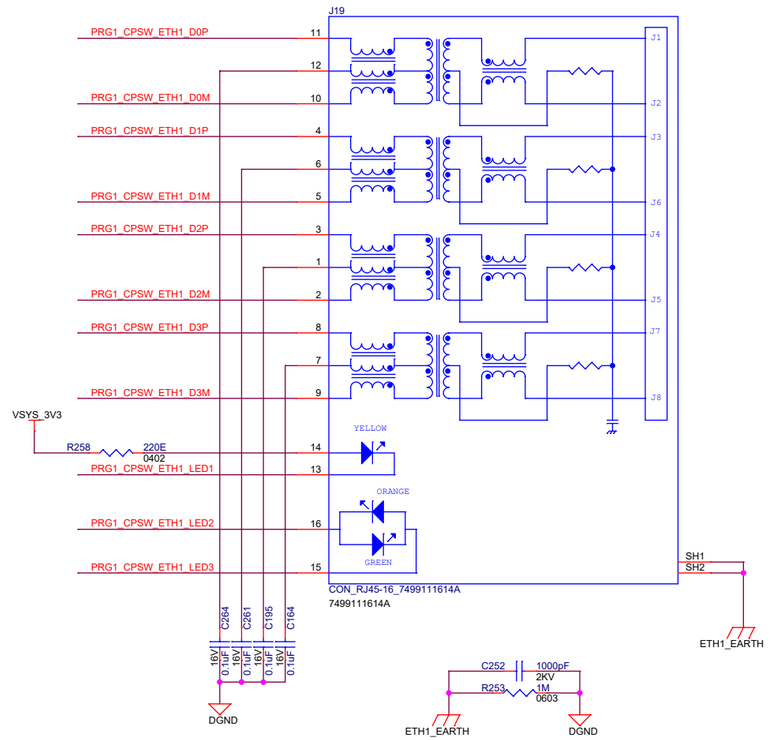
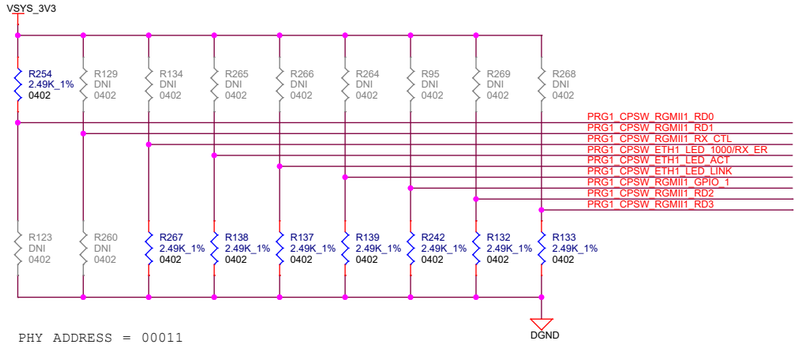
PRG / CPSW RGMII1 Ethernet PHY



RJ45 Connector with Integrated Magnetics



RGMII1 PHY Strapping Resistors

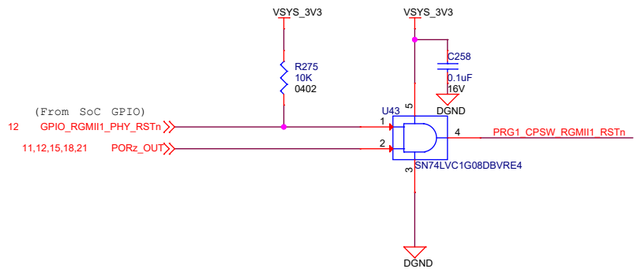


PHY ADDRESS = 00011

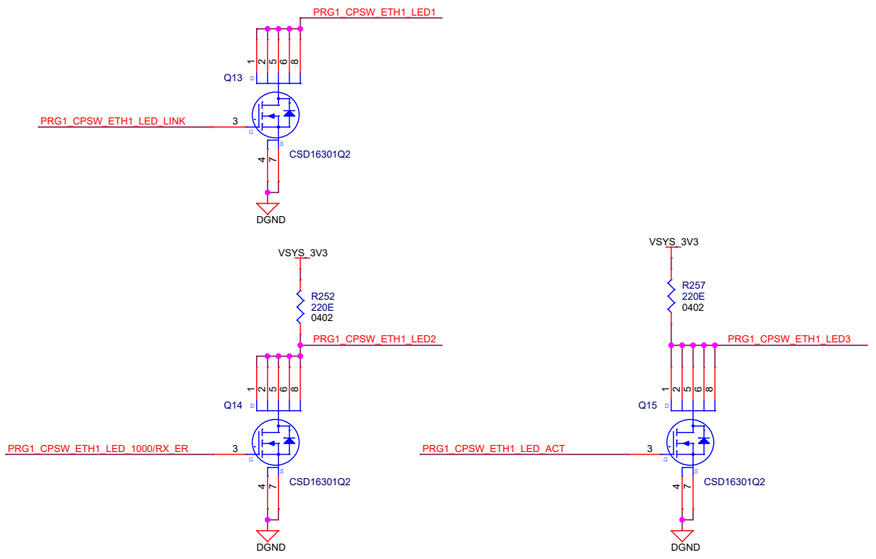
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X

RGMII to Copper (1000BaseT/100Base-TX/10Base-Te)

RGMII1 PHY Reset



RGMII1 PHY Speed & Activity LED Drivers



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Title	PRG/CPSW RGMII1 ETHERNET PHY	
Size C	PROC109 LP AM243	Rev E2
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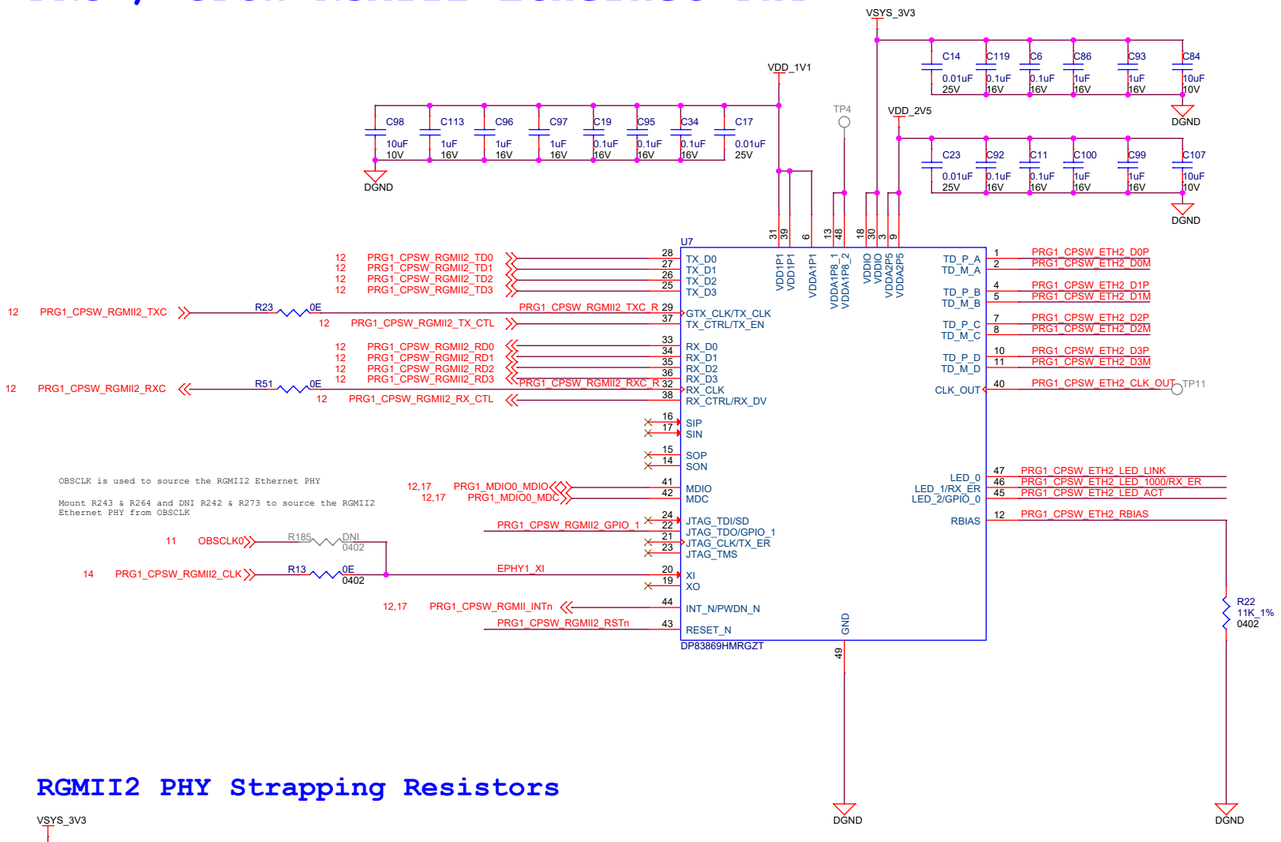
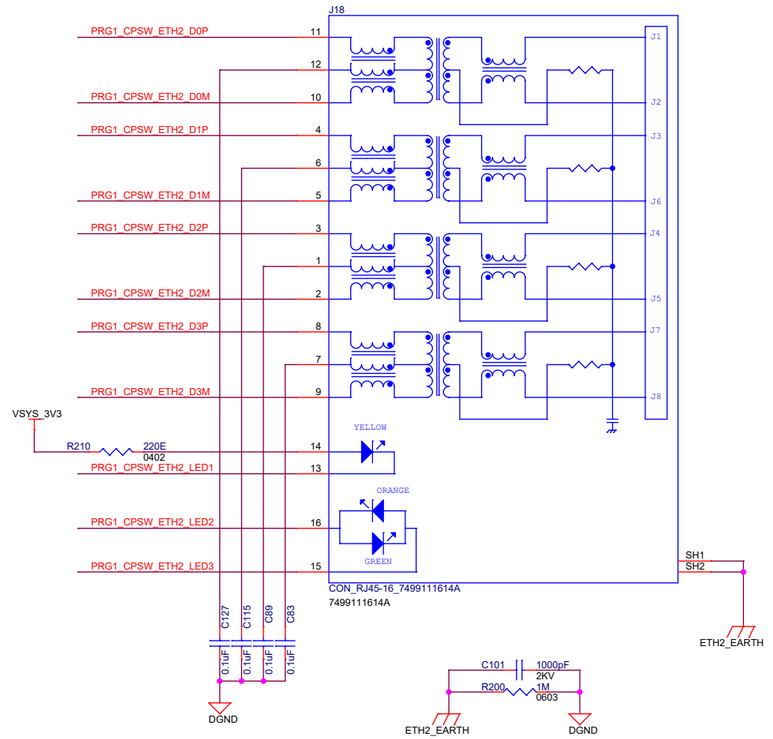
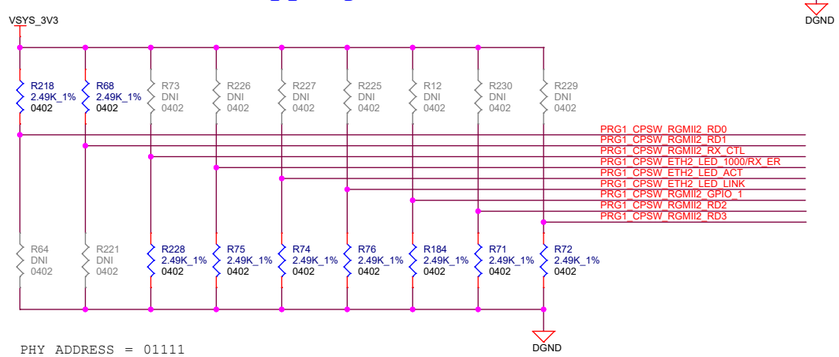
PRG / CPSW RGMII2 Ethernet PHY



RJ45 Connector with Integrated Magnetics



RGMII2 PHY Strapping Resistors

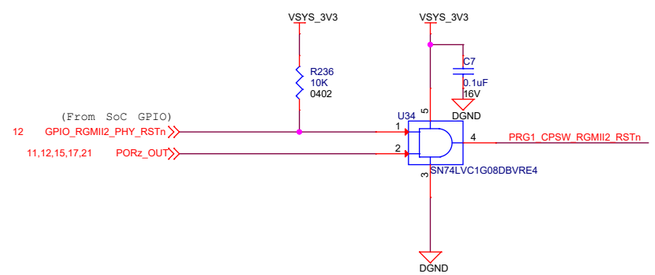


PHY ADDRESS = 01111

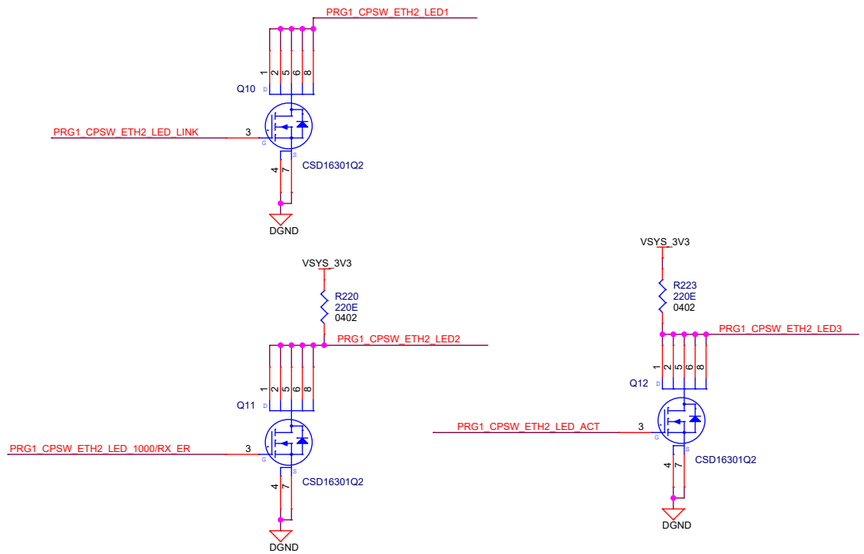
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X

RGMII to Copper (1000BaseT/100Base-TX/10Base-Te)

RGMII2 PHY Reset



RGMII2 PHY Speed & Activity LED Drivers



Designed for TI by Mistral Solutions Pvt Ltd

Title	PRG/CPSW RGMII2 ETHERNET PHY	
Size C	PROC109 LP AM243	Rev E2
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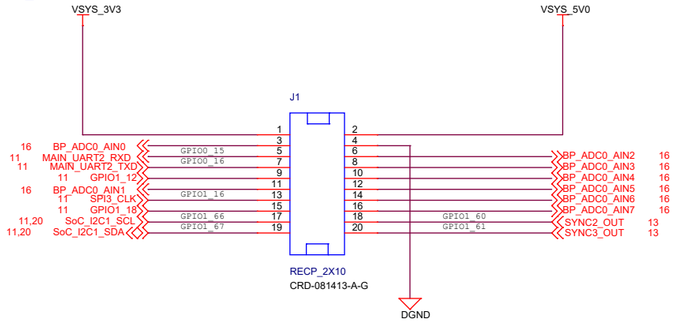
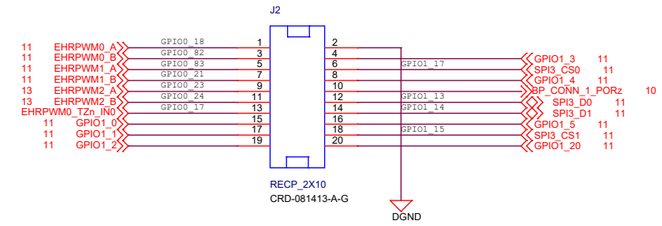
Booster Pack Header

Boosterpack Header Site - 1





Boosterpack Header Site - 2

SoC MMC1 Connection to BP Header

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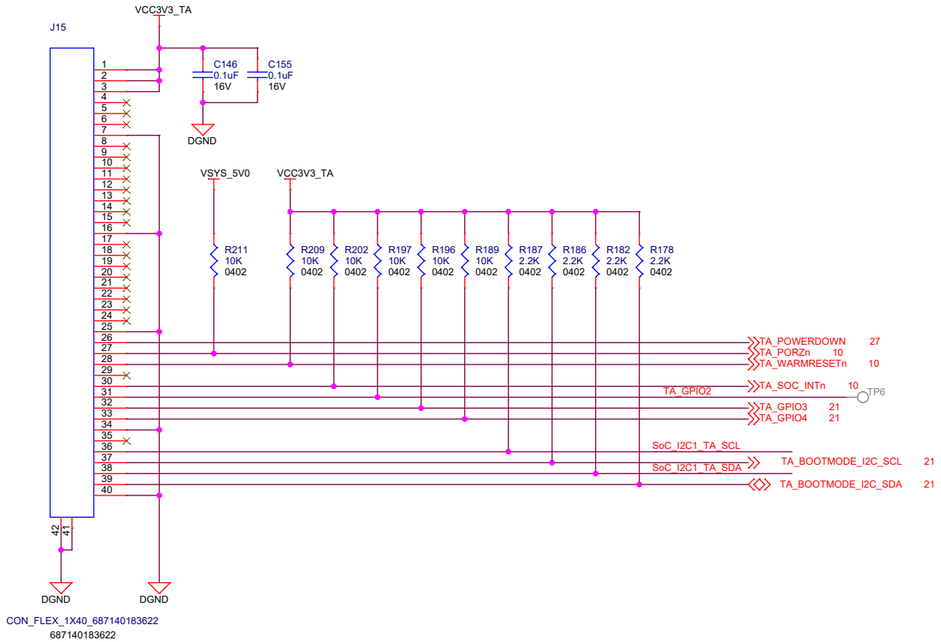
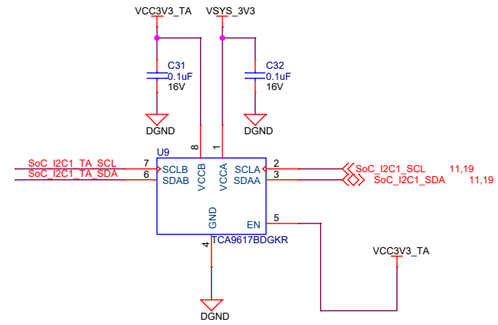
Title	BOOSTERPACK CONNECTOR	
Size	PROC109 LP AM243	Rev
C		E2
Date:	Monday, May 24, 2021	Sheet 19 of 29

40 - Pin Test Automation Header



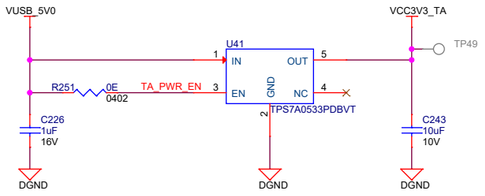
I2C Buffer for TA Header



Test Automation GPIO Mappping

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Powerdown the Board	OUTPUT	External Pullup
TA_PORZn	Used to Reset the SoC PORZ	OUTPUT	External Pullup
TA_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TA_GPIO3	Used to Disable the BOOTMODE Buffer	OUTPUT	External Pullup
TA_GPIO4	Used to Reset the BOOTMODE IO Expander	OUTPUT	External Pullup
TA_SOC_INTn	Interrupt to SoC	OUTPUT	External Pullup

Test Automation Board Power



3.3V @ 200mA

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Title	TEST AUTOMATION HEADER	
Size C	PROC109 LP AM243	Rev E2
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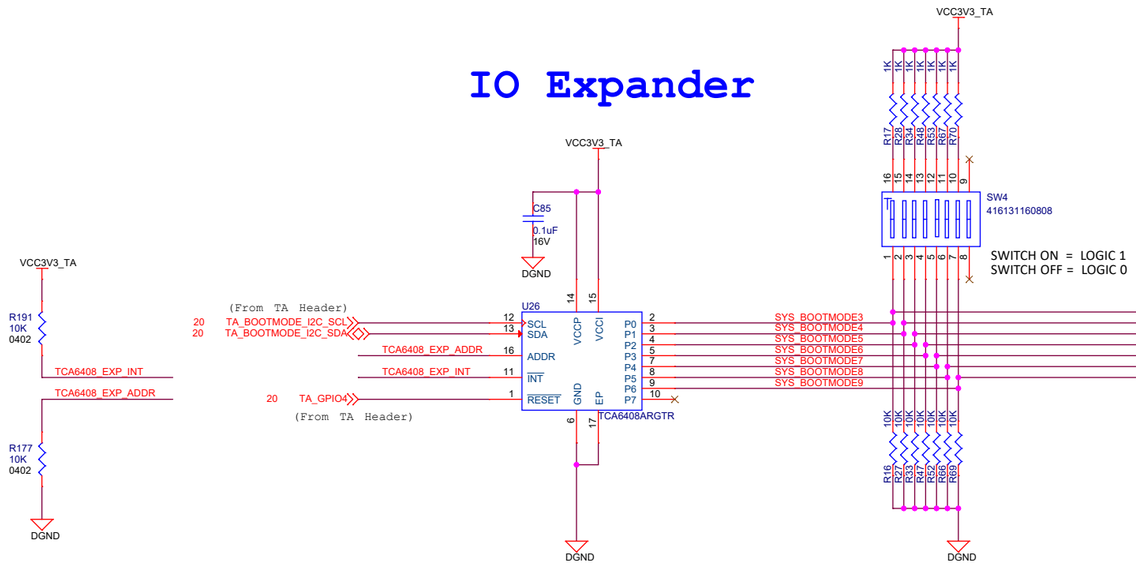
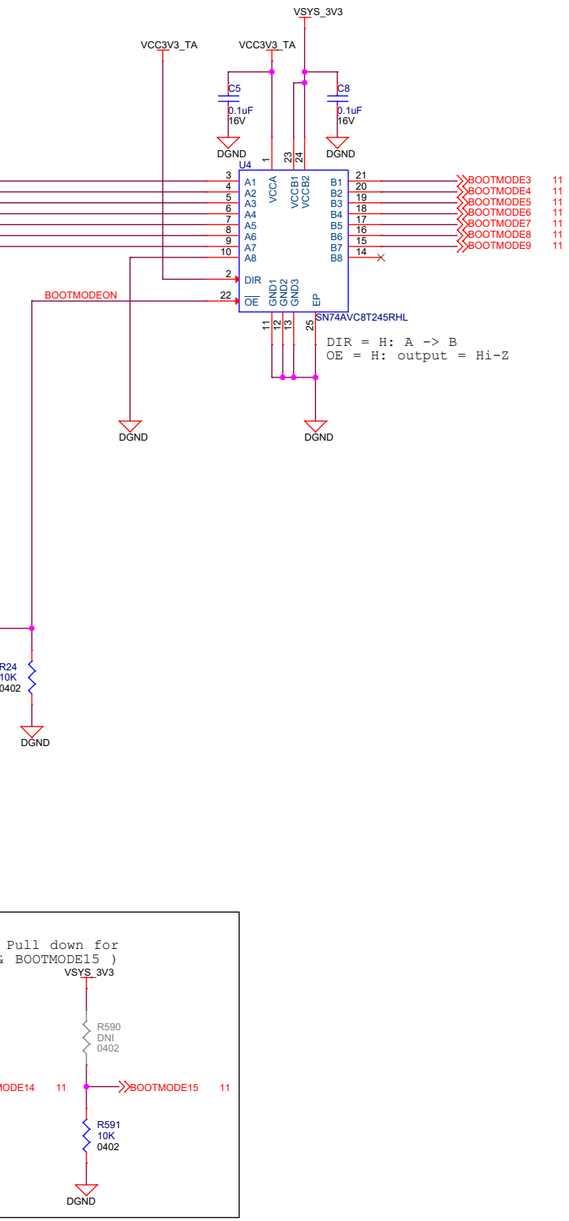
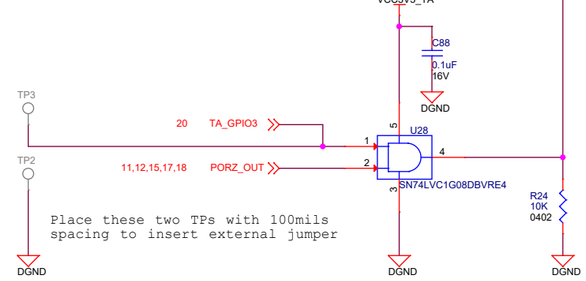
BOOT Mode Switch

IO Expander



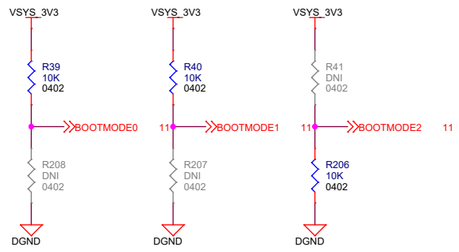
BOOT Mode Buffer



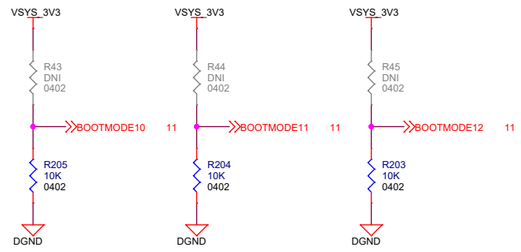


AM243x LP - Boot-Mode selection table							
Boot Modes Supported	**SW4.1**	**SW4.2**	**SW4.3**	**SW4.4**	**SW4.5**	**SW4.6**	**SW4.7**
QSPI FLASH	0	1	0	0	0	1	0
MMC1/SD Card	0	0	0	1	0	0	1
UART	1	1	1	0	0	0	0
USB - DFU	0	1	0	1	0	0	0
No Boot	1	1	1	1	0	0	0

BOOT_MODE0, 1 & 2 are used to select system Clock frequency
(Default 25 MHz is selected)



BOOT_MODE10, 11 & 12 are used to select Back-up Boot Mode
(By Default No Back-up Boot mode is selected)



TBD
(Pull up or Pull down for
BOOTMODE14 & BOOTMODE15)

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Title	BOOT MODE BUFFER & SWITCHES	
Size C	PROC109 LP AM243	Rev E2
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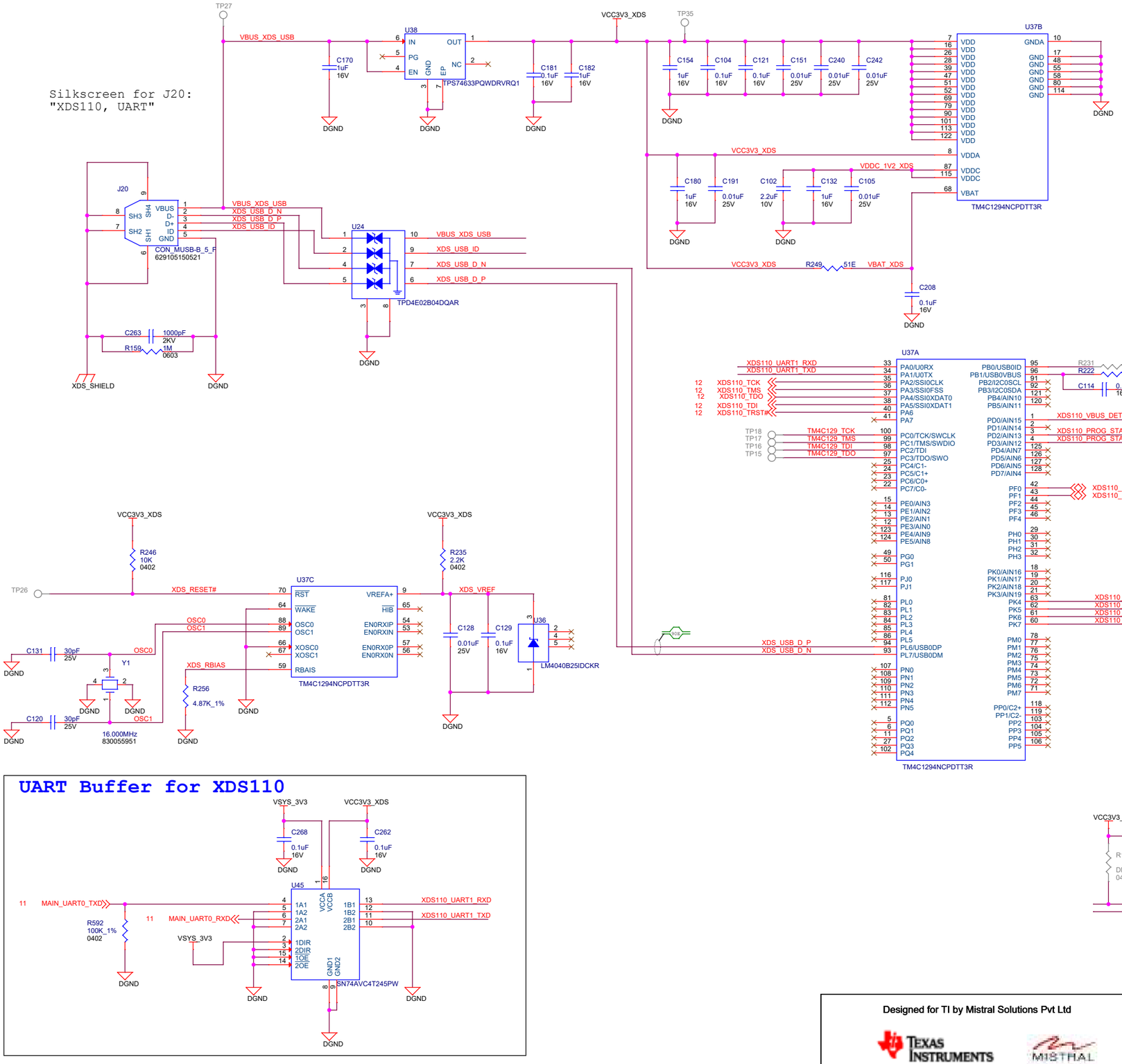
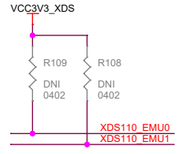
XDS110 Debugger

Silkscreen for J20:
"XDS110, UART"



UART Buffer for XDS110



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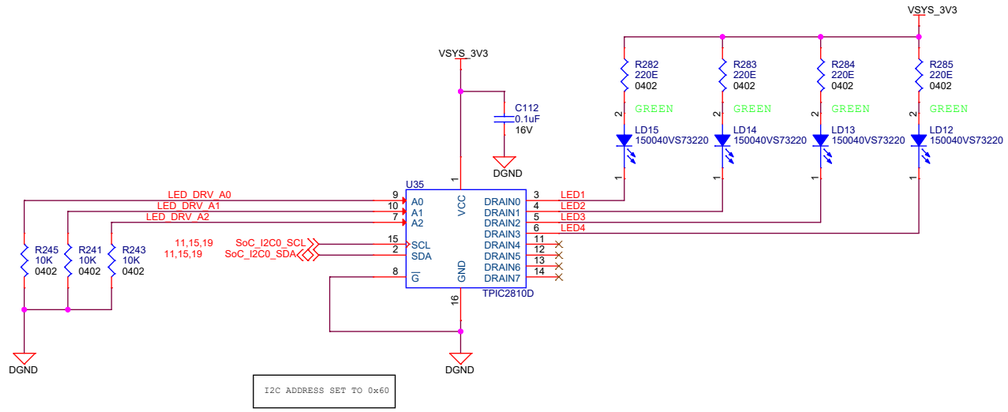
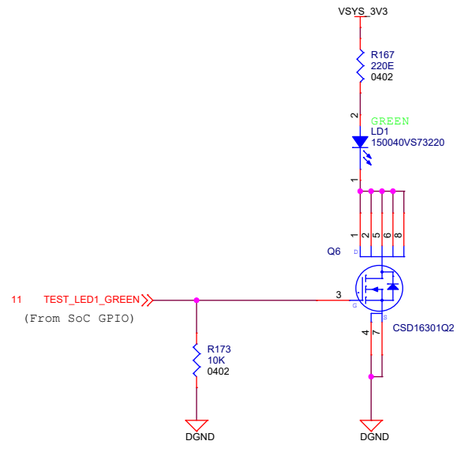
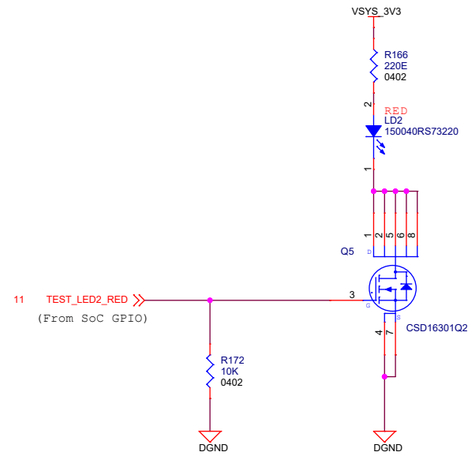
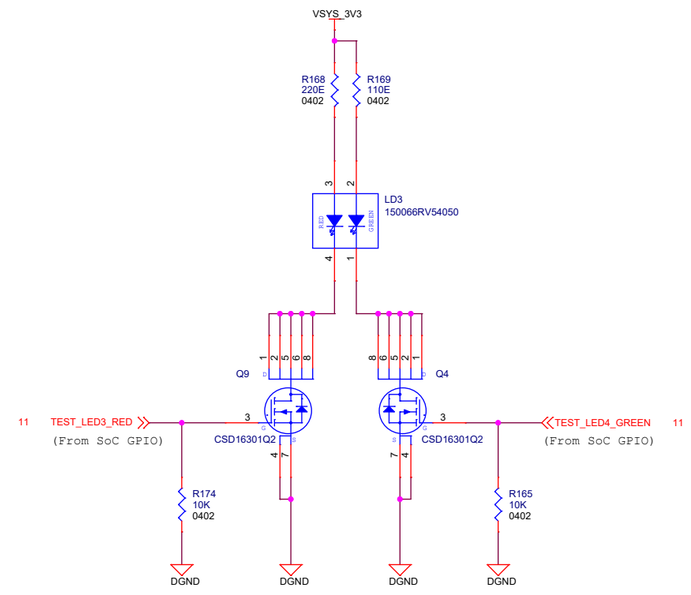
Title	XDS110 DEBUGGER	
Size C	PROC109 LP AM243	Rev E2
Date: Monday, May 24, 2021	Sheet 22 of 29	

Industrial Communication LEDs





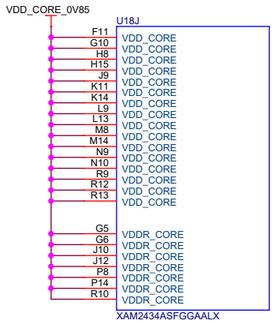


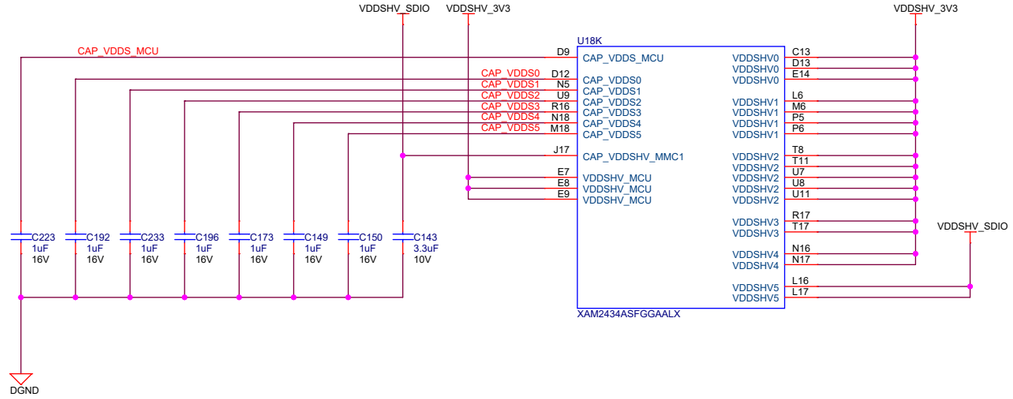


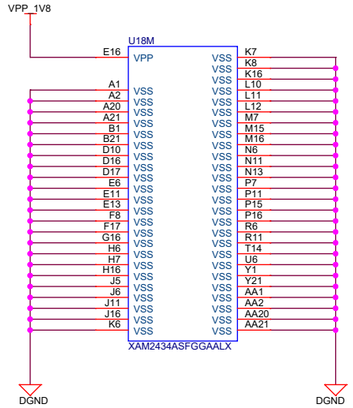
Designed for TI by Mistral Solutions Pvt Ltd

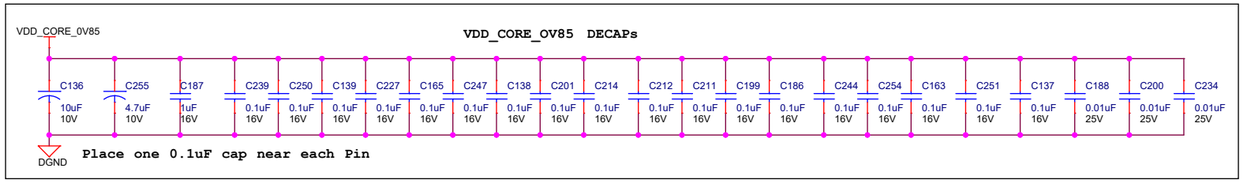
Title	INDUSTRIAL COMMUNICATION LEDs	
Size C	PROC109 LP AM243	Rev E2
Date: Monday, May 24, 2021	Sheet 23 of 29	

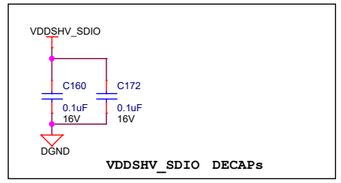
SoC Digital POWER & DECAPs

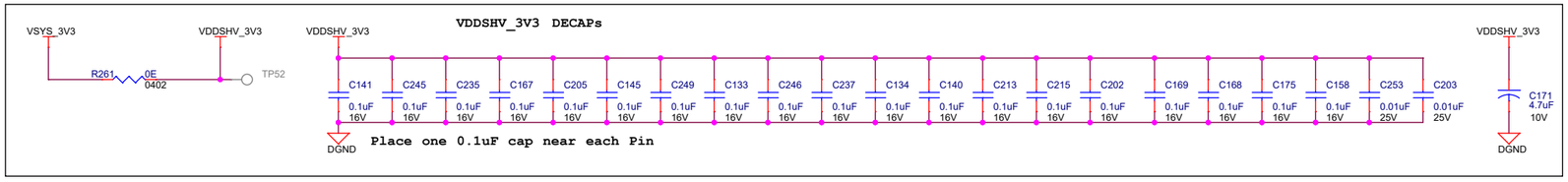








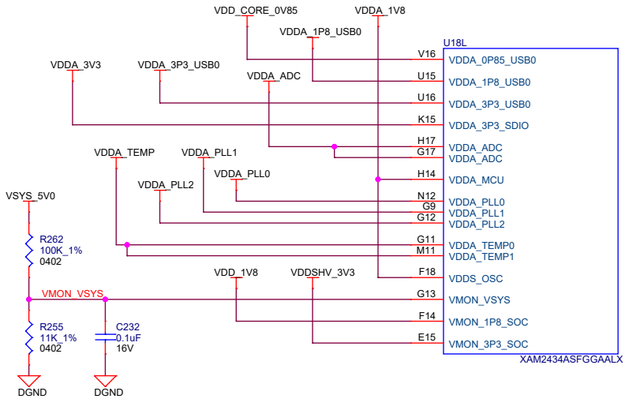


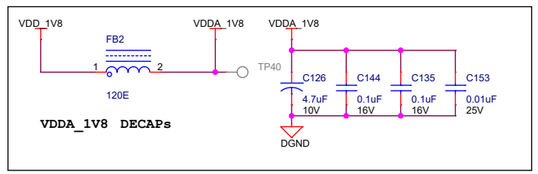


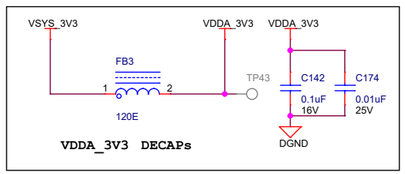
Designed for TI by Mistral Solutions Pvt Ltd

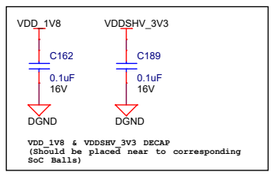
Title	SoC Digital POWER & DECAPs	
Size C	PROC109 LP AM243	Rev E2
Date: Tuesday, June 08, 2021	Sheet 24 of 29	

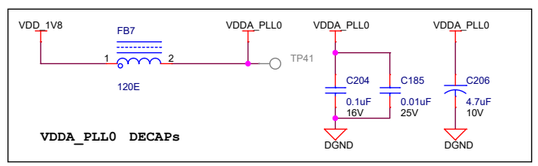
SoC Analog POWER & DECAPs

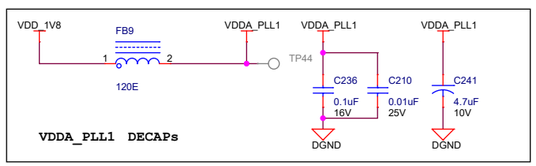


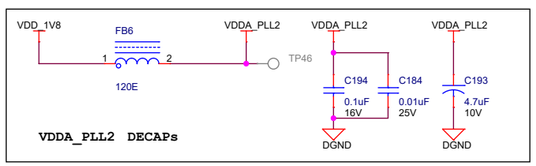


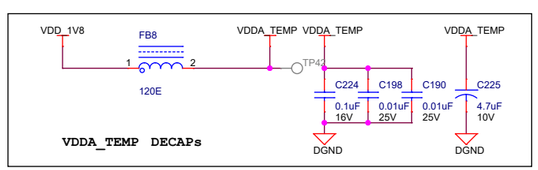


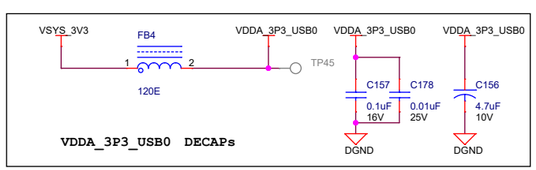


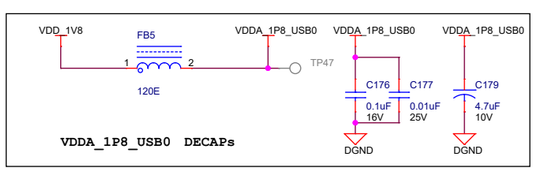


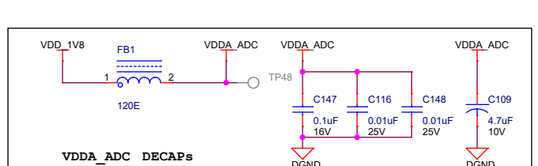












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Title	SoC Analog POWER & DECAPs	
Size: C	PROC109 LP AM243	Rev: E2
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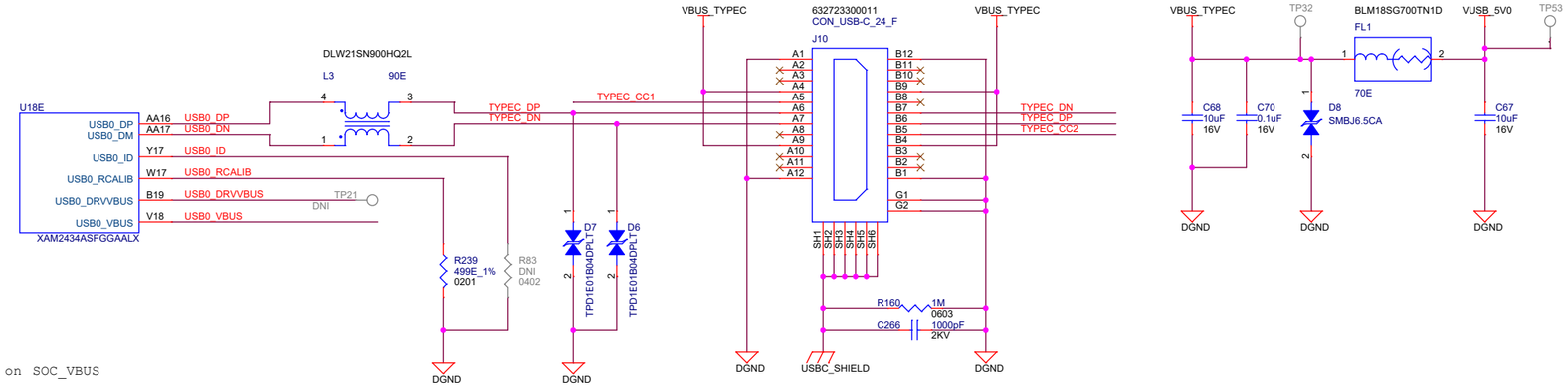
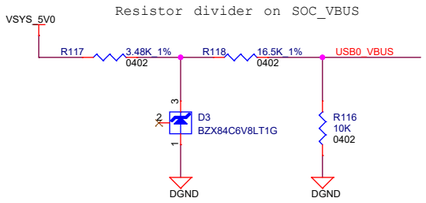
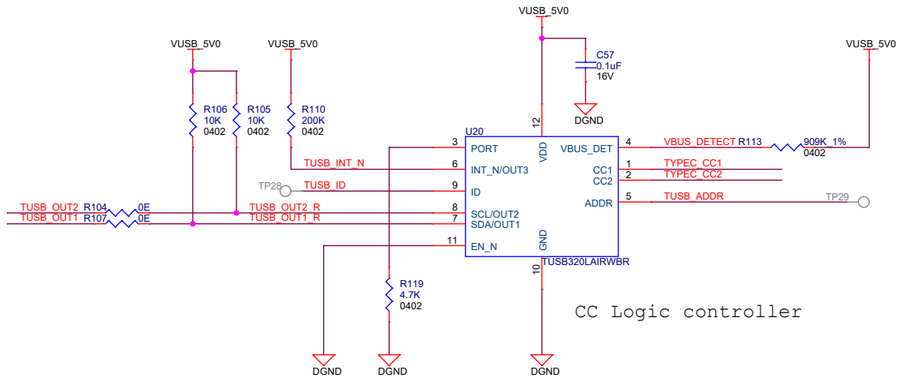
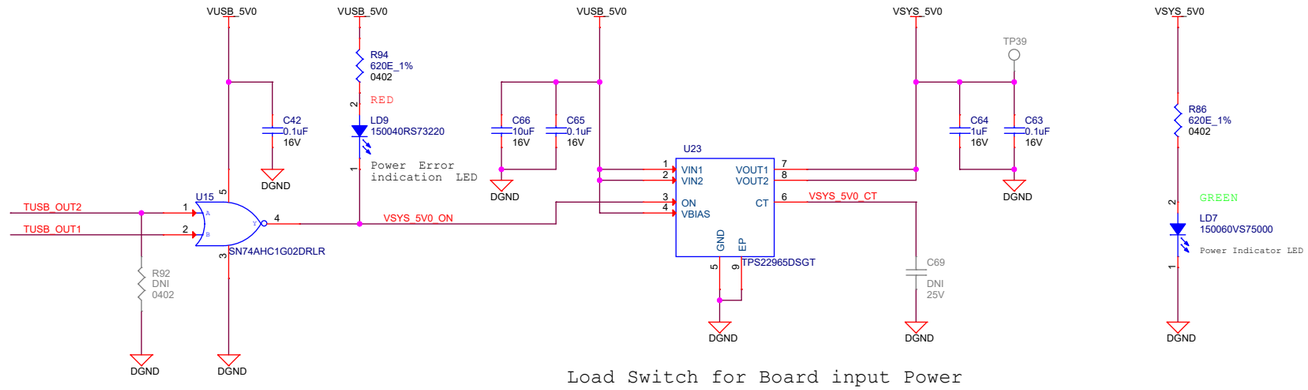
Type C Connector for Power Input & USB2.0









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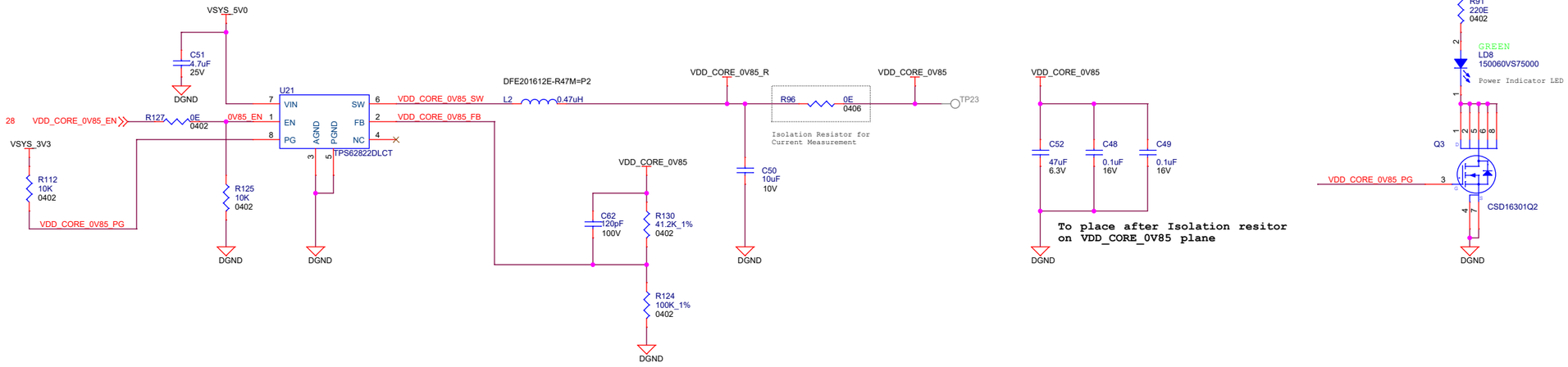
Title	BOARD POWER INPUT & USB2.0	
Size C	PROC109 LP AM243	Rev E2
Date: Monday, May 24, 2021	Sheet 26 of 29	

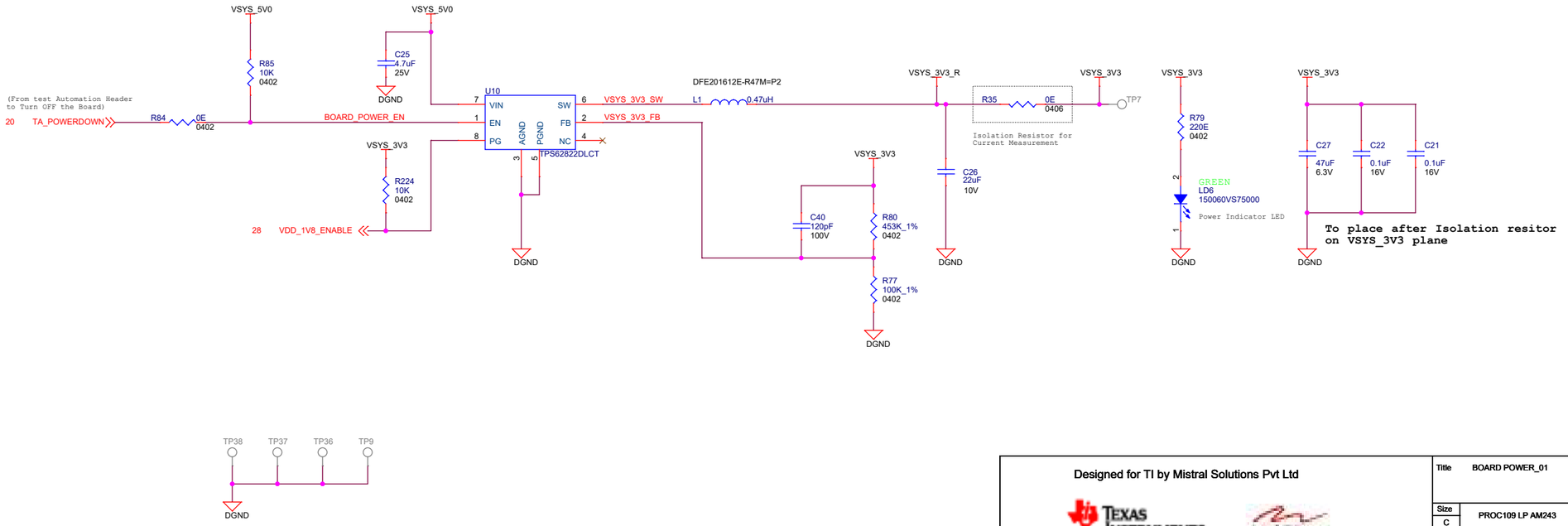
Core Voltage Generator

(0.85V, 2A)



Peripheral Voltage Generator

(3.3V, 2A)



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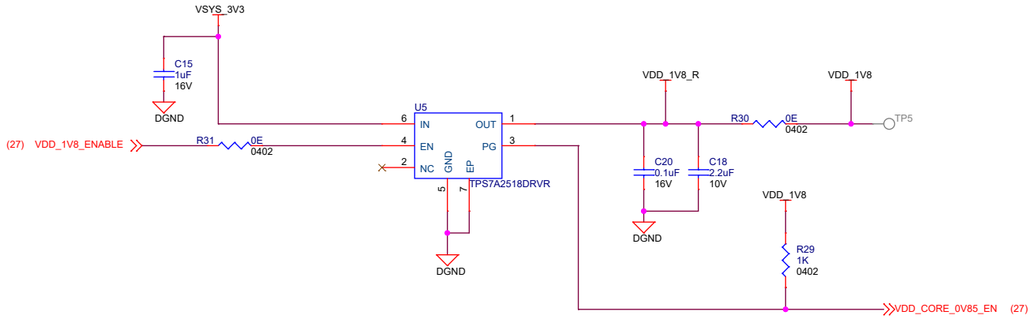
Title	BOARD POWER_01	
Size	PROC109 LP AM243	Rev
C		E2
Date:	Monday, May 24, 2021	Sheet 27 of 29

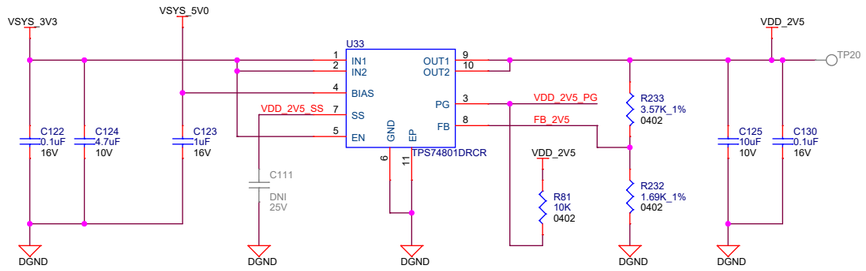
Analog Voltage LDO

(1.8V, 300mA)

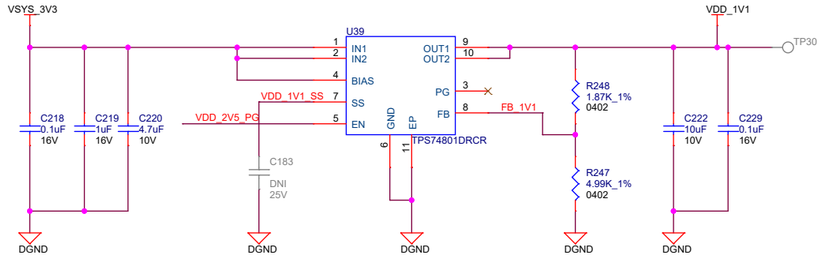


EPHY LDOs

3.3V to 2.5V

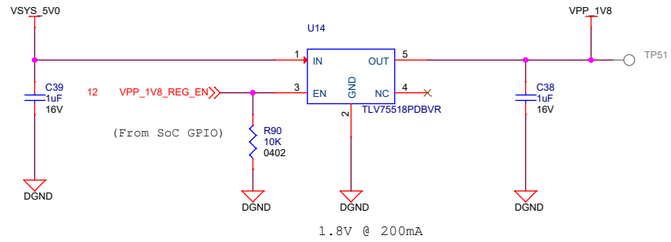


3.3V to 1.1V



eFUSE Programming Voltage LDO

(1.8V, 200mA)



Designed for TI by Mistral Solutions Pvt Ltd

Title	BOARD POWER_02		
Size	PROC109 LP AM243		Rev
C			E2
Date:	Monday, May 24, 2021	Sheet 28 of 29	

HARDWARE SCHEMATICS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards.
IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions
shall be observed.

5. These assemblies must be clean and free from flux and
all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and
packed securely before shipment.

Fiducials

FID1 DNI
FID2 DNI
FID3 DNI
FID4 DNI
FID5 DNI
FID6 DNI

BARE PCB

PCB1
PROC109E2

LABELS

Board Serial No.

LBL1
PCB LABEL
THT-103-423-10

Assembly Revision

LBL2
PCB LABEL
THT-103-423-10

LOGOs

PCB LOGO DNI
Texas Intruments

PCB LOGO DNI
TI Launch Pad Logo with web link

PCB LOGO DNI
Mistral Solutions

PCB LOGO DNI
WEEE Mark

PCB LOGO DNI
CE Mark

PCB LOGO DNI
For Evaluation only; not FCC approved for resale

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Title	HARDWARE SCHEMATICS	
Size C	PROC109 LP AM243	Rev E2
Date: Monday, May 24, 2021	Sheet 29 of 29	