Extended Data
Using the SN74VMEH22501
In a 21 Slot Back plane

Abstract

This is a collection of captured waveforms obtained from a standard 21-slot VME back plane used to evaluate the performance of the SN74VMEH22501 interface chip. Data was taken at both 25 nanosecond (2eSST specification) and 50 nanosecond (VME64 specification) pulse widths. The 2eSST draft calls for a maximum transfer rate of 320 Mbytes/second, which translates to 25 nanoseconds data pulse width. H-Spice nominal simulation data is also included for model (device and back plane) accuracy comparisons. All waveforms were taken at the connector on the back plane side.

The data pattern used consists of 8 alternating ones and zeroes followed by an equal period with no transitions. This pattern drives seven data bits and the inverted pattern drives the eighth data bit. In this eight-bit word, data bit four (D4) is inverted. Refer to the application note "VMEH22501 in 2eSST and Conventional VME Back plane Applications", appendix A for the VMEbus connector pin arrangements. The waveforms show the effects of seven signals switching in one direction and one switching the opposite direction.

The 'Case' indicates to how the slots were populated. Refer to the following table.

Case	Backplane Loading	Driving Slot
1	All slots	11
2	All slots	1
3	All slots	1
4	All slots	11
5	Slots 11 and 12	11
6	Slots 1 and 21	1
7	Slots 1, 11, and 17–21	1

The bus busy (Bbusy) line was held low by the driver and was monitored for the amount of cross talk picked up along the back plane and through the connectors.

Glossary

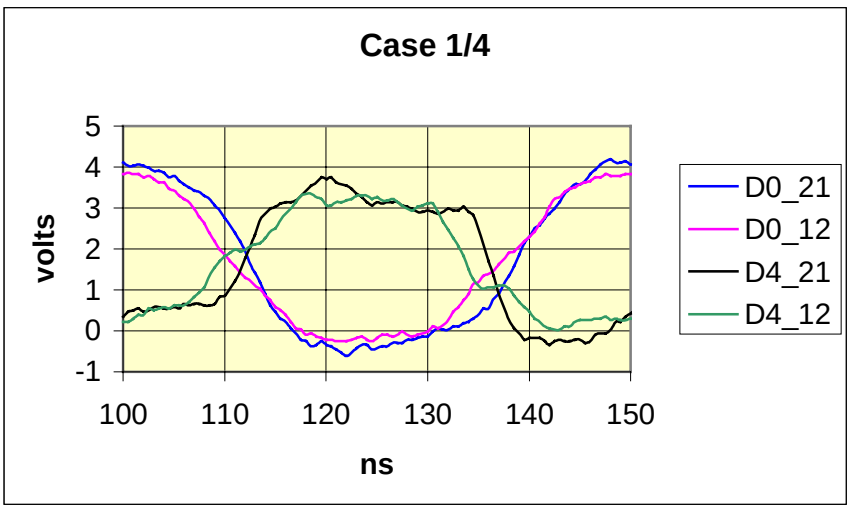
EVM	evaluation module, hardware back plane and daughter cards.
SIM	simulation results using H-Spice models for both the VMEH22501 device and the EVM.
D0_21	data bit D00 measured at back plane slot 21.

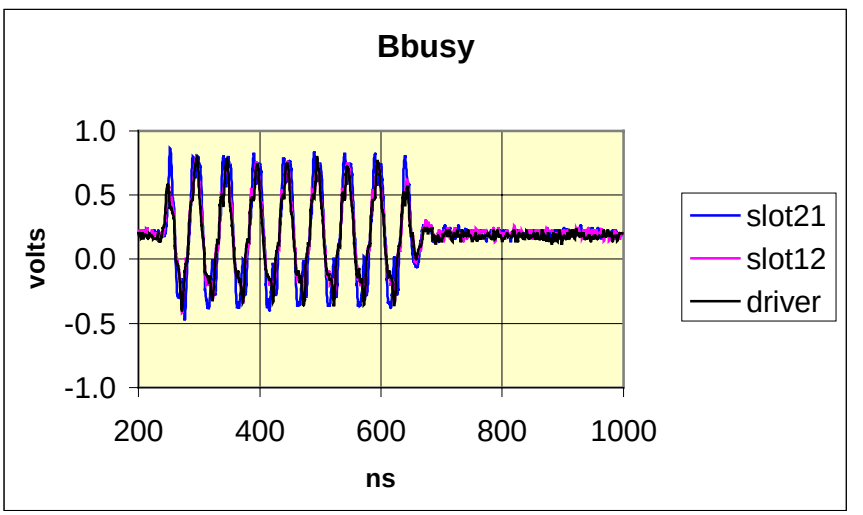
EVM Waveforms

25 Nanosecond Data Width

Case 1/4

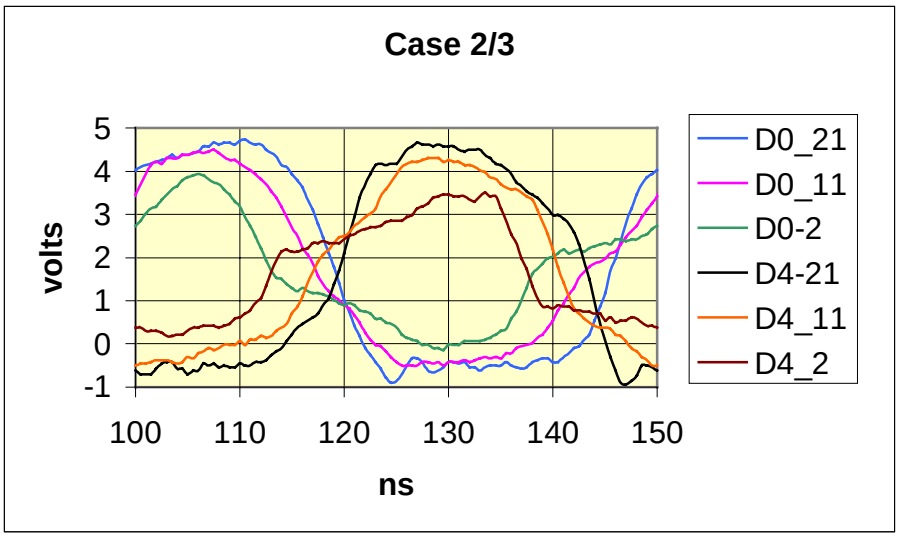
Driver: slot 11
Receiver: slot 1-10 & 12-21
D0: Normal data
D4: inverted data

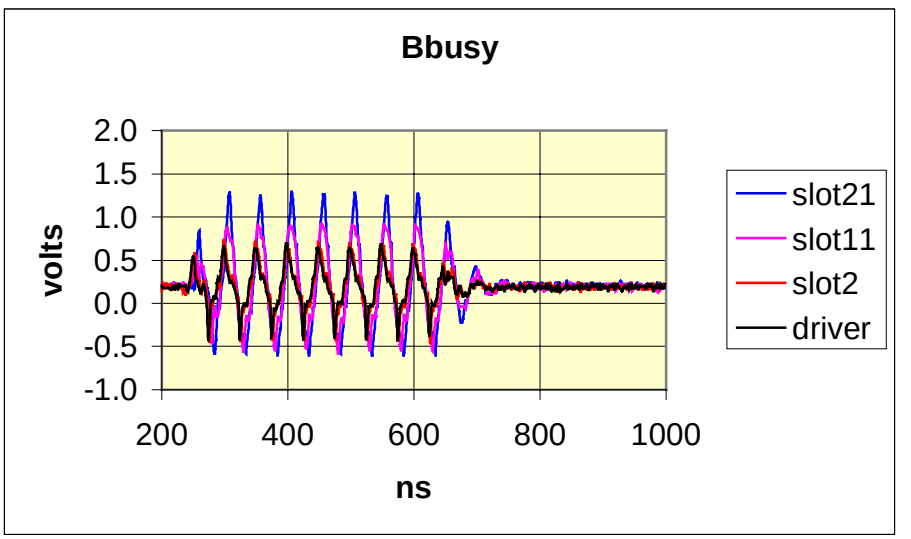




Case 2/3

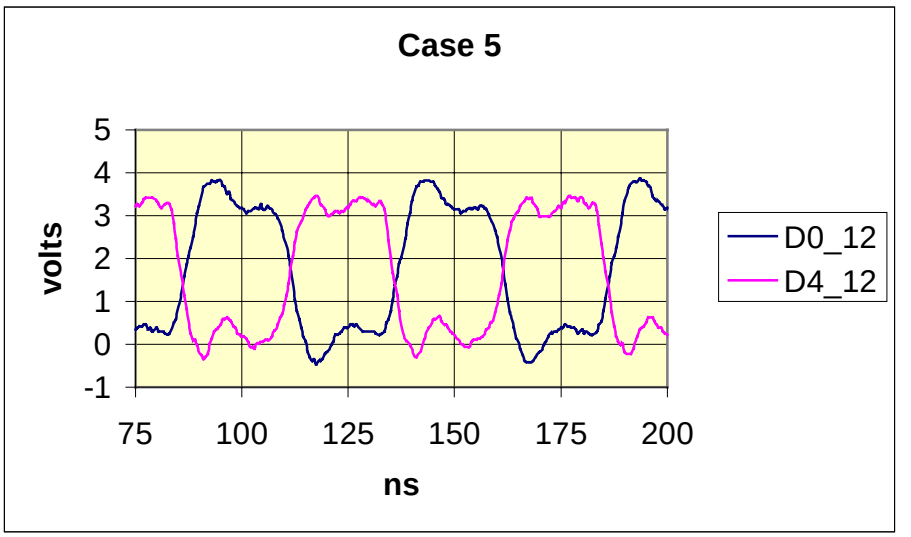
Driver: slot 1
Receiver: slot 2-21
D0: Normal data
D4: inverted data

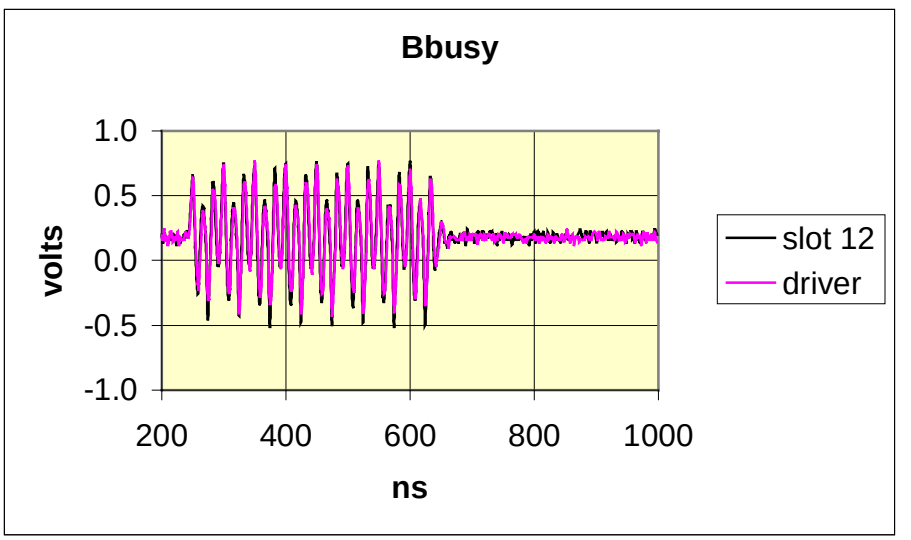




Case 5

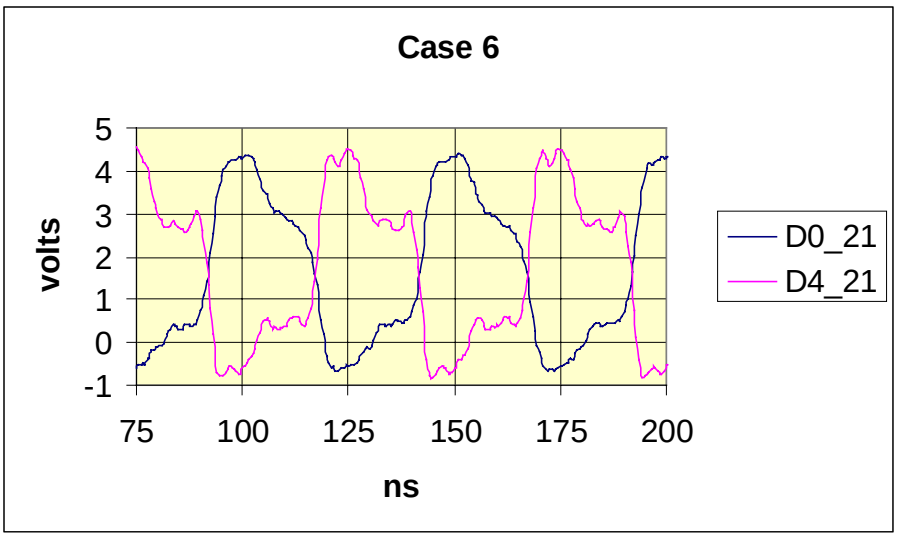
Driver: slot 11
Receiver: slot12
D0: Normal data
D4: inverted data

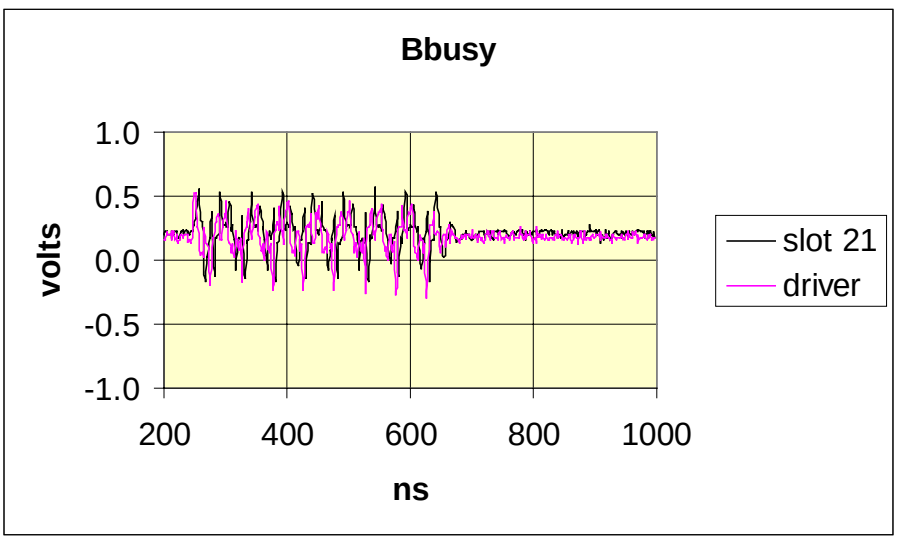




Case 6

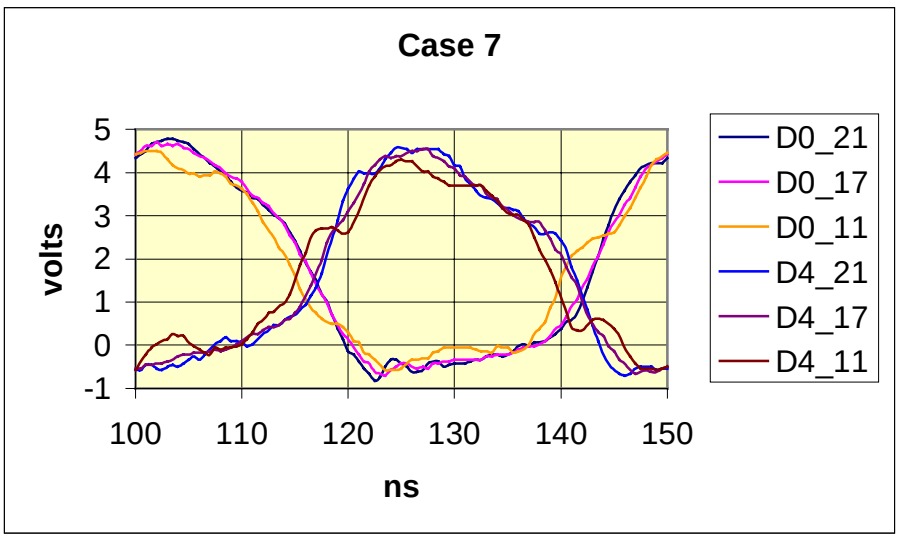
Driver: slot 1
Receiver: slot21
D0: Normal data
D4: inverted data

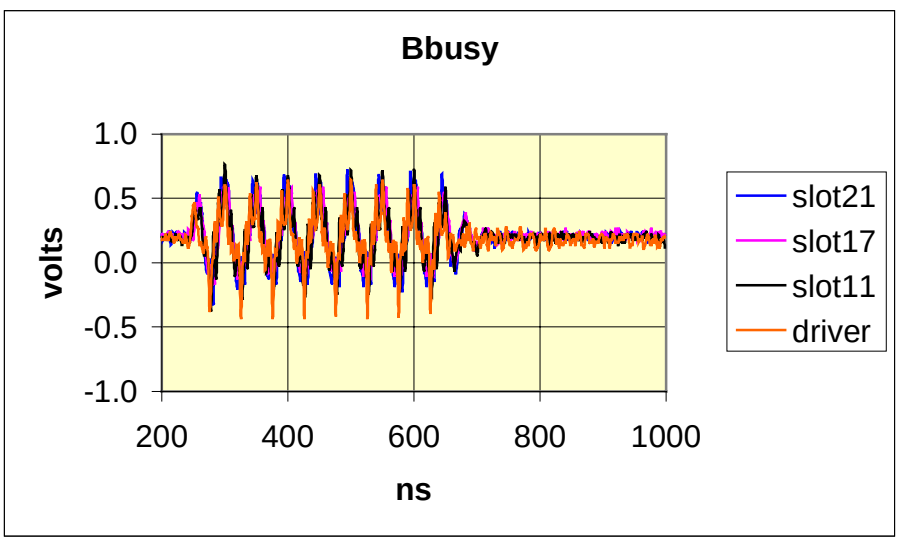




Case 7

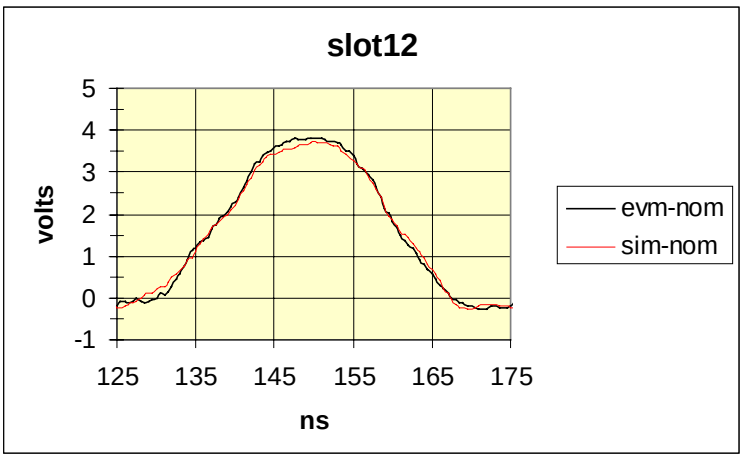
Driver: slot 1
Receiver: slot11 & 17-21
D0: Normal data
D4: inverted data

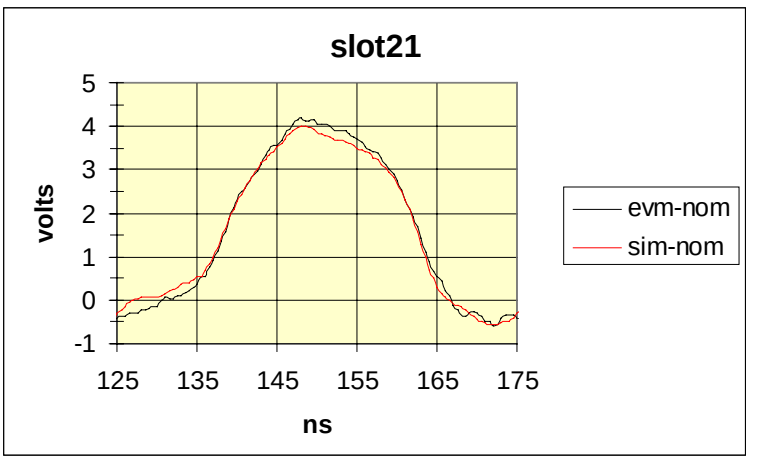




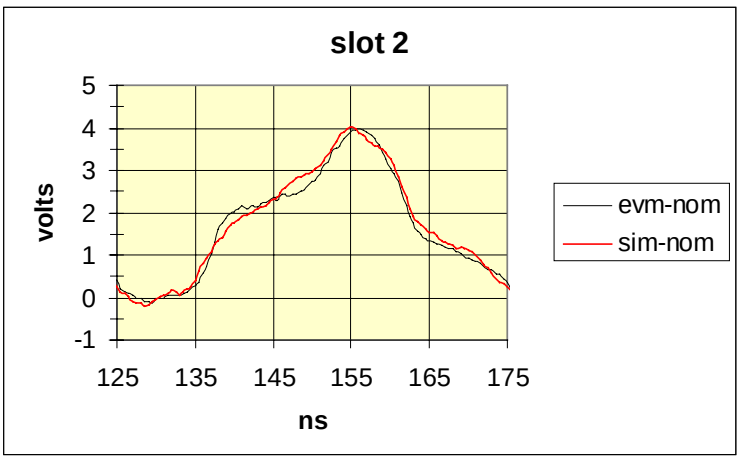
EVM & Simulation Comparisons

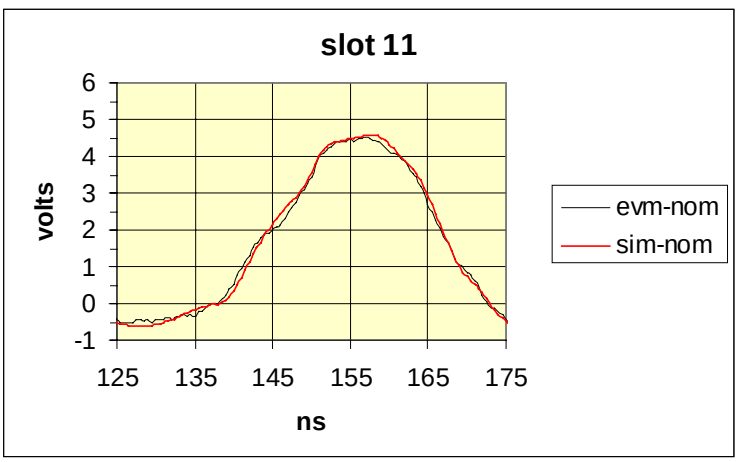
Case 1/4

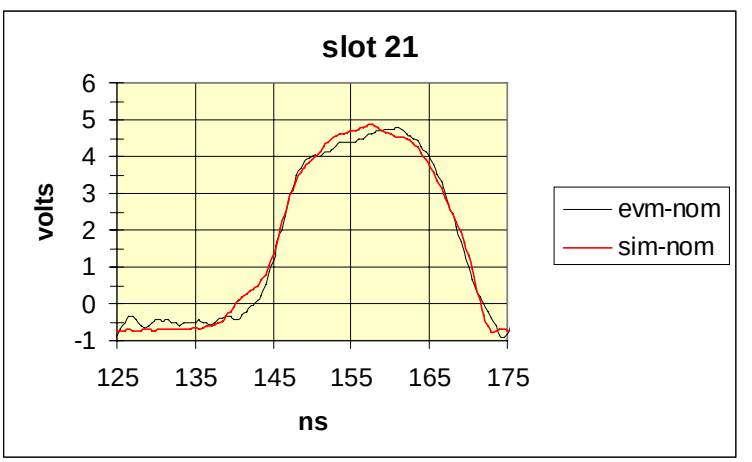

slot12
volts
5
4
3
2
1
0
-1
125
135
145
155
165
175
ns
evm-nom
sim-nom


slot21
volts
5
4
3
2
1
0
-1
125
135
145
155
165
175
ns
evm-nom
sim-nom

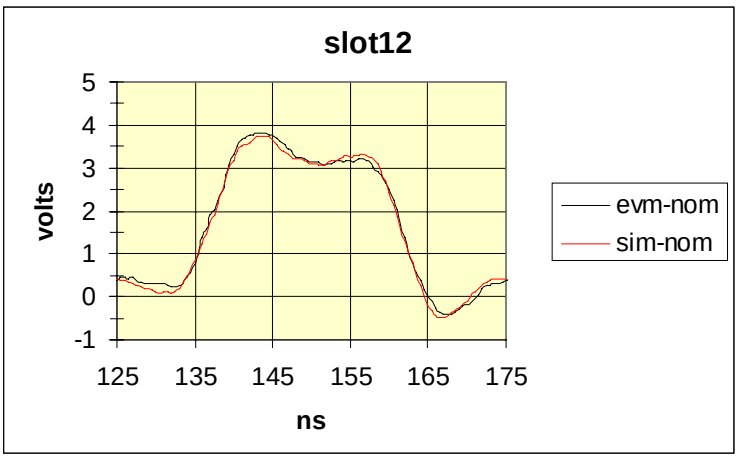
Case 2/3


slot 2
volts
5
4
3
2
1
0
-1
125
135
145
155
165
175
ns
evm-nom
sim-nom

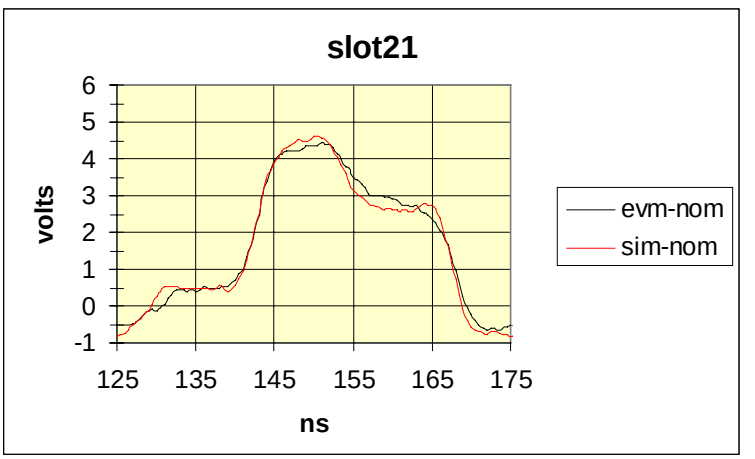

slot 11
volts
6
5
4
3
2
1
0
-1
125
135
145
155
165
175
ns
evm-nom
sim-nom


slot 21
volts
6
5
4
3
2
1
0
-1
125
135
145
155
165
175
ns
evm-nom
sim-nom

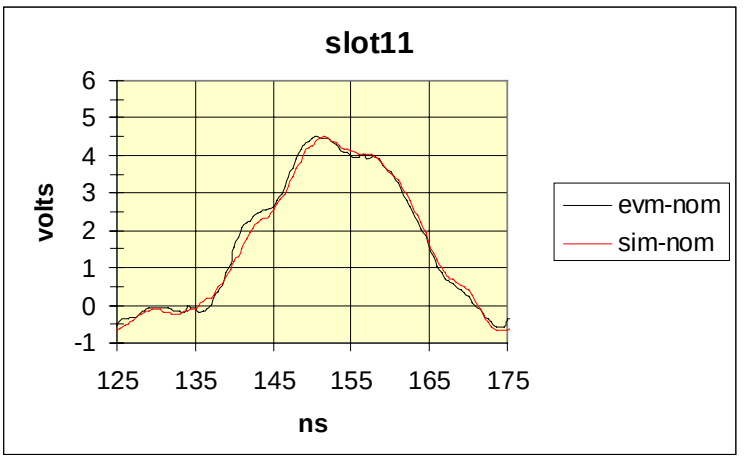
Case 5

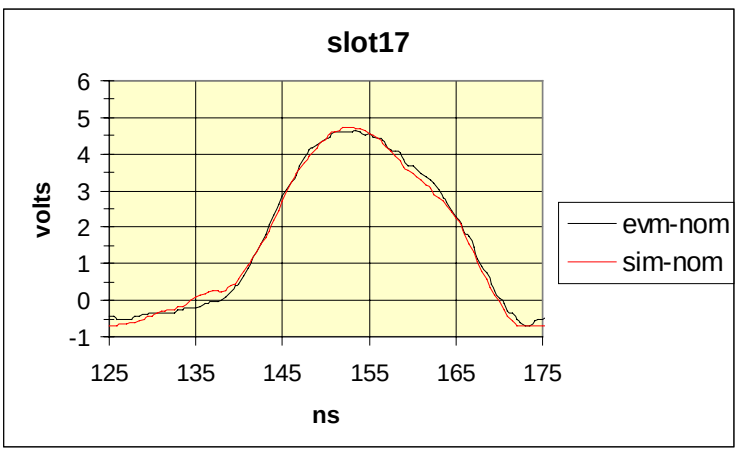

slot12
volts
5
4
3
2
1
0
-1
125
135
145
155
165
175
ns
evm-nom
sim-nom

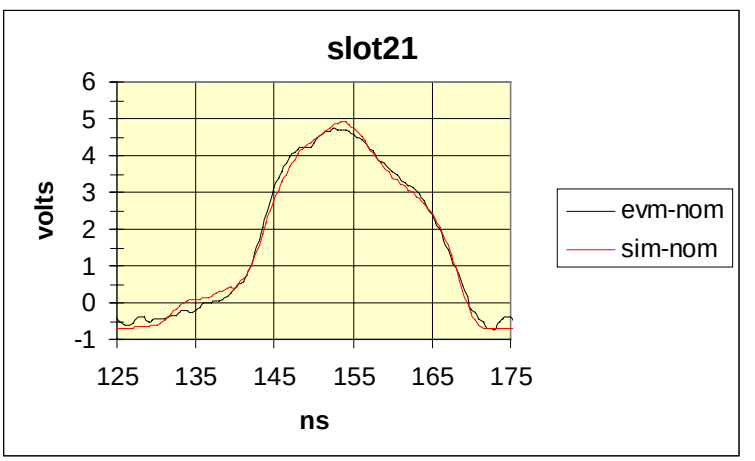
Case 6


slot21
volts
6
5
4
3
2
1
0
-1
125
135
145
155
165
175
ns
evm-nom
sim-nom

Case 7


slot11
volts
6
5
4
3
2
1
0
-1
125
135
145
155
165
175
ns
evm-nom
sim-nom


slot17
volts
6
5
4
3
2
1
0
-1
125
135
145
155
165
175
ns
evm-nom
sim-nom

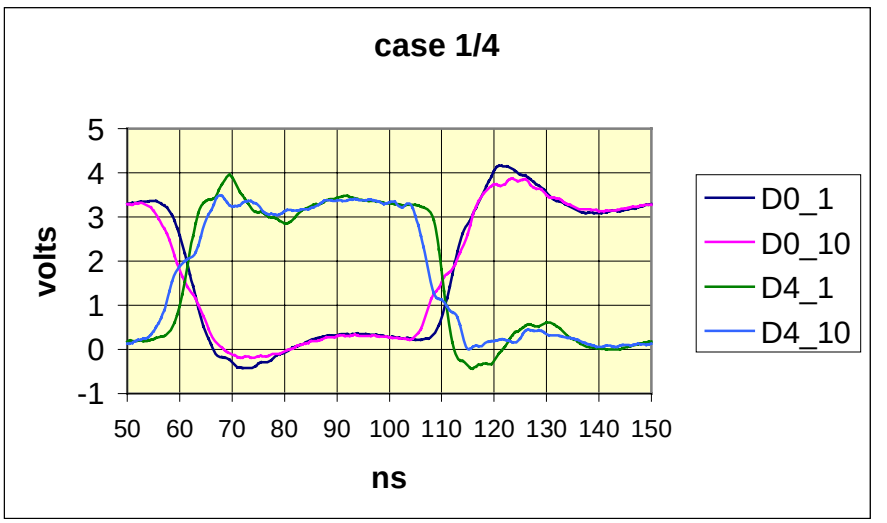

slot21
volts
6
5
4
3
2
1
0
-1
125
135
145
155
165
175
ns
evm-nom
sim-nom

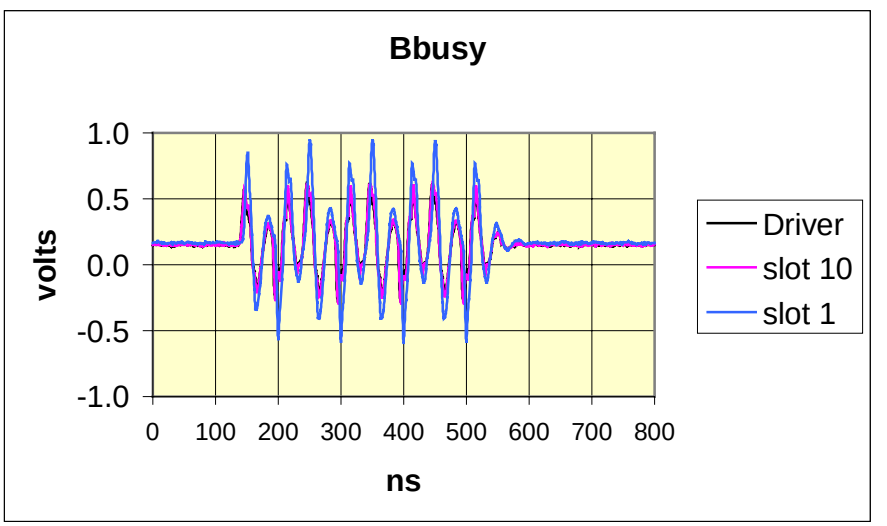
EVM Waveforms

50 Nanosecond Data Width

Case 1/4

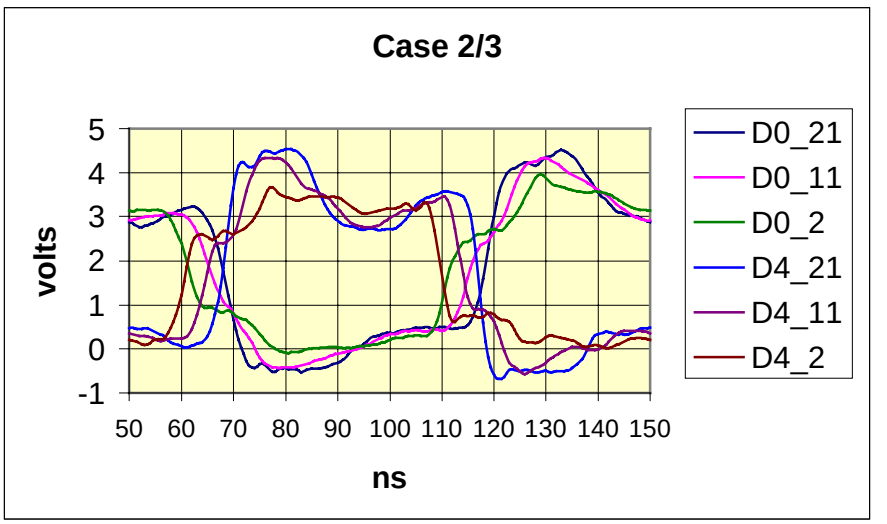
Driver: slot 11
Receiver: slot 1-10 & 12-21
D0: Normal data
D4: inverted data

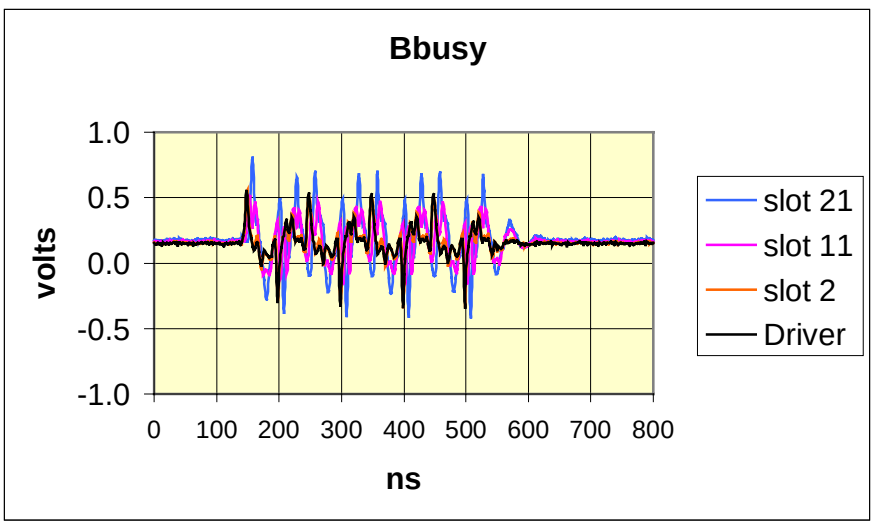




Case 2/3

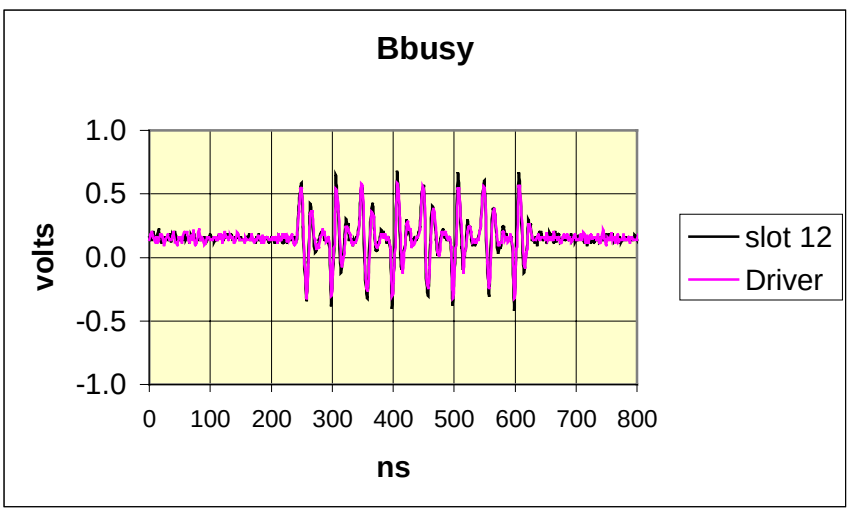
Driver: slot 1
Receiver: slot 2-21
D0: Normal data
D4: inverted data





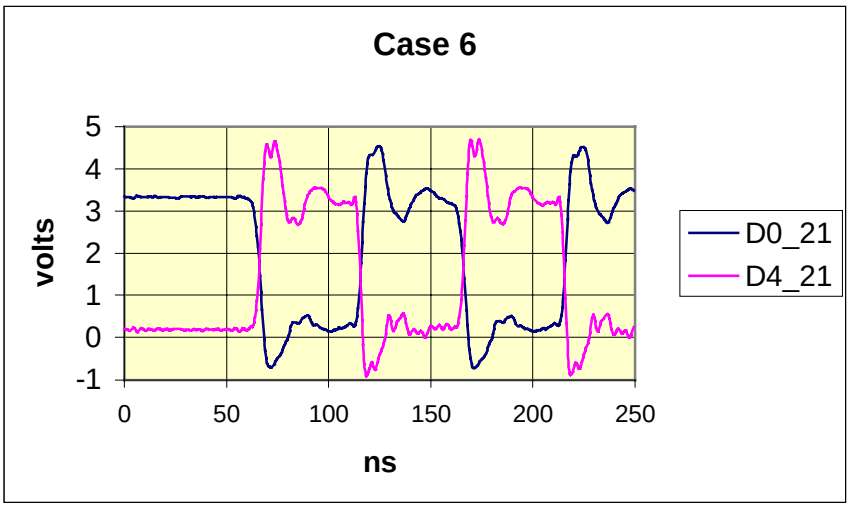
Case 5

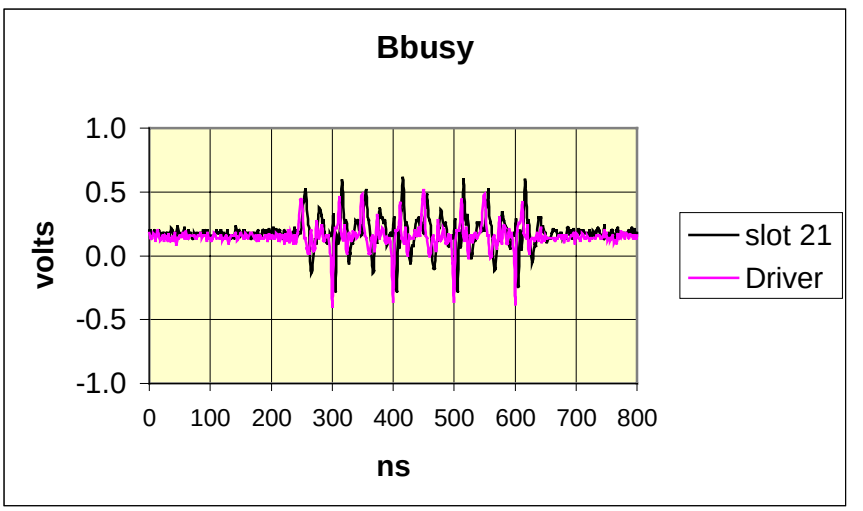
Driver: slot 11
Receiver: slot12
D0: Normal data
D4: inverted data



Case 6

Driver: slot 1
Receiver: slot21
D0: Normal data
D4: inverted data





Case 7

Driver: slot 1
Receiver: slot11 & 17-21
D0: Normal data
D4: inverted data